Preliminary

Comments

The initial results of this chapter were covered in the Chapter on Combinational Circuits & Sorting Networks. In particular, the 0-1 principle (see CLR pg 42) and Transposition Sort (See CLR pg 44) were covered at the end of Combinational Circuits Chapter.

In particular, the 0-1 principle was covered for a circuit in above chapter, but the argument given here for a linear array of processors is very similar to the one given in the previous set of slides for a circuit.

Likewise, the Transposition sort in the

previous chapter was for a circuit, but almost the same proof works here. In fact, the argument given in this set of slides show that the running time of the transposition sort is exactly n.

Given that we have only a short time left, it seems a better use of our time to not go through almost identical proofs, but instead to skip to the 2-D mesh sort algorithm, which is a very well-known algorithm.