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Growth of Intel Processors

Year of Introduction	Transistors	Processor
1971	2,250	4004
1972	2,500	8008
1974	5,000	8080
1978	29,000	8086
1982	120,000	286
1985	275,000	Intel386™ processor
1989	1,180,000	Intel486™ processor
1993	3,100,000	Intel® Pentium® processor
1997	7,500,000	Intel® Pentium® II processor
1999	24,000,000	Intel® Pentium® III processor
2000	42,000,000	Intel® Pentium® 4 processor
2002	220,000,000	Intel® Itanium® processor
2003	410,000,000	Intel® Itanium® 2 processor

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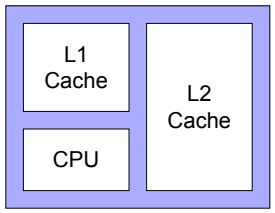

64-bit RISC CPU
w/ multithreading etc.

big level 1 cache,
bigger level 2 cache

CPU with Cache

What can we do with a billion (10^9) transistors?
Or more in a few years?

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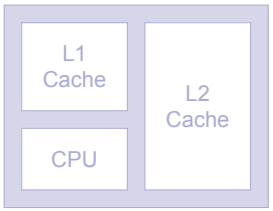
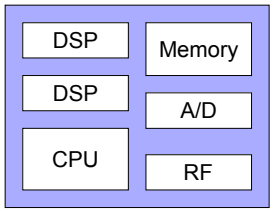


CPU with Cache



System on a Chip (SoC)

RISC CPU (ARM, etc.), cache, memory

DSP, MPEG, A/D, D/A, RF, analog

network-on-a-chip

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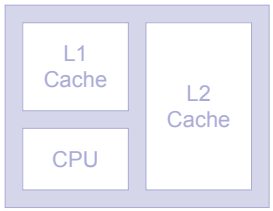
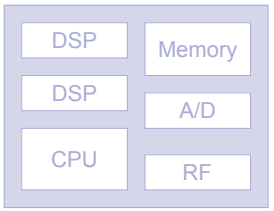


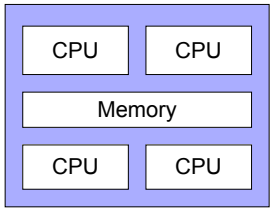
CPU with Cache



System on a Chip (SoC)

tens of powerful CPUs: RISC CPU (ARM, etc.), custom CPU, etc.

shared DRAM memory (paged, multi-port, etc.)



Multiprocessor SoC (MPSoC)

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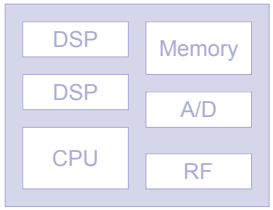
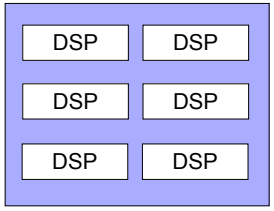
processing units customized for a specific application

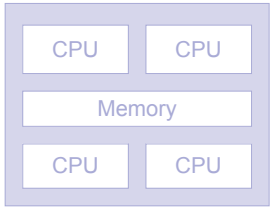
"sea of DSPs"



System on a Chip (SoC)



DSP Array SoC



Multiprocessor SoC (MPSoC)

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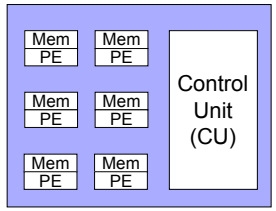
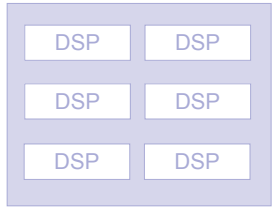


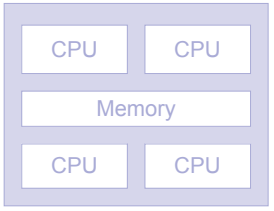
many (e.g., 100s, 1000s) small (e.g., 1-bit, 8-bit) Processing Elements (PEs)

Control Unit (CU) broadcasts instructions

SIMD Processor Array SoC



DSP Array SoC



Multiprocessor SoC (MPSoC)

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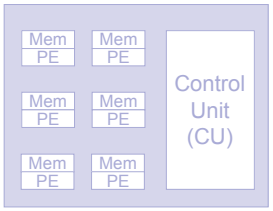
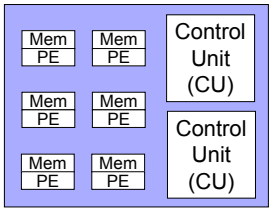
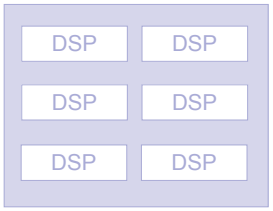


SIMD Processor Array SoC



MSIMD Processor Array SoC



DSP Array SoC

MSIMD = multiple SIMD

multiple CUs support "control parallelism"

some PEs do IF, others do ELSE

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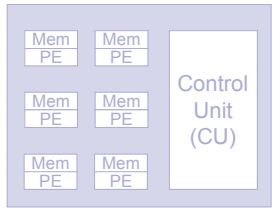
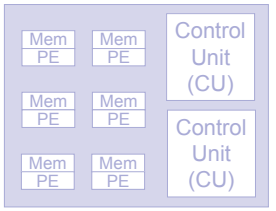


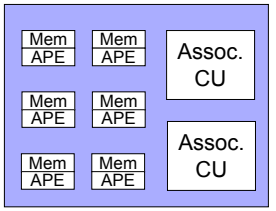
SIMD Processor Array SoC



MSIMD Processor Array SoC

SIMD or MSIMD Processor Array SoC (PASoC)

plus support for ***associative computing***



Associative MSIMD PASoC

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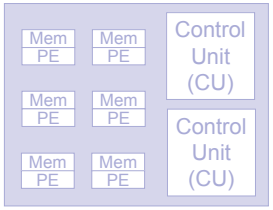
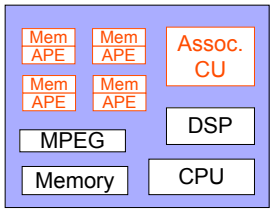
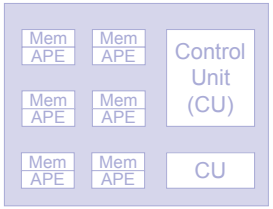
SIMD or MSIMD Processor Array SoC plus support for ***associative computing*** as part of a SoC



MSIMD Processor Array SoC



System on a Chip (SoC)

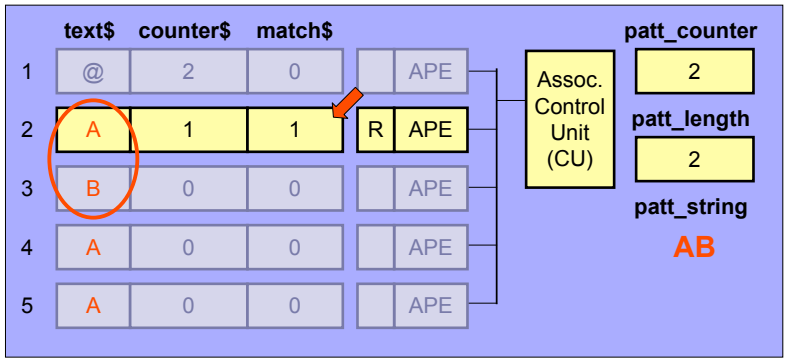


Associative MSIMD PASoC

Development of an ASC Processor

- **2001-02 — first 4-PE prototype w/ associative search, responder resolution, max/min search, not implemented**
- **2003 — scalable ASC Processor w/50 PEs, implemented on APEX 20K1000E**
- **2004 — scalable ASC Processor w/ 1-D and 2-D network, demonstrated on VLDC string-matching example & image processing example (edge detection using convolution)**
- **2005 — scalable ASC Processor w/ pipelined PEs and reconfigurable network, to be demonstrated**
- **2005 — scalable ASC Processor w/ augmented reconfigurable network and row/column broadcast, demonstrated on exact and approximate match LCS example**
- ***2006? — scalable MASC Processor w/ ? network***
- ***2007? — Multithreaded ASC/MASC Processor w/ ? network***

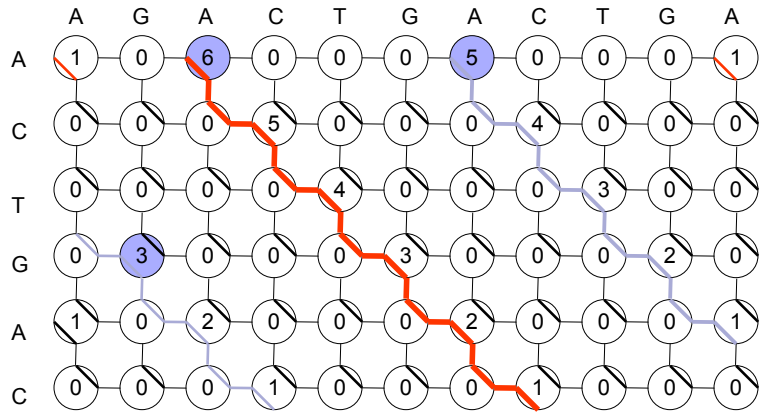
String Match by Associative Computing



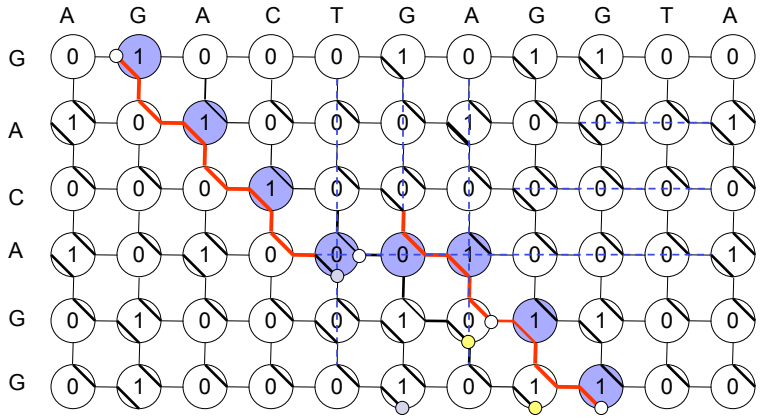
Set Responder if (match$ == 1)

Indicates cell(s) where match of pattern string AB in text string ABAA begins

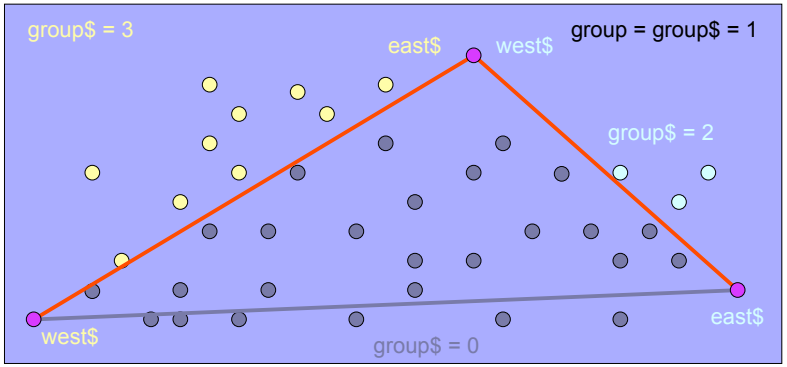
LCS Algorithm on Reconfigurable 2D Mesh

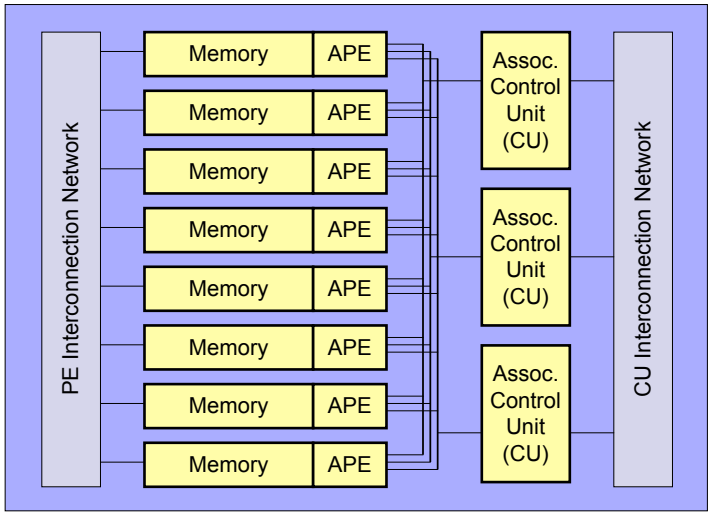


LCS Algorithm on Reconfigurable 2D Mesh



Convex Hull by Associative Computing





Multi-Associative SIMD Array w/ PE & CU Network

Some Currently Open Problems…

- **Implement & demonstrate "virtual PEs" on associative String Match and/or LCS algorithm**
- **Implement & demonstrate one or more associative Convex Hull algorithms using ASC and/or MASC**
- **Continue LCS algorithm research**
  - Investigate further the presence of "gaps"
  - Find "best" CS instead of "longest" CS
- **Demonstrate use of associative PE array in conjunction with standard processor core**