

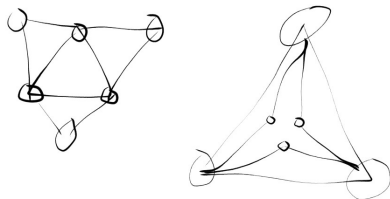
# Subgraph Isomorphism and its Application to Layout-Versus-Schematic Verification

Nathan Breitsch

March 28, 2016

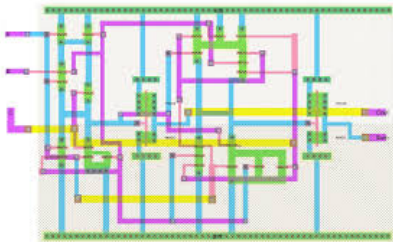
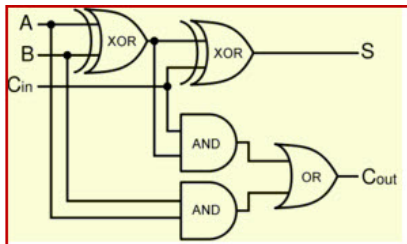
## Graph Isomorphism

Two graphs  $G = (V_1, E_1)$  and  $H = (V_2, E_2)$  are called isomorphic iff there exists a bijection  $f : G \rightarrow H$  that preserves vertex adjacency, that is, for all  $u, v \in V_1$

$$[f(u), f(v)] \in E_2 \iff [u, v] \in E_1$$


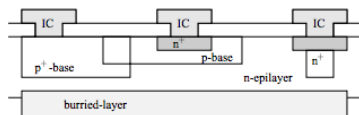
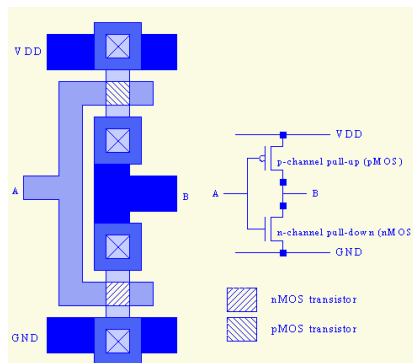
# Layout v.s. Schematic (LVS) Problem

- ▶ Schematic (left) shows interconnection of electrical components
- ▶ Layout (right) shows geometry of integrated circuit
- ▶ Do layout and schematic describe the same circuit?

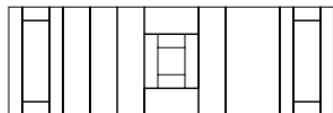


# Graph Representation of Layout

- ▶ Layout consists of multiple stacked masks
- ▶ Each mask is set of regions colored by material

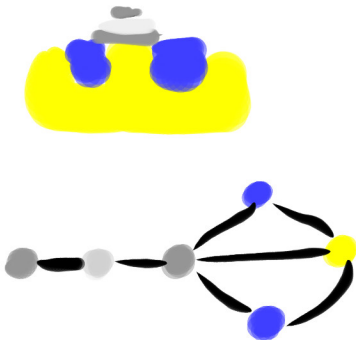


(a)



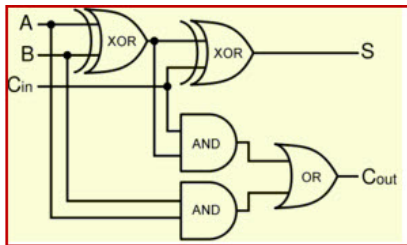
## Graph Representation of Layout

- ▶ Each region of a given material is represented by a vertex
- ▶ Junctions between regions are represented by edges
- ▶ Vertices are colored according to material

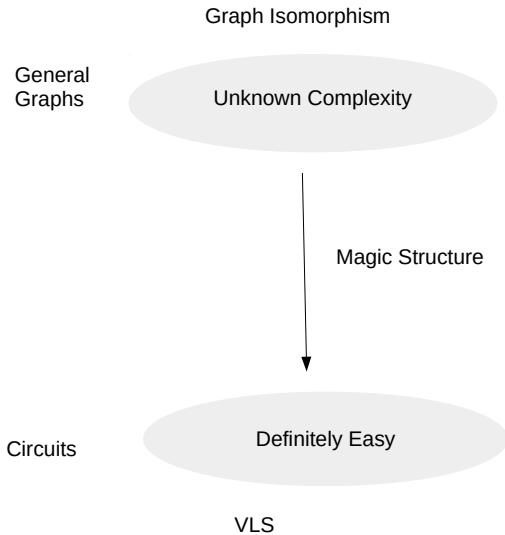


# Graph Representation of Schematic

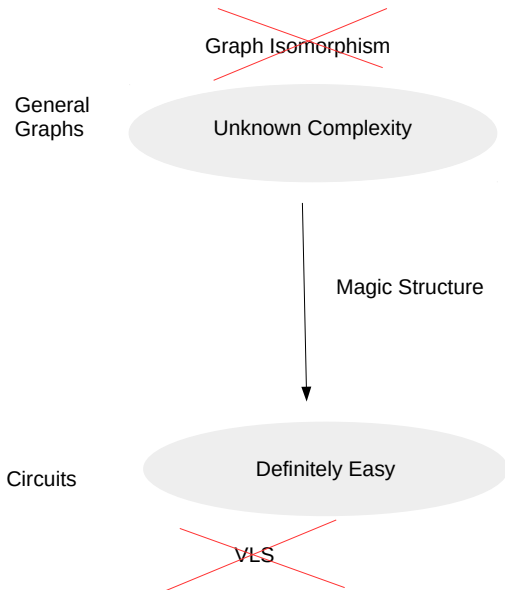
- ▶ Each conductor is vertex (called net)
- ▶ Each pin is vertex
- ▶ (Idea) connect layout graph for components to pins



# The Plan



# Plan Foiled





## Sub-Circuit Extraction

- ▶ Find a small circuit in a larger circuit
- ▶ Serves as a subroutine for practical VLS
- ▶ Related to subgraph isomorphism problem

# Subgraph Isomorphism Problem

Given two graphs  $G$  and  $H$ , determine whether  $G$  contains a subgraph  $H'$  which is isomorphic to  $H$ .

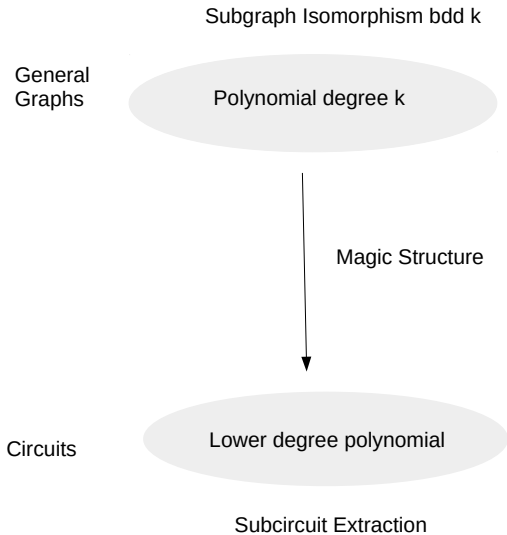
- ▶ NP Hard: we can use subgraph isomorphism to search for a clique of size  $k$ . Therefore, subgraph isomorphism is at least as hard as max clique.
- ▶ If  $|H| < k$  then complexity is reduced to  $O(|H|^k)$ .
- ▶ If  $G$  has the right structure (in addition to fixing  $|H|$ ), complexity may be reduced further.

# Brute Force Algorithm

Check all possible vertex assignments.

- ▶ There are  $\frac{|E_G|!}{(|E_G|-|E_H|)!}$  possible vertex assignments
- ▶ If  $|E_H| < k$ , this becomes  $(|E_G|) * (|E_G| - 1) * \dots * (|E_G| - k + 1)$  which is  $\Theta(|E_G|^k)$
- ▶ We can check each vertex assignment for isomorphism with  $|E_H|$  edge lookups.

# The New Plan



## Outlook Seems Bright

- ▶ Linear algorithm for planar graphs (Eppstein)
- ▶ Linear algorithm for graphs of bounded genus (Eppstein)
- ▶ "A linear matching time performance of the SCE algorithm is achievable, to the testing circuits that possess EU local distinguishability." (Ling)

# Planning Method

- ▶ Method from [Ling]
- ▶ Edge units in  $H$  (pattern graph) are tasks
- ▶ Edge units in  $G$  (target graph) are resources
- ▶ Assign tasks to resources subject to constraints

# Constraints

- ▶ Pattern vertex must be assigned to host vertex with greater or equal degree.
- ▶ Vertices must share labels.
- ▶ Edge units that share a vertex in the pattern graph must share the same vertex in the target graph.

## Scanning for isomorphic assignments

- ▶ In contrast to brute force algorithm, do not check every vertex assignment (or edge assignment).
- ▶ Instead, scan the decision tree of valid edge unit assignments, backtracking when no further assignments are possible.



## Eliminating starting points

- ▶ First, compute center spanning tree of pattern graph
- ▶ Choose center as starting vertex in pattern graph
- ▶ Eliminate starting vertices in host graph with different label
- ▶ Eliminate starting vertices in host graph with eccentricity less than that of the center in the pattern graph.

## Criticality and Cruciality

- ▶ Criticality: the number of valid host edge vertex assignments to a given pattern edge unit
- ▶ Cruciality: given a pairing of edge units (one in patten, one in host) the cruciality is the number of conflicting pairings.

Search Idea: choose the tasks with least criticality and choose the resources with least cruciality.

# Performance

- ▶ left shows linear performance in size of pattern graph (surprising)
- ▶ right shows performance in model graph

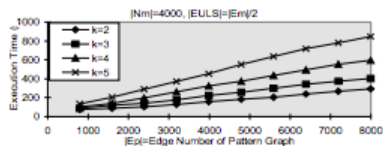


Figure 2. Near-Linear Performance

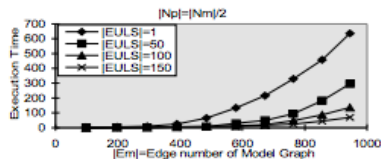






Figure 3. Impact of Label Sets

## We didn't quite make it

- ▶ Algorithm is heuristic, efficiency claims are experimental
- ▶ Algorithm appears to serve general graphs
- ▶ What is EU local distinguishability?

## References

-  Frederik Beeftink. *Advanced Subgraph Isomorphism for the Identification of Complex Device Structures*.  
[http://cas.et.tudelft.nl/space/publications/1997/beeftink\\_etcas9704\\_97.pdf](http://cas.et.tudelft.nl/space/publications/1997/beeftink_etcas9704_97.pdf)
-  David Eppstein. *Subgraph Isomorphism in Planar Graphs and Related Problems*.  
<https://www.ics.uci.edu/~eppstein/pubs/Epp-TR-94-25.pdf>
-  Zong Ling. *SubCircuit Extraction with SubGraph Isomorphism*.  
<http://software.nju.edu.cn/lingzong/papers/SCE.pdf>
-  Zong Ling. *An Effective Approach for Solving Subgraph Isomorphism Problem*.  
<http://software.nju.edu.cn/lingzong/papers/SGI.pdf>