InfiniBand[™] Architecture Specification Volume 2

	Release 1.2
	October, 2004 Final

Table 1 Revision History			
Revision	Release Date		
1.0	10/24/2000	Released version	
1.0.a	06/19/2001	Release 1.0 augmented with errata material. Updates only correct errors - no additional features have been added.	
1.1	11/06/2002	Release 1.0.a augmented with additional features.	
1.2	October, 2004	Release 1.1 augmented with additional features, including Enhanced Signaling.	

his 4 Devision History

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CHAPTER 1: INTRODUCTION

This document comprises the specification for the physical aspects of InfiniBand Architecture and addresses the following areas: 6

- Overview of the Physical Layer and the aspects that make it up
- Signal Definitions that comprise the defined connection interfaces
- Link/Phy layer that defines the encoding and lane striping functions ¹⁰
- High Speed Electrical Signaling defines the parameters for the basic link signals
 13
- Copper Cable Interconnects defines the wire cable interface
- Fiber Optic Interconnects defines the fiber attachment interface
- Mechanical Form Factors defines the standard physical structures
- Backplane Connector defines the mechanical and electrical characteristics of the connector used on the standard form factors
- Low Speed Electrical Signaling defines the parameters pertaining to the power and management signals of the backplane connector
- Power / Hot Plug defines the power delivery, control and consumption requirements for the defined form factors
 22
- System Management
- OS Power Management

1.1 DOCUMENT CONVENTIONS

The following conventions are used in this specification.

1.1.1 NORMATIVE TERMS

- Shall The use of the word **shall** indicates a mandatory requirement that must be implemented to claim compliance to this specification.
- Shall not

The use of the word shall not indicates a mandatory requirement to35not implement a given aspect in order to claim compliance to this36specification.37

1.1.2 INFORMATIVE TERMS

Should

The use of the word **should** indicates flexibility of choice in an implementation with a strongly preferred preference.

InfiniBand TM Architecture Release 1.2 VOLUME 2 - PHYSICAL SPECIFICATIONS	Introduction	October, 2004 FINAL	-
	• May		
	The use of the word may indicates flexibility tation with no implied preference.	of choice in an implemen-	1 2 3
1.1.3 COMPLIANCE NOTATION			4
	This specification has statements of compliance document. These are identified using two notated	e within the body of the tional conventions:	6
	 <u>Mandatory compliance</u>: statements in the statement text" where 'XX' is the chapter no vidual statement number. These statements isfied depending on the compliance level be 	form of " CXX-YY: umber and 'YY' is the indi- s are required to be sat- eing claimed.	789
	 Optional compliance: statements in the for text" where 'XX' is the chapter number and statement number. These statements are re- given optional feature is implemented within claimed. 	rm of " oXX-ZZ: statement 'ZZ' is the individual equired to be satisfied if a a compliance level being	1 1 1 1
	The '77' numbers for Optional compliance state	ments increment indepen-	1
	dently from the 'YY' numbers used for Mandato	ry compliance statements.	,
	Chapter 15: Volume 2 Compliance Summers	ofines the compliance	
	levels for Volume 2. Within that chapter, a sum	mary listing of all the Man-	
	datory compliance and Optional compliance sta	tements that apply for that	4
	level are shown.		
1.1.4 ARCHITECTURE NOTES			2
			2
	Architecture Note		
	This information appears in-line to clarify arch	nitected items	2
	This mornation appears in-line to claimy arch		2
1.1.5 IMPLEMENTATION NOTES			3
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	r		3
	Implementation Note		3
	This information appears in-line and describe tions.	s hints on implementa-	
	L		
			-

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1.1.6 RECOMMENDATION

Recommendation to Someone

This information appears in-line and describes a recommended approach of a feature.

1.2 REFERENCES AND RELATED DOCUMENTS

The following are documents to which this specification refers.

rne	following are documents to which this specification refers.	12
[1]	ANSI/TIA/EIA-492AAAA-A-97 - Detail Specification for 62.5-um Core Diameter/125-um Cladding Diameter Class 1a Graded-Index Multimode Optical Fibers Jan. 1, 1998	13 14 15
[2]	ANSI/TIA/EIA-492AAAB-98 - Detailed Specification for 50-um Core Diameter/125-um Cladding Diameter Class 1a Graded-Index Mul- timode Optical Fibers Nov. 16, 1998	16 17 18
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[4]	ANSI/TIA/EIA-604-10: FOCIS 10 – Fiber Optic Intermateability Standard Type LC, 1999	21 22
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[11]	IEC 1754-7-4 - Push/Pull MPO Female Plug Connector Interface	32
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	sification, Requirements and User's Guide, 1st Ed. Nov. 1993,	39 40
[47]	Amended Sep. 1997	41
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	[18] IEEE 802.3z Gigabi	t Ethernet Standard		_
	[19] ITU-T G.957 – Optic lating to the Synchro	cal Interfaces for Equipme onous Digital Hierarchy Ju	nt and systems Re- ine, 1999	1 2 3
	[20] TIA2.2.1 working sp surement Method fo	ecification TIA/EIA/455-20 or Multimode Fiber Bandw	04-FOTP204 Mea- idth – to be published	4 5
	[21] InfiniBand Architect	ure Specification, Volume	1	6
	InfiniBand ^{sм} Trade	Association, <u>http://www.in</u>	finibandta.org	7
	[22] ISO 8601 Date/Time	e Format, http://www.iso.c	h/cate/d15903.html	8
	[23] OFSTP-14 (TIA/EIA installed multimode	526-14) - Optical power l fiber cable plant, under ba	oss measurements of allot	10
	[24] System Managemer 1998. Copyright(c)1 Inc., Duracell Inc., E Linear Technology C subishi Electric Cor Toshiba Battery Co.	nt Bus Specification, Revis 996, 1997, 1998, Benchm Energizer Power Systems, Corporation, Maxim Integra poration, National Semico , Varta Batterie AG.	sion 1.1, December 11, harq Microelectronics Intel Corporation, ated Products, Mit- nductor Corporation,	12 13 14 15
	[25] The I2C-Bus Specification, Version 2.0, December 1998, Phi Semiconductors		mber 1998, Philips	17
	[26] IEEE Standard 181-	2003		20
				21
1.5 ACKNOWLEDGMENTS	This specification repres companies. Special than	pecification represents the collaboration of a number contributing inies. Special thanks to those who contributed.		22 23 24
1.3.1 STEERING COMMITTEE				25
	The following individuals sociation through the Ste 1.0 and 1.1 or creation of	owing individuals served as directors of the InfiniBand SM Trade As n through the Steering Committee during the creation of Release 1.1 or creation of Release 1.2 of this specification:		26 27 28 29
1.3.1.1 Co-CHAIRS - DIRECTORS				30
1.3.1.2 M EMBERS	Tom Bradicich	Tom Macdonald		31 32 33 34 35
	Jacqueline Balfour Kevin Deierling Balint Fleisher Dr. Alfred Hartmann David Heisey	Ken Jansen Michael Krause Todd Matters Ed Miller John Pescatore	Jim Pinkerton Martin Whittaker Bob Zak	36 37 38 39 40 41

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1.3.2 TECHNICAL WORK GROU	1.3.2 TECHNICAL WORK GROUP			
	The following individuals (TWG) with responsibility during the creation of Re this specification:	s served as members of t ty for the oversight of th eleases 1.0 and 1.1 or c	the Technical Work Group e technical production creation of Release 1.2 of	234
1.3.2.1 Co-chairs			67	5
	Dwight Barron Paul Grun	Jeff Hilland Irving Robinson	David Wooten g	} } 10
1.3.2.2 M EMBERS			1	11 12
	Dr. Alan Benner Mark Bradley Wolfgang Cristl Diego Crupnicoff	Dr. Al Hartmann Michael Krause Bill Lynn Ed Miller	Dr. Greg Pfister 1 Greg Still 1 Ken Ward 1 1	13 14 15 16 17 18
1.3.3 VOLUME WORKING GROU	IP		1	19 20
	This volume is authored Workgroup (EWG) of the groups that are part of th <i>tecture Specification, Vo</i> consultation and review	by the membership the InfiniBand Trade Association are blume 1. The EWG is inc	e Electrical/Mechanical ciation. The other working e listed in <i>InfiniBand Archi-</i> debted for their efforts in	21 22 23 24 25
1.3.3.1 Co-chairs	The following individuals	s served as co-chairs of	the EWG during the cre-	26 27
	Mike Chastain	David Moss	on: 2 2 3 3	29 30 31
	The following individual Release 1.2 of this spec	served as chair of the E ^v	WG during the creation of	32 33
	Moises Cases		3 3 3 3 4 4 4 4	<pre>>+ 35 36 37 38 39 40 41 42</pre>

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1.3.3.2 VOLUME EDITOR			1	1
	The following individual volume during its creation	served as editor of Releon	ease 1.0 and 1.1 of this 2	2
	Greg Still		4	1
			6	5
	The following individual during its creation:	served as editor of Rele	ease 1.2 of this volume 7	7 3
	Alan Benner		9) 10
1 3 3 3 SUDTEAM LEADEDS			1	11
1.3.3.3 OUBTEAM LEADERS	The following individual		dara and anasitis shartar 1	12 13
	editors of Release 1.0 a	and 1.1 of this volume du	uring its creation: 1	14
	Bill Bunton	Dominic Goodwill	Trevor Williams	15 16
	Jav Diepenbrock	John Leder Siamak Tavallaei	1	17
	, .		1	18
			2	20
	The following individuals editors of Release 1.2 c	s served as subteam lea of this volume during its	ders and specific chapter 2 creation: 2	21
	Alan Benner	Jay Diepenbrock	2	23
	Der Gecchi	Trevor williams	2	24 25
1.3.3.4 INDIVIDUAL CONTRIBUTOR	RS		2	26
	The following individuals 1.1 of this volume during	s provided active contrib g its creation:	utions to Release 1.0 and $\frac{2}{2}$	27 28
	Andrew Alduino	Art Kimmel	Harry Rogers 3	<u>29</u> 30
	Paul Artman Brian Beaman	Don Lentz Dennis Miller	Art Rousmaniere Richard Schumacher ³	31
	Dave Brown	J. P. Miller	Kim Sides 3	32 32
	Steve Contreras	Mark Myers	Bill Stanley 3	34
	Casimer DeCusatis	Istvan Novak	Dan Stigliani 3	35
	Pat Egan	Tom Osten	Pat Thaler	36 37
	Stillman Gates Ali Ghiasi	Ali Oztaskin Ken Privitt	Chris Trudeau Jim Warren	38
	Lowell Good	Kevin Przybylski	3	39
	Ken Gross	Eddie Reid	4	+U 11
			4	12

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	The following individuals provid this volume during its creation:	ed active contributions to Release 1.2 of
1.4 DISCLAIMER	Moises Cases John Calvin Del Cecchi William Cerreta Hillel Chapman Ian Colloff Casimer M. DeCusatis Christy Devonport Joseph (Jay) Diepenbrock Ronen Eckhouse Shahar Eytan Andy Kayner Tadashi Kumamoto Todd Leonard Jacques Longueville Gregory Mann Like any document, this specific clarity, and enhancements. The site at http://www.infinibandta.o and updates to this specificatio	Padraig McDaid J. P. Miller Keith Murr Dale Murray Jay Neer John Petrilla Greg Pfister Daniel Reed Eddie Reid Michael Rost Peter Smith Mike Sorna Greg Still Antonius Susanto Trevor Williams

Glossary

1 2

CHAPTER 2: GLOSSARY

		3
		4
3U	A chassis size defined by the IEEE 1101.10 specification.	5
<u>ell</u>	A phaseig size defined by the IEEE 1101 10 aposition	6
80	A chassis size defined by the TEEE TTOT. To specification.	/
_L	The L suffix to a signal name indicates a low true signal.	8 9
Address Handle	An object that contains the information necessary to transmit messages to a remote port over <u>Unreliable Datagram</u> service.	10 11 12
Actively Managed Chassis	An Actively Managed Chassis provides an InfiniBand TM specified <u>GUID</u> and physical <u>Slot Information</u> to every <u>IB Module</u> on the Module's unique <u>IB-ML</u> . In addition, it provides a <u>Chassis Management Entity</u> on at least one IB Module's IB-ML. In an actively managed chassis, the Slot Infor- mation for every Module provides information identifying all of the <u>Slot(s)</u> that have access to the CME.	13 14 15 16 17 18
Adapter	Also called I/O adapter. Please see <u>Host Channel Adapter</u> or <u>Target</u> <u>Channel Adapter</u> . A form of TCA which conforms to the InfiniBand™ Architecture form factor definition. The term adapter by itself is over- loaded due to its general use in the computer industry and should not be used by itself. Typically the term adapter pertains to the channel adapter but is also used in the context of an IO adapter.	19 20 21 22 23 24
Anycast	An identifier for a set of interfaces (typically belonging to different nodes). A packet sent to an anycast address is delivered to one of the interfaces identified by that address (the "nearest" one, according to the routing pro- tocols' measure of distance).	25 26 27 28
Attribute	The collection of management data carried in a Management Datagram.	29 30
Aux Power	The 5V auxiliary power input to an <u>IB Module</u> that is provided on the <u>VA_In</u> pin. This is the standby power source used when Bulk Power is off.	31 32 33
Average Optical Power	The optical power measured using an average reading power meter when transmitting a specified code sequence as defined in the test pro- cedure.	34 35 36 37
B_Key	Please see <u>Baseboard Management Key</u> .	38
		39
Backplane	Physical PCB into which an IB Module plugs, this may be into a Server, Switch, I/O Chassis, etc.	40 41
		42

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Backplane Connector	The connector located in a <u>Server</u> , <u>Switch</u> , <u>I/O Chase</u> with an <u>IB Module</u> s <u>Edge Connector</u> .	sis, etc. that mates 1	
Base LID	The numerically lowest Local Identifier that refers to a Port.		
Baseboard Managed Unit	Any Unit which provides InfiniBand™ specification defined information about itself by a Baseboard method MAD operation through the Infini-Band™ link.		
Baseboard Management Key	A construct that is contained in IBA management dat cate that the sender is allowed to perform the reques	tagrams to authenti- sted operation.	
Baseboard Management	Management of physical hardware (environmentals, LEDs, etc.). Considered synonymous with System N opposed to "Subnet Management".	Vital Product Data, 11 lanagement as 12	
Baseboard Management Proxy	A Unit which provides the means to translate InfiniBa Management Datagram (MAD) requests and respon- other transports on behalf of one or more other entities	and [™] Baseboard 14 ses to IB-ML or 15 es. 16	
	The proxy must be addressable by the InfiniBand operations to be targeted to it (aka it has a LID)	18 subnet to allow 18 19	
Baud	The signaling speed on a lane in transitions per seco	ond. 20	
Beacon Sequence	The periodic transmission of the <u>Training Sequence</u> <u>set</u> . The Beacon sequence is used to wake or begin the device on the opposite end of a <u>Link</u> that may be is state or has been just attached to the link.	1 <u>Control Ordered-</u> Link Training with in a power managed 24	
BER	Bit error rate.	26	
втн	Base Transport Header.	28	
Board	Physical, pluggable entity that is defined by the Infini	Band™ Architecture. 29	
Bulk Power	The 12V main power input to an IB Module that is propins.	ovided on the VB_In 31	
Burst-BER	Number of bit errors measured within a sliding windo	w. 34	
Byte Striping	The byte stream representing the packet is sent by d sequentially across the available <u>Physical Lanes</u> , on order. The first byte goes in lane 0, the second in lan 2 and so on. When the last physical lane is reached, again with lane 0.	listributing the bytes e byte per <u>Lane</u> , in e 1, the third in lane the process starts	
CA	Please see <u>Channel Adapter</u> .	40 41 42	
InfiniBand TM Architecture Release 1.2 Volume 2 - Physical Specifications	Glossary	October, 2004 FINAL	-
---	---	---	----------------------------
Carrier Module	The carrier module, designed specifically for each defines the thermal, EMI, ESD and vibration/shoc	n size of IB Module k interface to a chassis.	1 2
CDR	Clock Data Recovery unit		3
Center Wavelength	The nominal value of the central wavelength of the laser. This is the wavelength (see <u>FOTP</u> -127) whe power resides.	e operating, modulated ere the effective optical	5 6 7
Channel	The association of two queue pairs for communic	ation.	8 9
Channel Adapter	Device that terminates a link and executes transport of <u>Host Channel Adapter</u> or <u>Target Channel Adap</u>	ort-level functions. One <u>ter</u> .	10 11
Chassis	The collection of IB Modules, and their associated resources housed within a single mechanical pace Server, Switch, I/O Chassis, etc.	d power and cooling kage. This may be a	12 13 14 15
Chassis GUID	8 bytes of Globally Unique ID for every Chassis		16 17
Chassis Management En- tity	The Chassis Management Entity may or may not it's simplest form the CME is merely an IB-ML de/ provide proxy access to the IB Modules IB-ML.	include a processor. In ⁄MUX. The CME may	18 19 20
Clock Compensation	The <u>SKIP ordered-set</u> is used for clock compensation or drop a <u>SKP</u> symbol from the <u>Control Ordered-set</u> input/output buffer from over-running or under-running or under-runn	tion. A device may add set to prevent it's link nning.	21 22 23
СМЕ	Please see Chassis Management Entity.		24 25
СОМ	The Comma symbol is transmitted to identify the s Sequence 1, Training Sequence 2 or SKIP ordered	start of a <u>Training</u> ed-set.	26 27 28
Compliance Channel	A worst-case connection from driver to receiver. T and the transmitter define the minimum acceptabl ceiver shall be capable of receiving at a specified	he compliance channel le inputs which a re- bit error rate.	29 30 31
Compliant Channel	A compliant channel is any channel which provides which is better than the <u>Compliance Channel</u> .	s a signal at the receiver	32 33 34
Control Ordered-set	Control Ordered-sets are used for <u>Link Training</u> a <u>tion</u> . The first symbol of all ordered-sets is the <u>CC</u> symbols are unique to the set type.	nd <u>Clock Compensa-</u> M symbol, additional	35 36 37
Cover	The protective cover which mates with the carrier outer surface of an <u>IB Module</u> .	module defining the	38 39 40 41 42

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CQE		
CRC	Please see Cyclic Redundancy Check.	
Cyclic Redundancy Check	A number derived from, and stored or transmitted w order to detect corruption. By recalculating the CRC the value originally transmitted, the receiver can det transmission errors.	ith, a block of data in and comparing it to tect some types of
Data Payload	The data, not including any control or header inform packet.	nation, carried in one
DETH	Datagram Extended Transport Header.	
DFE	Decision Feedback Equalizer.	
DGID	Destination Globally Unique Identifier.	
DCD	Duty cycle distortion.	
DDJ	Data Dependant <u>Jitter</u> .	
de/MUX	Multiplexer / Demultiplexer	
DLID	Destination Local Identifier	
Disparity	The difference between the number of ones and nu mitted in a <u>Physical Lane</u> . The running disparity is a with a value of positive or negative.	mber of zeros trans- binary parameter
Dispersion	A term used to denote pulse broadening and distort links, the two general categories of dispersion are m to the difference in the propagation velocity of the p a multimode fiber, and chromatic dispersion, due to propagation of the various spectral components of t	ion. For fiber optic nodal dispersion, due ropagation modes in the difference in he optical source.
DJ	Deterministic <u>Jitter</u>	
EBP	Please see End of Bad Packet Delimiter.	
Edge Connector	The connector on an <u>IB Module</u> that mates with a <u>B</u>	ackplane Connector.
EGP	Please see End of Good Packet Delimiter.	
EMC	Electro-Magnetic Compatibility.	
EMC Gasket	The name of the gasket used between <u>IB Modules</u> magnetic emissions.	to shield for electro-

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End of Good Packet Delim- iter	The End of Good Packet Delimiter (EGP) symbol of each packet as it is transmitted by the origination	is used to mark the end 1 ng node. 2
End of Bad Packet Delimiter	The End of Bad Packet Delimiter (EBP) symbol is of a bad packet forwarded by a switch or router new second symbol is a switch or router new second symbol is a switch or router new second symbol is a	ode. 3
Endnode	An endnode is any node that contains a <u>Channel</u> , multiple queue pairs and is permitted to establish of context, and generate messages. Also referred to <u>Adapter</u> or <u>Target Channel Adapter</u> , two specific to	Adapter and thus it has 6 connections, end to end 7 as <u>Host Channel</u> 8 ypes of endnodes. 9
Endport	A <u>Port</u> which can be a destination of <u>LID</u> -routed co same <u>Subnet</u> as the sender. All <u>Channel Adapter</u> endports of that subnet, as is Port 0 of each <u>Switc</u> ports other than Port 0 may not be endports. Whe qualification, it may be assumed to mean <i>endport</i> indicates that it is a destination of communication	mmunication within the ports on the subnet are in the subnet. Switch on <i>port</i> is used without whenever the context
ESD	Electro-Static Discharge.	16 17
Error Event	A single root cause can result in multiple error even	ents. 18
Error Propagation	A special character in the end of packet delimiter ets in which a transmission error has already bee reported.	is used to delimit pack- n detected and 21 22
Even Alignment	A special character in the code set used on the lindisparity.	nk to establish a given 23 24
Extinction Ratio	The ratio (in dB) of the average optical energy in a average optical energy in a logic zero level mease conditions at the specified baud rate.	a logic one level to the ured under modulated 28
Fabric	The collection of <u>Link</u> s, <u>Switch</u> es, and <u>Router</u> s the <u>Channel Adapter</u> s.	at connects a set of 29 30 31
Fall Time	The time interval for the falling edge of a pulse to amplitude level to its 20% amplitude level.	transition from its 80% 32
FFE	Feedforward Equalizer.	34 35
Fiber Optic Adapter	A device into which two optical connectors plug, j ments.	oining two optical seg- 37 38
Fiber Optic Cable	A jacketed optical fiber or fibers.	39
Fiber Optic Segment	An unbroken length of optical fiber with an optical end. The fiber may contain splices. A fiber optic s	connector on each egment shall not con-

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	tain a fiber optic adapter.	1
Fiber Optic Test Procedure	EIA/TIA standards developed and published by the E Association (EIA) and Telecommunications Industry under the EIA-RS-455 series of standards. Please se	Electronic Industries 2 Association (TIA) 3 ee <u>FOTP</u> . 4
Form Factor	The definition of physical packaging that specifies monectors, and placement of connectors and connecto	echanical limits, con- plates.
FOTP	Please see Fiber Optic Test Procedure.	8
Fully Managed Repeater	A Repeater which provides VPD information about it MAD operation targeted to it and allows IB-ML access mation. A repeater cannot fulfill this definition.	self by a GetInfo 10 ss to defined infor- 11
Fully Managed TCA	A TCA which provides <u>Module Information</u> about itse <u>MAD</u> operation is targeted to it and allows <u>IB-ML</u> acc ule information.	If when a GetInfo cess to defined Mod- 15
Fully Managed Unit	Any Unit which is both a <u>Baseboard Managed Unit</u> a <u>aged Unit</u> .	nd an <u>IB-ML Man-</u> 17 18
Gb/s	Giga-bits per second (10 ⁹ bits per second)	19 20
GB/s	Giga-bytes per second (10 ⁹ bytes per second)	21 22
General Services Interface	An interface providing management services (e.g., c mance, diagnostics) other than subnet management. the GSI, which may redirect requests to other QPs.	onnection, perfor- 23 <u>QP</u> 1 is reserved for 24 25
GID	Please see Globally Unique Identifier.	26 27
Globally Unique Identifier	A software-readable number that uniquely identifies nent.	a device or compo- ²⁸ 29
GMP	General Management Packet.	30 31
Graceful Hot Removal	The removal of an <u>IB Module</u> that has first been place state. V_{Bulk} may or may not be on.	ed in a quiescent 32 33 34
GSI	Please see General Services Interface.	35 36
GT/s	Giga-transfers per second (10 ⁹ transfers per second). 37
GUID	Please see Globally Unique Identifier.	38 39
HCA	Please see Host Channel Adapter.	40 41 42

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Host	One or more <u>Host Channel Adapters</u> governed by complex.	y a single memory/CPU	1 2
Host Channel Adapter	A <u>Channel Adapter</u> that supports the <u>Verbs</u> interf	ace.	3 4
Host Connector	The connector interface associated with the matir to a printed circuit board (<u>PCB</u>).	ng of a pluggable device	567
Host Node	A host node is a type of endnode consisting of or adapters governed by a single memory/CPU com ports one or more software processes, which use nication between peer processes (IPC) and I/O s support processes that provide an I/O service (e. Such a process is considered an I/O controller ar that service the same as an I/O unit enumerates	ne or more host channel nplex. A host node sup- e the subnet for commu- ervices. A host may g., console service). nd the host enumerates I/O controllers.	/ 8 10 11 12 13
Hot Add	The insertion of an IB module into a backplane th V_{Aux} present. The IB module powers up and initial sequence.	nat has both V _{Bulk} and ates a training	14 15 16 17
IBA	InfiniBand™ Architecture.		18 19
IB-ML	InfiniBand™ Management Link.	4	20
IB-ML Managed Unit	Any Unit which provides InfiniBand™ specificatio about itself through accesses from the <u>IB-ML</u> .	n defined information	21 22 23
IB-ML Management Proxy	A Unit which serves as a means to translate <u>IB-N</u> and responses) to the InfiniBand [™] Subnet link(s) more other entities.	<u>AL</u> operations (requests) on behalf of one or	24 25 26 27
IB-ML Master	A device on the <u>IB-ML</u> that initiates operations an the transfer to or from an <u>IB-ML Slave</u> device.	nd provides the clock for	28 29 30
IB-ML Slave	A device on the <u>IB-ML</u> that responds to an operative by an <u>IB-ML Master</u> . The clock used for the transless the transless that the transless the transless that the transless the transless the transless that the transless	tion that is addressed to nsfer is provided by the	31 32 33
IB Board	The <u>PCB</u> assembly inside an <u>IB Module</u> .		34 35
IB Module	A unit that conforms to any of the form factors de InfiniBand [™] specification. The IB module minima lowing: at least one <u>IB Board</u> , a <u>Carrier Module</u> , a two defined module heights and two defined mod width modules occupy two IB chassis slots. Standard Module	fined in Volume 2 of the ally consists of the fol- and a <u>Cover</u> . There are dule widths. Double	36 37 38 39 40 41 42

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	Standard Double Wide Module	1
	Tall Module	2
	Tall Double Wide Module	3
IBT	InfiniBand™ Technology	4
IHV	Independent Hardware Vendor	6
Idle Data	Data symbols transmitted to fill idle time on a link. The part of a packet and do not have delimiters symbols the end.	nese symbols are not 8 o mark their start and 9 10
In-band Management	Refers to the monitoring and control of InfiniBand™ the IB Subnet Link.	components using 12
Independent Hardware Vendor	Any vendor providing hardware. Used synonymousl ware Vendor.	y at times with Hard-
Inter IB-ML Management Proxy	A unit which serves to translate IB-ML operations fro another unit's IB-ML. (This is currently not specified Architecture but is included for completeness).	om one unit to 17 in the InfiniBand™ 18 19 20
Intersymbol Interference	The effect on a sequence of symbols in which the syby transmission through a limited bandwidth medium adjacent symbols begin to interfere with each other.	ymbols are distorted 22 n to the extent that 22 Also referred to as 22 24
Invalid Key	A Key is invalid if it numerically different from the co ciated with an IBA-defined resource. Please see Ke	rrect Key value asso- 24 <u>↓</u> . 26
I/O	Input/Output.	28
I/O Adapter	An I/O controller and TCA, usually implemented as provides access to one or more I/O devices possible ondary peripheral bus of network.	an IB Module, that 30 e attached via a sec- 32
I/O Chassis	The collection of <u>Slot</u> s and their associated power a housed within a single mechanical package.	nd cooling resources 33 34 35
I/O Controller	One of the two architectural divisions of an <u>I/O Unit</u> . (IOC) provides I/O services, while a <u>Target Channel</u> transport services.	An I/O controller 30 Adapter provides 33 38
I/O Hierarchy	An I/O unit contains one or more I/O controllers. Early vides access to one or more I/O devices or I/O ports equivalent to a PCI card that might contain up to 8 I.	ch I/O controller pro- 40 5. This is roughly 70 functions. 42

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	On the host side, the equivalent of a controller is a the I/O process that accesses an I/O controller is r driver. An I/O driver controls one or more I/O control instance of an I/O device for each I/O controller.	process. The part of eferred to as the I/O ¹ ollers, thus there is an ³
I/O Node	A type of endnode that provides I/O functions.	4 5
I/O Plate	Physical end of an <u>IB Module</u> where the I/O media for exit.	cables are mounted ⁶ ₇ 8
I/O Unit	An I/O unit (IOU) provides I/O service(s). An I/O ur more I/O Controllers attached to the fabric through nel Adapter.	nit consists of one or ⁹ a single <u>Target Chan-</u> 10 11
IOC	Please see <u>I/O Controller</u> .	12 13
IOU	Please see <u>I/O Unit</u> .	14 15
ISI	Please see Intersymbol Interference.	16
Jitter	Deviations from the ideal timing of an event which >=10kHz. Jitter is customarily subdivided into dete components.	occur at frequencies 18 rministic and random 19 20
Jitter, Deterministic	Timing distortions caused by normal circuit effects system. Deterministic jitter is often subdivided into (DCD) caused by propagation differences between a signal and data dependent jitter (DDJ) caused by limited bandwidth of the transmission system comp bol sequence.	in the transmission duty cycle distortion the two transitions of the interaction of the ponents and the sym-
Jitter, Random	Jitter due to thermal noise which may be modeled cess. The peak-to-peak value of RJ is of a probabi any specified value yields an associated <u>BER</u> .	as a Gaussian pro- listic nature and thus
Key	A construct used to limit access to one or more respassword. Security is provided by (1) limiting the a and check keys to well-trusted levels of function in ing the keys large numbers, and managing how the that each key should be unique within the system a detection of invalid key usage is raised to high level the source of the invalid key can be identified and ing keys are defined by the InfiniBand [™] Architecture Baseboard Management Key. Management Key. Queue Key.	sources, similar to a bility to generate keys the network, (2) mak- ey are changed, so at once, and (3) the els of software where dealt with. The follow- re: 32 34 34 35 36 36 36 36 36 36 36 36 36 36 36 36 36

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	Partition Key.	4
L_Key	Please see Local Route Header.	2
Lane	Please see Physical Lane	3
Lane Identifier	The second symbol of a training sequence that ide <u>Lane(s)</u> of a 1x, 4x or 12x <u>Link</u> . It is used to recogn reversal and to determine link width, etc.	ntifies the <u>Physical</u> 5 ize physical lane 6 7
LED	Light Emitting Diode.	8 9
'Let-Through' Failure	A Failure mechanism of non-isolated voltage conve primary input power of the converter, through a DC	rters which allows the path, onto the output.
LID	Please see Local Identifier.	13
Link	A full duplex transmission path between any two ne ments, such as <u>Channel Adapters</u> or <u>Switches</u> .	etwork fabric ele-
Link Heartbeat Ordered-Set	The sixteen symbol ordered-set composed of a <u>CC</u> <u>tifier</u> , three D1.2 data symbols, an OpCode symbol, PortNum symbol (only used for switch ports), and a bally Unique ID (GUID), used for ensuring link alive link round-trip latency.	M symbol, <u>Lane Iden</u> a reserved symbol, a an eight-symbol Glo- ness and determining
Link Training	Link Training is the process of establishing link syn two Link Endpoints. The Link Training State Machir tion between the Link Down and Link UP state. This is not limited to:	chronization between ne controls the transi- s process includes but
	1) Bit synchronization	20
	2) Symbol synchronization	28
	3) Width and Speed negotiation	29
	4) <u>Physical Lane</u> ordering	30
	5) <u>Physical Lane</u> polarity	32
	6) Training Sequence handshake	33
	7) Error recovery	34
Local Identifier	An address assigned to a port by the <u>Subnet Mana</u> subnet, used for directing packets within the subne Destination LIDs are present in the <u>Local Route He</u>	ger, unique within the 30 t. The Source and 37 eader. 38
Local Route Header	Routing header present in all InfiniBand™ Architect routing through switches within a subnet.	ture packets, used for 40 40 42 42

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Logic Ground	The voltage to which the logic signals (high speed referenced. This is synonymous with Signal Groun	and low speed) are 1
Longitudinal Airflow	As it pertains to the <u>IB Module</u> , longitudinal airflow across the module predominantly in the direction r plane and connector housing.	is defined as airflow 3 normal to the back- 4 5
LRH	Please see Local Route Header.	6 7
M_Key	Please see <u>Management Key</u> .	8
MAD	Please see <u>Management Datagram</u> .	1C 11
Managed Unit	A Unit which provides <u>Module Information</u> about its source.	self to an external 12
Management Datagram	Refers to the contents of an <u>Unreliable Datagram</u> munication among the <u>HCA</u> s, <u>Switch</u> es, <u>Router</u> s, a the network. InfiniBand [™] Architecture describes th of these management commands.	packet used for com- and <u>TCA</u> s to manage ne format of a number 17
Management Key	A construct that is contained in IBA Management I cate the sender by the receiver.	Datagrams to authenti- 19 20
Management Proxy	A Unit which serves as a means to allow for system tions to get from one "band" to the other (i.e. an In <u>ML</u> or IB-ML to an InfiniBand™ link)	m management opera- finiBand™ <u>Link</u> to <u>IB-</u> 23 24
MB/s	Mega-bytes per second (10 ⁶ bytes per second)	25
Message	A transfer of information between two or more Chaconsists of one or more packets.	annel Adapters that 26 27 28
MN	Please see Modal Noise.	29 30
Modal Noise	Noise in a laser based optical communication syst incomplete collection of the spatially correlated inte	em caused by the31erference pattern.32
Mode-Partition Noise	Noise in a laser based optical communication syst changing distribution of laser energy partitioning its modes (or lines) on successive pulses in the data different center wavelength for the successive puls time jitter attributable to chromatic dispersion in the	em caused by the self among the laser stream. The effect is a ses resulting in arrival e fiber.
Mode-Partition Noise k Factor	Empirically derived factor linking mode-partition no	bise to system penalty. 39
Modifiers	In a verb definition, the list of input and output obje	ects that specify how, 41

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	and on what, the verb is to be executed.		1
Module Information	Information provided to Management Software about a	n <u>IB Module</u> .	2
MPN	Please see Mode-Partition Noise.		4
MPN-k	Please see Mode-Partition Noise k Factor.		5 6
Numerical Aperture	The sine of the radiation or acceptance half angle of an tiplied by the refractive index of the material in contact entrance face.	n optical fiber, mul- with the exit or	7 8 9
O/E	Optical/Electrical.		11
OFSTP	Please see Optical Fiber System Test Practice.		12 13
OMA	Please see Optical Modulation Amplitude.		14 15
ORL	Please see Optical Return Loss.		16
Operating System Vendor	The software manufacturer of the operating system that node under discussion.	t is running on the	17 18 19
Optical Cable Plant	All passive communications elements (e.g., optical fibe splices, etc.) between a transmitter and a receiver.	r, connectors,	20 21 22
Optical Connector	An optical connector connects the optical media to the optical transmitter, to the receptacle of an optical received optic adapter.	receptacle of an /er, or to a fiber	23 24 25
Optical Connector Loss	The optical power lost between two optical connectors optic adapter.	mated in a fiber	26 27 28
Optical/Electrical Converter	Also referred to as " <u>O/E</u> Converter". A device that conv nals on a board to/from IB-compliant optical signals. It of CDR and/or de/MUX functionality, but it does not conta and is not protocol aware. The electrical signals into / of cal/Electrical Converter may be vendor-specific.	verts electrical sig- optionally contains in data buffers out of an Opti-	29 30 31 32 33
Optical Eye Opening	For a fiber optic link, the time interval across the eye, n 50% normalized eye amplitude which is error free to th	neasured at the e specified BER.	34 35 36
Optical Fiber	Any filament or fiber, made of dielectric material, that g	uides light.	37
Optical Fiber System Test Practice	Standards developed and published by the EIA/TIA uno 526 series of standards. This term is also referred to as	der the EIA/TIA- s <u>OFSTP</u> .	38 39 40 41
			42

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Optical Modulation Ampli- tude	The absolute difference between the optical power of and the optical power of a logic zero level. This term is	a logic one level abbreviated <u>OMA</u> . 1
Optical Passive Loss	The insertion loss resulting from connections (adapter attenuation attributable to the fiber cable plant.	rs or splices), and 3 4
Optical Receiver	The part of an Optical/Electrical Converter which rece nal.	ives an optical sig- 7
Optical Receiver Bandwidth	High frequency 3dB roll-off frequency of the optical re-	ceiver. 8
Optical Receiver Overload	The maximum acceptable value of the received average the receiver input to achieve the specified BER.	ge optical power at 10 11
Optical Receiver Sensitivity	The minimum acceptable value of average received sign optical test point, to achieve the specified <u>BER</u> . It takes power penalties caused by use of a transmitter with a In the case of an optical path it does not include power ated with <u>Dispersion</u> , <u>Jitter</u> , effects related to the mode source or reflections from the optical path. These effects separately in the allocation of maximum optical path p	gnal, at the defined12gnal, at the defined13es into account14worst-case output.15er penalties associal16al structure of the16cts are specified17enalty.18
Optical Receptacle	The part of the Optical Transmitter or Receiver into whe nector plugs.	nich an optical con- 20 21
Optical Return Loss	The ratio (expressed in units of dB) of optical power in ponent port or an assembly to the optical power reflect nent when that component or assembly is introduced system. This term is abbreviated <u>ORL</u> .	cident upon a com- ted by that compo- into a link or 24 25
Optical Stressed Receiver Sensitivity	Minimum receiver sensitivity required in order to perfor the data. This measure takes a transmitter with worst- adds the channel loss and the EYE losses. The stress principally used to know how the jitter affect the system low pass filter has to be in the receiver.	rm PLL locking on case output, and sed EYE is used m and how low the 30
Optical System Penalty	An optical link penalty to account for those effects othe sive loss.	er than optical pas- 32 33
Optical Transceiver	A device that converts IB-compliant electrical signals of IB-compliant optical signals. An optical transceiver may wide. In general, an Optical Transceiver will contain or <u>cal/Electrical Converters</u> , <u>CDR</u> 's, and data buffers.	on a board to/from ay be 1x, 4x or 12x ne or more <u>Opti-</u> 37
Optical Transmitter	The part of an Optical/Electrical Converter which trans	38 smits an optical sig- 39 40
Ordered Set	See <u>Control Ordered-set</u> .	41 42

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Out-of-band Management	Management messages which traverse a transport othe Band™ fabric.	er than the Infini-	1 2
P_Key	Please see Partition Key.		3
Packet	The indivisible unit of IBA data transfer and routing, con more headers, a Packet Payload, and one or two CQEs	sisting of one or	5 6
Packet Data	Data symbols transmitted as part of a Data Packet Payl Packet Payload. Packet data is delimited by start symbol and terminated by end symbols EGP and EBP.	oad or a Link Is SDP and SLP	7 8 9 10
Packet Payload	The portion of a <u>Packet</u> between (not including) any Tra and the CRCs at the end of each packet. The packet pay to 4096 bytes.	nsport header(s) /load contains up	11 12 13
PAD	The PAD symbol is transmitted only on a 12x link to main framing alignment.	intain packet	14 15 16
Partition Key	A value carried in packets and stored in <u>Channel Adapte</u> determine membership in a partition.	rs that is used to	17 18
Partition Manager	The entity that manages partition keys and membership		19 20
Passively Managed Chassis	A Passively Manage d chassis provides an InfiniBand [™] and physical <u>Slot Information</u> to every <u>IB Module</u> on the <u>IB-ML</u> .	¹ specified <u>GUID</u> Modules unique	21 22 23
РСВ	Printed Circuit Board		24 25
PD	Photodiode, used for converting optical signals to electr	ical at a receiver.	26 27
Permanent Errors	A permanent error is surfaced when a continuous and in present within an IBA component.	reversible fault is	28 29 30
Physical Lane	A set of one transmit and one receive differential pairs. I link is composed of one, four and twelve physical lanes	A 1x, 4x and 12x respectively.	31 32
Pluggable	A description for a transceiver module which may be unp or replacement.	lugged for repair	33 34 35
PM	Please see Partition Manager.		36
PN	Processor Node		37 38
Polling	A port state where the transmitter is generating a <u>Beaco</u> the receiver is waiting to respond to a Beacon Sequence	<u>n Sequence</u> and e.	39 40 41 42

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Port	Location on a <u>Channel Adapter</u> or <u>Switch</u> to which a line may be multiple ports on a single <u>Channel Adapter</u> , ea context information that must be maintained. <u>Switches</u> contain more than one port by definition.	k connects. There ch with different /switch elements
Port Type 1	An electrical interface type that utilizes the parameters InfiniBand specification (1.0, 1.0a).	of the original 5 6
Port Type 2	An electrical interface type that utilizes more stringent <u>Port Type 1</u> . Port Type 2 is currently associated with p	parameters than 7 bluggable devices. 9
Power Management	The ability for an operating system to control the powe InfiniBand [™] Architecture compliant devices (<u>Endnode</u> <u>Switch</u> es).	r consumption of 10 devices and 11 12
Power Subsystem Manage- ment	The ability to monitor and control the power supplies of sis.	a system or chas- 14
Processor Node	One or more general-purpose processors running under coherent memory model that uses a HCA to connect a one or more Ports. Additionally, a PN is capable of per- tion and configuration.	er a single cache 16 processor bus to 17 forming initializa- 18 19
Proxy Managed Repeater	A Repeater which must have a proxy in-place to respon operations but allows IB-ML access to defined VPD inf repeater boards fulfill this definition.	nd to GetInfo MAD formation. All
Proxy Managed TCA	A TCA which must have a proxy in-place to respond to operations but allows IB-ML access to defined VPD inf type of TCA in not defined by the InfiniBand [™] specification.	GetInfo MAD24formation. This25ation.26
Proxy Managed Unit	Any Unit which must have a proxy in-place because Ba tion is not accessible through its native InfiniBand™ fat	aseboard informa- pric link(s).
PSE	Protocol State Engine (Phy, Link, Frame)	30
QP	Please see <u>Queue Pair</u> .	31
Queue Pair	Consists of a Send and a Receive Work Queue. Send queues are always created as a pair and remain that w their lifetime. A Queue Pair is identified by its <u>Queue P</u>	and receive 33 vay throughout 35 <u>air Number</u> . 36
Queue Pair Number	Identifies a specific Queue Pair within a Channel Adap	ter. 37
RDETH	Reliable Datagram Extended Transport Header.	38
Receive Queue	One of the two queues associated with a <u>Queue Pair</u> . T contains <u>Work Queue Element</u> s that describe where to	The receive queue 40 place incoming 42

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	data.	
Relative intensity noise	Laser noise in dB/Hz with 12 dB optical return loss, v optical modulation amplitude.	vith respect to the
Retiming Repeater	A device which recovers and retransmits data, using eliminate jitter transfer, and hence perform a jitter res	a local oscillator to set. (<u>SKIP ordered-</u>
RIN12-OMA	Please see Relative intensity noise.	
Rise Time	The time interval for the rising edge of a pulse to tran amplitude level to its 80% amplitude level.	nsition from its 20%
RJ	Please see <u>Jitter, Random</u> .	
RMS	Root Mean Square.	
RNR Nak	Receiver Not Ready. A response signifying that the r rently able to accept the request, but may be able to	eceiver is not cur- do so in the future.
Router	A device that transports packets between IBA subne	ts.
Run Length	Maximum number of consecutive identical bits in the e.g., the pattern 0011111010 has a run length of five	transmitted signal (5).
Running Disparity	A binary parameter indicating the cumulative disparit tive) of all previously issued bits.	y (positive or nega-
SA	Please see Subnet Administration.	
SDP	Please see Start of Data Packet Delimiter.	
Send Queue	One of the two queues of a <u>Queue Pair</u> . The Send que that describe the data to be transmitted.	eue contains WQEs
Server	1) The passive entity in a connection establishment	exchange.
	2) An entity (e.g., a process) that provides services quests from clients.	in response to re-
	 The class of computers that emphasize I/O connection tralized data storage capacity to support the need remote, client computers. 	ectivity and cen- ds of other, typically
SGID	Source Globally Unique Identifier.	
Signal Ground	Please see <u>Logic Ground</u> .	

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Skew	The timing difference between <u>Physical Lanes</u> as measured crossings of the differential voltage of the <u>COM</u> training sequences <u>TS1</u> and <u>TS2</u> or in the <u>SKIP order</u>	asured using the 1 has present in the 2 ed-set. 3
SKP	The SKP symbol is transmitted as part of a SKIP orde	ered-set. 4
SKIP ordered-set	The SKIP ordered-set consists of a <u>COM</u> symbol follo symbols when initially transmitted. It may consist of a lowed by one to five SKP symbols when received.	wed by three <u>SKP</u> COM symbol fol- 8
Sleeping	A port state where the transmitter is quiescent and the to respond to a <u>Beacon Sequence</u> .	e receiver is waiting 9 10
SLID	Source Local Identifier	12
Slot	An InfiniBand [™] specified volumetric envelope with a s connector into which one of the defined IB Modules p	pecified backplane 14 lug.
Slot ID	A Slot Designation provided in Slot Information	16 17
Slot Information	Information provided by the Chassis about individual	Slots 18
SLP	Please see Start of Link Packet Delimiter.	19 20
SM	Please see <u>Subnet Manager</u> .	21 22
SMA	Please see Subnet Management Agent.	23
SMA GUID	The <u>Globally Unique Identifier</u> common to all resource of a single <u>Subnet Management Agent</u> .	24 es within the scope 25 26
SMD	See Subnet Management Data.	27 28
SMP	Please see Subnet Management Packet.	29
Solicited Event	A facility by which a message sender may cause an even at the recipient when the message is received.	ent to be generated 31 32
Spectral Width	The weighted root mean square width of the optical spectrum FOTP-127).	33 Dectrum (see 34 35
Start of Data Packet Delim- iter	The Start of Data Packet Delimiter symbol is transmitt start of a end-to-end data packet.	ed to identify the 36 37
Start of Link Packet Delim- iter	The Start of Link Packet Delimiter symbol is transmitter start of a link control packet.	ed to identify the 39 40
Stressed Receiver	In a Stressed Receiver test the worst case transmitter	eye opening is 41

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	applied to the optical receiver under test. The ey generated with a combination of coaxial cable ar ter driving a laser diode directly.	re closure typically is nd/or Bessel 4th order fil-
Stress Receiver ISI Penalty	Vertical eye closure penalty due to ISI.	4
Stressed Receiver DCD component of DJ	Horizontal eye closure caused by <u>DCD</u> measure power.	d at average optical 6 7
Subnet	A set of InfiniBand [™] Architecture <u>Port</u> s, and asso common Subnet ID and are managed by a com Subnets may be connected to each other throug	ociated links, that have a 8 mon <u>Subnet Manager</u> . 9 h routers. 10
Subnet Administration	The architectural construct that implements the in manipulating subnet management data.	nterface for querying and 12
Subnet Manager	One of several entities involved in the configurat subnet.	ion and control of the
	Active Subnet Manager: Any subnet manager control over all or part of the subnet. An active be the master subnet manager, or an alternate on the behalf of the master. This is sometimes subnet manager.	ger currently exercising ve subnet manager may e subnet manager acting referred to as the formal
	Alternate Subnet Manager: Any subnet ma the behalf of the master subnet manager, but manager.	nager that is acting on is not the master subnet
	Master Subnet Manager: The subnet mana that has the reference configuration informat	ger that is authoritative, 28 ion for the subnet.
	Standby Subnet Manager: A subnet manag cent, and not in the role of a master SM, by a Standby Isms are dormant managers.	er that is currently quies- gency of the master SM. 28
Subnet Management Agent	An entity present in all IBA <u>Channel Adapters</u> ar cesses <u>Subnet Management Packets</u> from <u>Subr</u>	nd <u>Switch</u> es that pro-30 <u>aet Manager</u> (s).
Subnet Management Data	Vital Product Data required by the Subnet Mana	ger. 32
Subnet Management Packet	The subclass of <u>Management Datagrams</u> used to SMPs travel exclusively over <u>Virtual Lane</u> 15 and sively to <u>Queue Pair Number</u> 0.	o manage the subnet. 34 d are addressed exclu- 36 36
Surprise Hot Removal	The removal of an <u>IB Module</u> from a backplane V_{Aux} present without first being placed in a quies	that has both V _{Bulk} and 38 scent state. 39
Switch	A device that routes packets from one link to and <u>net</u> , using the Destination <u>Local Identifier</u> field in	other of the same <u>Sub-</u> the Local Route Header.

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Switch Management Port	A virtual port by which a <u>Switch</u> may be managed.	1
Symbol Time	The transmit time for 1 symbol. With 8b/10b encoding, a long; thus, a symbol time is 10*UI (e.g., 4 ns for 2.5Gb/s ns for 10Gb/s signaling).	symbol is 10 bits 2 signaling, and 1 3 4
ТСА	Please see Target Channel Adapter.	5
Target Channel Adapter	A <u>Channel Adapter</u> typically used to support I/O devices required to support the <u>Verbs</u> interface. See also <u>I/O Un</u>	s. TCAs are not ⁷ <u>sit</u> . 9
Training Sequence 1	The sixteen symbol ordered-set which consists of a <u>CO</u> <u>Identifier</u> and fourteen D10.2 data symbols.	<u>M</u> symbol, <u>Lane</u> 10 11
Training Sequence 2	The sixteen symbol ordered-set which consists of a <u>CO</u> <u>Identifier</u> and fourteen D5.2 data symbols.	12 <u>M</u> symbol, <u>Lane</u> 13 14
Training Sequence 3	The sixteen symbol ordered-set which consists of a <u>CO</u> <u>Identifier</u> , six D13.2 data symbols, a bit map of the activ map requesting transmitter driver de-emphasis and/or li enabling, a symbol describing the driver de-emphasis se should be used, and five reserved symbols. TS3 is used link configuration between two peer ports on a link.	M symbol, Lane15e speeds, a bit16nk heartbeat17etting which18d for negotiating1920
Training Sequence for Test	The sixteen symbol ordered-set which is used by test eq a port link/phy state machine into one of several states transmitter and receiver compliance with physical layer	uipment to place 21 used for testing 23 specifications. 23
Transparent Retiming Re- peater	A device that recovers and retransmits data, to eliminate and hence perform a jitter reset. (<u>SKP</u> symbols are not a to <u>SKIP ordered-set</u>)	e jitter transfer, 25 added or deleted 26 27
Transport Service Type	Describes the reliability, sequencing, message size, and that will be used between the communicating Channel A	l operation types 28 Adapters. 29
	Transport service types that use the IBA transport and t Volume 2 are:	hat pertain to 31
	<u>Unreliable Datagram</u>	33
	See Volume 1 for other Transport Service Types.	35
Transverse Airflow	As it pertains to the <u>IB Module</u> , transverse airflow is defit that might predominantly enter the module parallel to the vertical module orientation this direction would be an up entrance point. Transverse airflow may be directed long the module, but the predominant entrance and/or exitpo- is in a direction parallel to the backplane.	ined as airflow backplane. In a per or lower itudinally within int for the airflow 41

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TS1	Please see Training Sequence 1.	1
TS2	Please see <u>Training Sequence 2</u> .	2
TS3	Please see Training Sequence 3.	4
тѕ-т	Please see Training Sequence for Test.	5 6
UI	Please see <u>Unit Interval</u> .	7
Unit	One or more sets of processes and/or functions attached one or more channel adapters. Please see <u>Host</u> and I/I	ed to the fabric by 9 <u>O Unit</u> . 10
Unit Interval	The time interval equivalent to one bit on the high spee active transmission speed.	d serial link at the 12
Unmanaged Chassis	An Unmanaged chassis does not implement any IB-sp Slot Information and leaves the Module IB-ML unconne	ecified <u>GUID</u> or 14 ected.
Unreliable Datagram	A <u>Transport Service Type</u> in which a <u>Queue Pair</u> may t receive single-packet messages to/from any other QP. delivery are not guaranteed, and delivered packets ma the receiver.	ransmit and 17 Ordering and 18 y be dropped by 19 20
VA_In	The Auxiliary Voltage Input pin (5V nominal) that is def Module edge connector and backplane connector.	ined on the <u>IB</u> 21 22
VB_In	The Bulk Voltage Input pins (12V nominal) that are defined and the second secon	ined on the <u>IB</u> 24 25
Verbs	An abstract description of the functionality of a <u>Host Cha</u> operating system may expose some or all of the verb f through its programming interface.	annel Adapter. An unctionality 28
Virtual Lane	A method of providing independent data streams on th link.	e same physical 30 31
Virtual Memory	The address space available to a process running in a memory management unit (MMU). The virtual address divided into pages, each consisting of 2**N bytes. The bits (the offset within a page) are left unchanged, indica within a page, and the upper bits give a (virtual) page r mapped by the MMU to a physical page address. This is the offset to give the address of a location in physical r	system with a space is usually bottom N address ating the offset number that is s recombined with nemory 32 34 34 35 36 36 37 37 38 38 38 39 38 39 39 39 39 39 39 39 39 39 39 39 39 39
Vital Product Data	Device-specific data to support management functions	- 39 40
VL	Please see <u>Virtual Lane</u> .	41 42

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VPD	Please see Vital Product Data.	1
Wake Request Event	Events that can be produced by an <u>IB Module</u> that a <u>Sleeping</u> or <u>Polling</u> state to an operation state.	desires to return from 2 3
Wander	Deviations at <10kHz from the ideal timing of an ev	vent. 5
Work Queue Element	The <u>Host Channel Adapter</u> 's internal representation The consumer does not have direct access to <u>Wor</u>	n of a <u>Work Request</u> . 7 <u>k Queue Element</u> s. 8
Work Queue Pair	See <u>Queue Pair</u> .	9
Work Request	The means by which a consumer requests the creater the	ation of a <u>Work Queue</u> 11 12
Workstation, or Client Com- puter	The class of computers that emphasize numerical mance and provide an interface to a human being.	and/or graphic perfor-
WRE	Please see <u>Wake Request Event</u>	16 17 18 20 21
		22 23 24 24 25
		26 27 28 29
		31 32 33 34
		35 36 37
		38 39 40
		41 42

CHAPTER 3: PHYSICAL LAYER OVERVIEW

3.1 INTRODUCTION

This volume defines the low level physical interface protocols, electrical and mechanical specifications for developing applications based on the InfiniBand Architecture. The InfiniBand Architecture supports a range of applications from the backplane interconnect of a single host, to a com-plex system area network consisting of multiple independent and clus-tered hosts and I/O components. In keeping with the layered nature of the InfiniBand Architecture, Figure 1 depicts the structure within the Physical Layer itself.



Figure 1 Physical Layer Structure

The basic interconnect of the InfiniBand Architecture is a link (or "physical link"), which is a full duplex transmission path between any two fabrics elements. A fabric is a collection of links, switches, repeaters and routers that connects a set of end nodes. A link physically terminates at a port.

The physical attach point to a port is either:

- 1) A Cable Connector, which is defined for use for copper cables.
- 2) A Fiber Connector, which is defined for use for optical cables.
- 3) A Backplane Connector, which is defined for accepting a specified form factor that houses a function (Channel Adapter, Switch, etc.).

For the form factors, elements of Power and Hardware Management are also specified.

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The remaining chapters in this volume provide the detailed specifications to be met in order for devices to properly function on an InfiniBand fabric.

3.2 PHYSICAL PORT

A physical "Port" is a set of signals as seen on a connector interface identified by this specification. The physical ports defined are:

- Backplane Port
- Cable Port
- Fiber Optic Port

Some physical ports contain all signals (e.g. backplane) while others contain a subset (e.g. cable and optics).

A physical port consists of up to four groups of signals which serve different purposes. These groups are:

- Signaling Group
- Hardware Management Group
- Bulk Power Group
- Auxiliary Power Group

<u>Figure 2</u> depicts a Backplane Port and the signal groupings containing a single physical link made of a number of physical lanes dependent on the link width. Similarly, <u>Figure 3</u> and <u>Figure 4</u> depict a Cable Port and a Fiber Optic Port, respectively.

See <u>Chapter 4: Port Signal Definitions</u> for further details on these port types.





Physical Layer Overview

<u>Figure 5</u> depicts a Backplane Port containing multiple independent physical links in a single physical connector; this is also referred to in this specification as being "multi-ported".



Figure 5 Backplane Port - Multiple Physical Links

A similar configuration of multiple 4x physical links in a 12x connector applies for cables also, as described in <u>Section 7.7.10, "12x to 3-4x Copper</u> <u>Cables," on page 259</u>.

3.2.2 ACTIVE CABLES

This release of this specification allows provision of power to cable connectors, to allow incorporation of active components in the cables, as described in <u>Section 7.8, "Active Cables," on page 264</u>.

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3.3 LINK ELECTRICAL SIGNALING

This specification defines the characteristics required to communicate between the output of a port of one InfiniBand node and the input of a port of another InfiniBand node using copper printed wiring and optional cabling. The only signaling rate for encoded data on the media for prior releases is 2.5 Gbits/sec which results in a data rate that can be considered to be 250 MBytes/second per physical lane, at the "SDR" (Single Data Rate) speed. Additional enhanced signaling rates defined in this release are 5.0 Gbits/sec for the "DDR" (Double Data Rate) speed, and 10.0 Gbits/sec for the "QDR" (Quad Data Rate) speed. The connections are point to point and signaling is full duplex, unidirectional.

See <u>Chapter 6: High Speed Electrical Signaling - 2.5, 5.0, & 10.0 Gb/s</u> for details of SDR (2.5Gb/s), DDR (5.0Gb/s) and QDR (10.0 Gb/s) operation. See <u>Chapter 7: Copper Cable</u> for details of the copper cable and connectors used for electrical links.

3.4 LINK OPTICAL SIGNALING

This specification defines the characteristics required to communicate between the output of a port of one InfiniBand node and the input of a port of another InfiniBand node using optical fiber. The only signaling rate for encoded data on the media for prior releases was 2.5 Gbits/sec which results in a data rate that can be considered to be 250 MBytes/second per physical lane, at the "SDR" (Single Data Rate) speed. Additional enhanced signaling rates described in this release are 5.0 Gbits/sec for the "DDR" (Double Data Rate) speed, and 10.0 Gbits/sec for the "QDR" (Quad Data Rate) speed. The connections are point to point and full duplex, unidirectional.

See <u>Chapter 8: Fiber Attachment - 2.5 Gb/s, 5.0 Gb/s, & 10 Gb/s</u> for specification details of SDR (2.5 Gb/s), DDR (5.0 Gb/s) and QDR (10 Gb/s) operation over optical fiber.

3.5 LINK PHYSICAL LAYER

The Link Physical layer provides the interface between the packet byte stream of Link Layer defined in *InfiniBand Architecture Specification, Volume 1* and the serial bit stream(s) of the physical media. The packet byte stream will be byte striped across the available physical lanes. The byte stream on each physical lane is encoded using the industry standard 8B/10B coding. In addition to encode and decode, the link physical layer includes link training and initialization logic, clock tolerance compensation logic, receive error detecting logic, and link heartbeat logic. This layer is described in <u>Chapter 5: Link/Phy Interface</u>.

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3.5.1 SPEED NEGOTIATION			1
	The previous releases of the InfiniBand Archite 2.5Gb/s signaling. However, provisions were m (speed) increases in a future version of this sp specifies negotiation for the use of SDR (2.5G QDR (10.0Gb/s) speeds.	ecture supported only ade for potential frequency pecification. This release b/s), DDR (5.0 Gb/s) and	2 3 4 5 6
	The link speed negotiation mechanism is part of Training process. This process provides for tw speed of the interface that will allow for operat quency architecturally supported that is achieve pability and interconnect signal integrity.	of the Link Initialization and to nodes to determine the tion at the maximum fre- able based on endnode ca-	7 8 9 10
3.5.2 WIDTH NEGOTIATION			12
	The link width negotiation mechanism is also p and Training. This process provides for two no of the interface that will allow for the maximum able based on endnode capability and intercor	eart of the Link Initialization des to determine the width bandwidth that is achiev- nnect.	14 15 16 17
	This specification defines three interface width	is as follows:	18 10
	 1x Electrical: 2 differential pair, 1 per direct Optical: 1 transmit/1 receive per direction 4x Electrical: 8 differential pair, 4 per direct Optical: 4 transmit / 4 receive per direct 3) 8x Electrical: 16 differential pair, 8 per direct 	ction for a total of 4 wires on for a total of 2 fibers ction for a total of 16 wires ction for a total of 8 fibers ection for a total of 32 wires	200 211 222 233 244 255 266 277 288 299
	Optical: 8 transmit / 8 receive per direc	tion for a total of 16 fibers	30
	 4) 12x Electrical: 24 differential pair, 12 per dia wires Optical: 12 transmit / 12 receive per dia bers 	rection, for a total of 48 rection for a total of 24 fi-	31 32 33 34 35 36
3.6 MODULE MECHANICAL			37
	An InfiniBand Module conforms to any of the c <u>Chapter 9: Mechanical Specification</u> . A module	lefined form factors in e consists of the following:	39 40
	a) The module carrier - the basic metal st	ructure	41 42

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	b) The module ejector & latch - a handle and la	itch	1
	 c) The module cover - easily removable cover t board(s) 	to protect the	2
	d) The board(s) which implement the module's	functionality	4
	This version of the specification defines two module dard) and two module widths. Double width modules fined chassis slots.	heights (tall and stan- s occupy two IB de-	6 7 8 9
	As double wide standard and both forms of tall mode double wide) allow for the presence of more than one a nomenclature is needed to refer to the connector p	ules (single and e physical connector, positions.	10 11 12
	Every module contains a connector positioned for the mary being defined as the left-most slot the module <u>Chapter 9: Mechanical Specification</u> , a tall module all locations: one in the lower portion and one in the upp upper in this context is when the module is in the ver consistency between standard and tall module desig (for tall) or only (for standard) location is termed "Prim "C" by convention. The upper location (for tall) is desi- tional).	he primary slot - pri- covers. As shown in low for two connector ber portion; lower and rtical orientation. For gnations, the lower hary" and designated signated "O" (for op-	13 14 15 16 17 18 19 20 21
	Architectural Note		22
	The most obvious designation for "Primary" would be is used in this specification to designate "Ports". The indicates "Primary <u>C</u> onnector".	e "P". However, "P" e designation of "C"	23 24 25 26
	For the case of a standard module, the only connect nated C1.	tor present is desig-	27 28 29
	For the case of standard wide modules, there may be positioned for the adjacent slot - adjacent being defin right of the left-most slot the module covers. The two the "C" location, are designated C1 and C2.	e a second connector ned as the slot to the o connectors, both in	30 31 32 33 34
	For the case of a tall module, as noted previously, the nector designated C1 and may optionally have a construction designated O1.	nere is a primary con- nnector in the upper	35 36 37
	For the case of a tall wide module, in addition to the I ally be connectors in the upper locations for both the positions. The two upper connectors, both in the upp designated O1 and O2.	low there may option- primary and adjacent per "O" locations are	30 39 40 41 42

Physical Layer Overview

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Within any of the physical connector locations, up to three (3) link ports is defined. The pin designation for these ports is defined in Chapter 10: Backplane Connector Specification. Figure 6 depicts these designations. "O" Locations Links Connector **O1** 02 Port 1 **P1** Р3 Port 3 Port 2 _ **P2 P1 P1 P1** "C" Locations Р3 **P**3 **P**3 C1 C2 **P2 P2 P2 P1** P1 **P1** P1 **P1 P1** P3 **P**3 **P**3 **P**3 **P**3 **P**3 **P2 P2 P2 P2 P2 P2** Standard Standard Tall Tall Wide Wide Figure 6 Module Connector Location Designation A slot is the volumetric envelope with a specified backplane connector into which one of the defined InfiniBand Modules plug. This specification provides for the enablement of 3U and 6U chassis implementations with modules oriented vertically or horizontally.

<u>Chapter 9: Mechanical Specification</u> provides details for system and chassis designers to implement slots which will accommodate the module form factor options. Only single width slots are physically defined; double width modules occupy two single width slots.

As only single width slots are defined, the connector location designation only indicate whether a connector is in the lower position (for standard and

3.7 CHASSIS SLOT MECHANICAL

tall) designated "C" or in the upper position (for tall only) designated "O". The additional designation is for the slot number.

As for the module, any of the physical connector locations present may contain up to three (3) link ports. The pin designation for these ports is defined in <u>Chapter 10: Backplane Connector Specification</u>.



3.8 POWER

Physical Layer Overview

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The combination of connector contact staggering and on-module power control circuitry allow for InfiniBand module to be hot plugged, both inserted and removed, without physical damage. Additionally, features are specified to allow for a "Graceful Removal" operation whereby software is notified of a pending removal such that appropriate actions can take place so as to not disrupt operations. LED indicators on the module indicate when an appropriate state has been achieved so that operationally safe removal can be performed.

Please see <u>Chapter 12: Power / Hot Plug</u> for details on power functionality and <u>Chapter 11: Low Speed Electrical Signaling</u> for details on the electrical parameters of the Bulk and Auxiliary Power groups.

3.9 HARDWARE MANAGEMENT

Hardware Management describes the functions that manage, control, and monitor physical components of InfiniBand modules and the Chassis in which they reside. Additionally, xCAs and switches that are packaged in some form factor other than those defined by this specification but optionally provide the hardware management functionality defined are described. The functions defined include:

- Communication mechanisms for optionally present Baseboard Manager software running on one or more nodes attached to the Infini-Band fabric,
- Communication mechanisms for an optionally present Chassis Management Entity (CME) which is local managing the physical elements of a chassis,
 23 24 25
- 3) Graceful Hot Removal mechanisms,
- 4) Standard visual indicators (LEDs) to assist the user in Hot Add and Hot Removal operations,
- 5) Module Vital Product Data (VPD) accessible to both a Baseboard Manager and a CME,
- 6) Access to module optional environmental variables.

Baseboard Manager software access these facilities using defined datagrams of the Baseboard class on the InfiniBand fabric. The Chassis Management Entity, typically with firmware, access these facilities through the InfiniBand Management Link (IB-ML) interface defined on the standard InfiniBand backplane connector to a module.

Please see <u>Chapter 13: Hardware Management</u> for details on this functionality.

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3.10 OPERATING SYSTEM (OS) POWER MANAGEMENT

Operating System Power Management defines a set of states and facilities that allow for an operating system (or a prescribed agent) to control the power consumption of InfiniBand modules and switches that provide this support. Power management of devices or media not directly attached to the InfiniBand fabric as an addressable node are outside the scope this specification.

The defined states are controlled from the InfiniBand fabric connection of the module. This includes the ability to "power down" to a state only drawing auxiliary power and "power up" from activity on the InfiniBand link. Further, in the presence of a fully operational link, states are defined to allow modules varied levels of power consumption.

Please see <u>Chapter 14: OS Power Management</u> for details on this functionality.

CHAPTER 4: PORT SIGNAL DEFINITIONS

4.1 SIGNAL NAMING CONVENTIONS

The symbol substitution and type notation used for the signal naming within this specification are defined in <u>Table 2</u> and <u>Table 3</u>.

Table 2 Symbol Substitution

Symbol Convention	Substitution
w in Signal Name	Differential pair distinction - IB Signaling Group Replaced by 'p' for positive rail of differential pair Replaced by 'n' for negative rail of differential pair
x in Signal Name	Replaced by respective board or backplane Port x may range from 1 to n where n is the number of connectors on a board edge or backplane slot
s in Signal Name	For Boards, replaced by 't' for I/O Plate connec- tion, or 'b' for backplane connection. For Backplanes, replaced by slot number. Slots are numbered from 1 to n from left to right, or bottom to top for horizontal mounting

Signal Type	Definition
InDiff	Differential input signal - IB signaling levels
OutDiff	Differential output signal - IB signaling levels
ShRet	Shield Return - Shield Ground for both the IB board and the IB backplane
Rx	Optical Receiver Input
Tx	Optical Transmitter Output
PwrU	Pull Up derived from 12V Bulk power input (VB_In)
PwrD	Pull Down to Bulk power return (VB_Ret)
APwrU	Pull Up to Auxilliary power input (VA_In)
APwrD	Pull Down to Auxiliary power return (VA_Ret)
InOut	Open Drain - Wired OR Input/Output pull-up referenced to Auxiliary power (VA_In)
In	Input - logic is powered from Auxiliary power (VA_In)

Table 3 Type Notation

	Table 3 Type Notation
Signal Type	Definition
Out	Output - derived from Auxiliary power (VA_In)
PwrIn	12 Volt Input from backplane/system power supply
PwrRet	12 Volt Return to backplane/system power supply
APwrIn	5 Volt Input from backplane/system power supply
APwrRet	5 Volt Return to backplane/system power supply
	Signal names ending with "_L" indicates the "asserted" or "true" condition is a low voltage.
SIGNAL SU	JMMARY
	This section summarizes the signals that comprise the physical ports de
	inted by this specification.

4.2.1 BACKPLANE PORT

Table 4 summarizes the signals of backplane port.

Table 4 Backplane Port Signal Summary

				·			- J		·
	Inter	face		Signal Name	Signal Type	Mate Order ^a	Break Order ^b	Number of Contacts	Description
Signa	aling (Group	- Higł	n Speed Different	ial				
12x	8x	4x	1x	IBsxlw(0)	InDiff	High Speed	High Speed	2 1 pair	IB Symbol Input Differential Signaling
				IBsxOw(0)	OutDiff	High Speed	High Speed	2 1 pair	IB Symbol Output Differential Signaling
				IBsxlw(3:1)	InDiff	High Speed	High Speed	6 3 pair	IB Symbol Input Differential Signaling
				IBsxOw(3:1)	OutDiff	High Speed	High Speed	6 3 pair	IB Symbol Output Differential Signaling
			-	IBsxlw(7:4)	InDiff	High Speed	High Speed	8 4 pair	IB Symbol Input Differential Signaling
				IBsxOw(7:4)	OutDiff	High Speed	High Speed	8 4 pair	IB Symbol Output Differential Signaling
		-		IBsxlw(11:8)	InDiff	High Speed	High Speed	8 4 pair	IB Symbol Input Differential Signaling
				IBsxOw(11:8)	OutDiff	High Speed	High Speed	8 4 pair	IB Symbol Output Differential Signaling
	-			IB_Sh_Ret	ShRet	High Speed	High Speed	24	Shield Return tied to Logic Ground
Hard	ware I	Manag	emen	t Group	•	•			
				IMxClk	InOut	3	2	1	IB Management Link Clock
				IMxDat	InOut	3	2	1	IB Management Link Data
				IMxInt_L	Out	3	2	1	IB Management Link Interrupt
				IMxPRst	InOut	4	1	1	Presence/Reset
				IMxPReq_L	Out	3	2	1	Power Request

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Interface	Signal Name	Signal Type	Mate Order ^a	Break Order ^b	Number of Contacts	Description
ulk Power Group						
	VB_In ^c	PwrIn	2	3	4	12 Volt Bulk Power Input
	VB_Ret	PwrRet	1	4	4	12 Volt Bulk Power Return
	VBxEn_L	PwrU / PwrD	4	1	1	Bulk Power Enable Not Asserted - Disable Asserted - Enable
	VBxCap	APwrU / APwrD	3	2	1	Bulk Power Capability Not Asserted - 25W; Asserted - 50W
	VBxPFW_L	In	3	2	1	Power Fail Warning
Auxilliary Power Gro	pup	•	•		•	
	VA_In ^c	APwrIn	2	3	1	5 Volt Auxiliary Power Input
	VA_Ret ^c	APwrRet	1	4	1	Logic Ground

Table 4 Backplane Port Signal Summarv

a. See the InfiniBand Architecture Specification, Volume 2, Section 12.6.1 on page 471 for detailed description b. See the InfiniBand Architecture Specification, Volume 2, Section 12.6.2 on page 473 and Section 12.6.3 on page 475 for detailed description

c. This signal may or may not be specific to a port. If it is not specific to a port (i.e, it is common among multiple ports), the "_" is used in the signal name; if it is specific to a port, then the "_" shown should be replaced with the port number in the same manner as "x" is used for other signals as described in Table 2 Symbol Substitution on page 69. For documentation clarity, the "_" is used through the remainder of this specification.

> As shown in Figure 2 Backplane Port - Single Physical Link on page 59, the Signaling Group signals make up the IB Link for the width supported by a backplane port. The ports are physically located on the defined module form factors and the backplanes into which they plug as specified in Chapter 9: Mechanical Specification. Some of the module form factors defined allow for multiple backplane ports to be present. However, one is always required.

> C4-1: In order to establish an IB Link, all modules shall have at least one backplane port containing the Signaling Group signals defined in Table 4 located at Primary Port (1) as defined by Figure 154 Module Bulk Power Ports (Logical) on page 460 and Section 12.5, "Chassis Power Rules," on page 470.

C4-2: In order to establish an IB Link, all chassis that accept InfiniBand 38 modules **shall** have at least a backplane port containing the Signaling 39 Group signals defined in Table 4 located at Primary Port (1) as defined by 40 Figure 154 Module Bulk Power Ports (Logical) on page 460 and 41 Section 12.5, "Chassis Power Rules," on page 470. 42
InfiniBand TM Architecture Release 1.2 VOLUME 2 - PHYSICAL SPECIFICATIONS	Port Signal Definitions	October, 2004 FINAL	
	Primary Port (1) requirements for the Hardware Mar found in <u>Chapter 13: Hardware Management</u> . Requi Power Group and Auxiliary Power Group are found i <u>/ Hot Plug</u> .	nagement Group are irements for the Bulk n <u>Chapter 12: Power</u>	1 2 3
	The backplane connector is specified in <u>Chapter 10</u> <u>nector Specification</u> .	: Backplane Con-	4 5 6
4.2.2 CABLE PORT		-	7 2
	<u>Table 5</u> summarizes the signals of a cable port. Cab are found in <u>Chapter 7: Copper Cable</u> .	le port requirements	9 1

	Interface Signal Name Signal Number of Description					Description	
Signa	aling G	roup -	High S	peed Differential			•
12x	8x	4x	1x	IBsxlw(0)	InDiff	2 1 pair	IB Symbol Input Differential Signaling
				IBsxOw(0)	OutDiff	2 1 pair	IB Symbol Output Differential Signaling
				IBsxlw(3:1)	InDiff	6 3 pair	IB Symbol Input Differential Signaling
				IBsxOw(3:1)	OutDiff	6 3 pair	IB Symbol Output Differential Signaling
			-	IBsxlw(7:4)	InDiff	8 4 pair	IB Symbol Input Differential Signaling
				IBsxOw(7:4)	OutDiff	8 4 pair	IB Symbol Output Differential Signaling
		-		IBsxlw(11:8)	InDiff	8 4 pair	IB Symbol Input Differential Signaling
				IBsxOw(11:8)	OutDiff	8 4 pair	IB Symbol Output Differential Signaling
				IB_Sh_Ret	ShRet		Inner Shield Return tied to Logic Ground

Table 5 Cable Port Signal Summary

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4.2.3 FIBER OPTIC PORT

<u>Table 6</u> summarizes the signals of a fiber optic port. Fiber optic port requirements are found in <u>Chapter 8: Fiber Attachment - 2.5 Gb/s, 5.0 Gb/s,</u> <u>& 10 Gb/s</u>.

Table 6 Fiber Optic Port Signal Summary

	Inter	face		Signal Name ^a	Signal Type	Number of Fibers	Description
Signa	ling G	roup - I	High Sp	peed Optical			
12x	8x	4x	1x	IBsxlp(0)	Rx	1	IB Symbol Input
				IBsxOp(0)	Тx	1	IB Symbol Output
				IBsxlp(3:1)	Rx	3	IB Symbol Input
				IBsxOp(3:1)	Тx	3	IB Symbol Output
			-	IBsxlp(7:4)	Rx	4	IB Symbol Input
				IBsxOp(7:4)	Тх	4	IB Symbol Output
				IBsxlp(11:8)	Rx	4	IB Symbol Input
				IBsxOp(11:8)	Тх	4	IB Symbol Output

a. As each lane in made of a single fiber per direction versus a differential pair per direction for electrical interfaces, the "w" portion of the signal name only will have one polarity present. By convention, the "p" (positive) polarity is used.

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4.2.4 ACTIVE CABLE PORT

<u>Table 7</u> summarizes the signals of an active cable port. Active Cable port requirements are found in <u>Section 7.8, "Active Cables," on page 264</u>.

	Inter	face		Signal Name	Signal Type	Number of Pins	Description
Signa	aling G	roup - l	High Sp	beed Differential			
12x	8x	4x	1x	IBsxlw(0)	InDiff	2 1 pair	IB Symbol Input Differential Signaling
				lBsxOw(0)	OutDiff	2 1 pair	IB Symbol Output Differential Signaling
				IBsxlw(3:1)	InDiff	6 3 pair	IB Symbol Input Differential Signaling
				IBsxOw(3:1)	OutDiff	6 3 pair	IB Symbol Output Differential Signaling
			-	lBsxlw(7:4)	InDiff	8 4 pair	IB Symbol Input Differential Signaling
				IBsxOw(7:4)	OutDiff	8 4 pair	IB Symbol Output Differential Signaling
		-		IBsxlw(11:8)	InDiff	8 4 pair	IB Symbol Input Differential Signaling
				IBsxOw(11:8)	OutDiff	8 4 pair	IB Symbol Output Differential Signaling
				IB_Sh_Ret	ShRet		Inner Shield Return tied to Logic Ground
Activ	e Cable	e Powe	r Grou	р			
12x	8x	4x		Sense-3.3V	In	1	Detection of Active Cable oper- ating at 3.3V
12x	8x	4x		Sense-12V	In	1	Detection of Active Cable oper- ating at 12V
12x	8x			Vcc	PwrIn	1	3.3Volt or 12Volt Bulk Power Input (for 4x). Return is through IB_Sh_Ret Logic Ground
12x	8x			Vcc	PwrIn	2	3.3V or 12V Bulk Power Input (for 8x & 12x). Return is through IB_Sh_Ret Logic Ground

Table 7 Active Cable Port Signal Summary

InfiniBand ^{1M} Architecture Release 1.2 Volume 2 - Physical Specifications	Port Signal Definitions	October, 2004 FINAL	
4.3 SIGNALING GROUP			1
	This group is comprised of the high speed signals Band link. The link consists of two uni-directional in as an input (or receiver) and one operating as an o are IBsxIw and IBsxOw , respectively.	s that make up the Infini- nterfaces, one operating output (or driver). These	2 3 4 5
4.3.1 HIGH SPEED ELECTRICAL			6
	Based on the width of interface supported, the nut the group varies: 1x consists of 4 conductors (1 of ferential pair out); 4x consists of 16 conductors (4 ferential pair out); 8x consists of 32 conductors (8 differential pair out); and 12x consists of 48 conduct in, 12 differential pair out).	umber of signals within differential pair in, 1 dif- differential pair in, 4 dif- differential pair in, 8 ctors (12 differential pair	7 8 9 10 11
	These signals conform to the electrical signaling a High Speed Electrical Signaling - 2.5, 5.0, & 10.0	as defined in <u>Chapter 6:</u> <u>Gb/s</u> .	13 14 15
4.3.2 HIGH SPEED OPTICAL			16
	Based on the width of interface supported, the nut the group varies: 1x consists of 2 fibers (1 in, 1 out (4 in, 4 out); 8x consists of 16 fibers (8 in, 8 out); fibers (12 in, 12 out).	umber of signals within t); 4x consists of 8 fibers and 12x consists of 24	17 18 19 20
	These signals conform to the electrical signaling a Fiber Attachment - 2.5 Gb/s, 5.0 Gb/s, & 10 Gb/s	as defined in <u>Chapter 8:</u>	21 22 23
4.4 HARDWARE MANAGEMENT	GROUP		24
	The Hardware Management Group provides a set face which supports communication between the intelligent environmental controller (hereafter calle ment Element or "CME") associated with the IB b cludes additional signals to allow for low level inte chassis backplanes and the module.	erial management inter- module and an optional ed the Chassis Manage- packplane. It also in- eraction between the	20 26 27 28 29 30 31

The InfiniBand Management Link, also known as IB-ML, is made up by the **IMxDat** and **IMxClk** signals and allow access to a number of architected facilities that provide identification, status, and control of hardware management features.

The **IMxInt_L** signal originates from the module and allows the module to provide an interrupt notification of a condition that requires backplane attention. IB-ML operations are used in response to this signal to determine the event type.

The **IMxPRst** signal is a bidirectional signal that allows the backplane to detect module presence or force module reset

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Port Signal Definitions

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The **IMxPReq_L** signal originates from the module and allows the module to request that bulk power be supplied.

These signals conform to the electrical signaling as defined in <u>Chapter 11:</u> Low Speed Electrical Signaling.

4.5 BULK POWER GROUP

The Bulk Power Group provides the majority of the IB module's operational power. In particular, the IB Signaling Group and the IB module application (i.e. Fibre Channel, Gigabit Ethernet, etc.) are powered only by the Bulk Power Group. Power is delivered at nominally 12V.

The VB_In and VB_Ret connections drive an on-board power sequencer 12 that controls power to the module's local DC-DC power converter(s). The 13 IB standard requires an on module power sequencer capable of: 14

- Sensing full insertion of the module
- Checking power required by a board and the power provided by the backplane
 17 18
- Enabling board power-up on board/backplane power compatibility 19
- Power-up override by a Chassis Management Element (CME) associated with a managed backplane (See <u>Chapter 13: Hard-</u> <u>ware Management</u> for information on Chassis Management Elements as it pertains to this specification.)

These capabilities are provided by the **VBxEn_L** and **VBxCap** pins.

The **VBxPFW_L** signal originates from the system or chassis power supply and provides an indication that the module's bulk power input may be about to go out of specified tolerance.

These signals conform to the electrical signaling as defined in Chapter 11: 29Low Speed Electrical Signaling. Further details of the usage of the Bulk30Power group can be found in Chapter 12: Power / Hot Plug of this specification.31

4.6 AUXILIARY POWER GROUP

35 The Auxiliary Power Group provides a low power, yet always available 36 supply from which certain management functions can be available in the 37 absence of Bulk Power. Functions include module information access through IB-ML (See Chapter 13: Hardware Management), beacon se-38 quence detection for in-band Power Management (See Chapter 14: OS 39 Power Management, Chapter 5: Link/Phy Interface), and detection or 40 generation of Wake Request Events (See Chapter 14: OS Power Man-41 agement). 42

Power is delivered at nominally 5V.

The VA_In connection provides the power. The return for this supply is VA_Ret which may be tied to logic ground.

These signals conform to the electrical signaling as defined in <u>Chapter 11:</u> <u>Low Speed Electrical Signaling</u>. Further details of the usage of the Auxiliary Power group can be found in <u>Chapter 12: Power / Hot Plug</u> of this specification.

4.7 ACTIVE CABLE POWER GROUP

The Active Cable Power Group provides power for active cables, which are specified in <u>Section 7.8, "Active Cables," on page 264</u>.

Two **Sense** pins are used to distinguish Active Cables operating at either 3.3V or 12V from passive (non-powered) cables, which use the same physical connector. The **VCC** pins provide power for active components in the cable, with return through signal ground. Power is delivered nominally at either 12V or 3.3V, as determined by needs of the active cable assembly.

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LINK/PHY INTERFACE CHAPTER 5:

5.1 INTRODUCTION

The Link Physical layer provides an interface between the packet byte 7 stream of upper layers and the serial bit stream(s) of the physical media. 8 The physical media may be implemented as 1, 4, 8, or 12 physical lanes. 9 The packet byte stream will be byte striped across the available physical lanes. (See Figure 8) The byte stream on each physical lane is encoded 11 using the industry standard 8B/10B coding. In addition to encode and de-12 code, the link physical layer includes link training and initialization logic, clock tolerance compensation logic, and receive error detecting logic. 13 14

The Transmit Data Flow is responsible for:

- Insertion of control sequence information
- 8B/10B encoding The Receive Data Flow is responsible for:
- Deletion of control sequence information
- Error detection and handling
- 8B/10B decoding

Figure 8 shows a block diagram of the link physical layer.





5.2 SYMBOL ENCODING (8B/10B CODING)

The InfiniBand physical lane encoding uses the industry standard 8B/10B code which is used by Fibre Channel, Gigabit Ethernet (IEEE 802.3z), FICON, and ServerNet. The 8B/10B code provides DC balance, limited run lengths, byte (symbol) synchronization, and the ability to distinguish between data characters and control characters.

C5-1: All ports shall use the industry standard 8B/10B code as defined in Section 5.2, "Symbol Encoding (8B/10B coding)," on page 80.

5.2.1 NOTATION CONVENTIONS

The 8B/10B transmission code uses letter notation for describing the bits of an un-encoded information byte and a single control variable. Each bit of the un-encoded information byte contains either a binary zero or a bi-

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nary Whe byte to as enco code	v one. A control variable, Z, has either the value D or the value K. en the control variable associated with an un-encoded information e contains the value D, the associated encoded code-group is referred s a data code-group. When the control variable associated with an un- oded information byte contains the value K, the associated encoded e-group is referred to as a special code-group.	1 2 3 4 5
The used A,B, sion a by 8B/1 Eacl vent	bit notation of A,B,C,D,E,F,G,H for an un-encoded information byte is d in the description of the 8B/10B transmission code. The bits ,C,D,E,F,G,H are translated to bits a,b,c,d,e,i,f,g,h,j of 10-bit transmis- code-groups. <u>Figure 10</u> illustrates the byte and bit nomenclature as re stream is encoded (decoded) and serialized (de-serialized). 10B code-group bit assignments are illustrated in <u>Table 8</u> and <u>Table 9</u> . h valid code-group has been given a name using the following con- tion:	6 7 8 9 10 11 12 13
1) /	/Dx.y/ for the 256 valid data code-groups, and	14
2) /	/Kx.y/ for the special control code-groups where x is the decimal value of bits EDCBA, and y is the decimal value of bits HGF.	15 16
Exa	amples of this are D10.2 or K28.5.	18
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5.2.2 VALID AND INVALID CODE-GROUPS

Table 8defines the valid data code-groups (D code-groups) of the 8B/10B30transmission code. Table 9defines the valid special code-groups (K code-
groups) of the code. The tables are used both for generating valid code-
groups (encoding) and for checking the validity of received code-groups
(decoding).30313232333334

In the tables, each byte entry has two columns that represent two codegroups which are not necessarily different. The two columns correspond to the valid code-group based on the current value of the running disparity (Current RD - or Current RD +). Running disparity is a binary parameter with either the value negative (-) or the value positive (+). See <u>Section 5.2.3, "Running disparity rules," on page 91</u> for the definition of and rules for disparity.

ıps			

Table 8 Valid Data Code Groups

Data Buta	Data Brita	Bits	Current RD -	Current RD +
Byte Name	Byte Value	HGF EDCBA	abcdei fghj	abcdei fghj
D0.0	00	000 0000	100111 0100	011000 1011
D1.0	01	000 00001	011101 0100	100010 1011
D2.0	02	000 00010	101101 0100	010010 1011
D3.0	03	000 00011	110001 1011	110001 0100
D4.0	04	000 00100	110101 0100	001010 1011
D5.0	05	000 00101	101001 1011	101001 0100
D6.0	06	000 00110	011001 1011	011001 0100
D7.0	07	000 00111	111000 1011	000111 0100
D8.0	08	000 01000	111001 0100	000110 1011
D9.0	09	000 01001	100101 1011	100101 0100
D10.0	0A	000 01010	010101 1011	010101 0100
D11.0	0B	000 01011	110100 1011	110100 0100
D12.0	0C	000 01100	001101 1011	001101 0100
D13.0	0D	000 01101	101100 1011	101100 0100
D14.0	0E	000 01110	011100 1011	011100 0100
D15.0	0F	000 01111	010111 0100	101000 1011
D16.0	10	000 10000	011011 0100	100100 1011
D17.0	11	000 10001	100011 1011	100011 0100
D18.0	12	000 10010	010011 1011	010011 0100
D19.0	13	000 10011	110010 1011	110010 0100
D20.0	14	000 10100	001011 1011	001011 0100
D21.0	15	000 10101	101010 1011	101010 0100
D22.0	16	000 10110	011010 1011	011010 0100
D23.0	17	000 10111	111010 0100	000101 1011
D24.0	18	000 11000	110011 0100	001100 1011
D25.0	19	000 11001	100110 1011	100110 0100
D26.0	1A	000 11010	010110 1011	010110 0100
D27.0	1 B	000 11011	110110 0100	001001 1011
D28.0	1C	000 11100	001110 1011	001110 0100
D29.0	1D	000 11101	101110 0100	010001 1011
D30.0	1E	000 11110	011110 0100	100001 1011

Link/Phy Interface

	Tal	ble 8 Valid Da	ta Code Grou	ps
Data Byte	Data Byte	Bits	Current RD -	Current RD +
Name	Value	HGF EDCBA	abcdei fghj	abcdei fghj
D31.0	1F	000 11111	101011 0100	010100 1011
D0.1	20	001 00000	100111 1001	011000 1001
D1.1	21	001 00001	011101 1001	100010 1001
D2.1	22	001 00010	101101 1001	010010 1001
D3.1	23	001 00011	110001 1001	110001 1001
D4.1	24	001 00100	110101 1001	001010 1001
D5.1	25	001 00101	101001 1001	101001 1001
D6.1	26	001 00110	011001 1001	011001 1001
D7.1	27	001 00111	111000 1001	000111 1001
D8.1	28	001 01000	111001 1001	000110 1001
D9.1	29	001 01001	100101 1001	100101 1001
D10.1	2A	001 01010	010101 1001	010101 1001
D11.1	2B	001 01011	110100 1001	110100 1001
D12.1	2C	001 01100	001101 1001	001101 1001
D13.1	2D	001 01101	101100 1001	101100 1001
D14.1	2E	001 01110	011100 1001	011100 1001
D15.1	2F	001 01111	010111 1001	101000 1001
D16.1	30	001 10000	011011 1001	100100 1001
D17.1	31	001 10001	100011 1001	100011 1001
D18.1	32	001 10010	010011 1001	010011 1001
D19.1	33	001 10011	110010 1001	110010 1001
D20.1	34	001 10100	001011 1001	001011 1001
D21.1	35	001 10101	101010 1001	101010 1001
D22.1	36	001 10110	011010 1001	011010 1001
D23.1	37	001 10111	111010 1001	000101 1001
D24.1	38	001 11000	110011 1001	001100 1001
D25.1	39	001 11001	100110 1001	100110 1001
D26.1	3A	001 11010	010110 1001	010110 1001
D27.1	3B	001 11011	110110 1001	001001 1001
D28.1	3C	001 11100	001110 1001	001110 1001
D29.1	3D	001 11101	101110 1001	010001 1001
D30.1	3E	001 11110	011110 1001	100001 1001
D31.1	3F	001 11111	101011 1001	010100 1001
	-			

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	Tal	ole 8 Valid Da	ta Code Grou	ps
Data	Data	Bits	Current RD -	Current RD +
Byte Name	Byte Value	HGF EDCBA	abcdei fghj	abcdei fghj
D0.2	40	010 00000	100111 0101	011000 0101
D1.2	41	010 00001	011101 0101	100010 0101
D2.2	42	010 00010	101101 0101	010010 0101
D3.2	43	010 00011	110001 0101	110001 0101
D4.2	44	010 00100	110101 0101	001010 0101
D5.2	45	010 00101	101001 0101	101001 0101
D6.2	46	010 00110	011001 0101	011001 0101
D7.2	47	010 00111	111000 0101	000111 0101
D8.2	48	010 01000	111001 0101	000110 0101
D9.2	49	010 01001	100101 0101	100101 0101
D10.2	4A	010 01010	010101 0101	010101 0101
D11.2	4B	010 01011	110100 0101	110100 0101
D12.2	4C	010 01100	001101 0101	001101 0101
D13.2	4D	010 01101	101100 0101	101100 0101
D14.2	4E	010 01110	011100 0101	011100 0101
D15.2	4F	010 01111	010111 0101	101000 0101
D16.2	50	010 10000	011011 0101	100100 0101
D17.2	51	010 10001	100011 0101	100011 0101
D18.2	52	010 10010	010011 0101	010011 0101
D19.2	53	010 10011	110010 0101	110010 0101
D20.2	54	010 10100	001011 0101	001011 0101
D21.2	55	010 10101	101010 0101	101010 0101
D22.2	56	010 10110	011010 0101	011010 0101
D23.2	57	010 10111	111010 0101	000101 0101
D24.2	58	010 11000	110011 0101	001100 0101
D25.2	59	010 11001	100110 0101	100110 0101
D26.2	5A	010 11010	010110 0101	010110 0101
D27.2	5B	010 11011	110110 0101	001001 0101
D28.2	5C	010 11100	001110 0101	001110 0101
D29.2	5D	010 11101	101110 0101	010001 0101
D30.2	5E	010 11110	011110 0101	100001 0101
D31.2	5F	010 11111	101011 0101	010100 0101
D0.3	60	011 00000	100111 0011	011000 1100

Table 8 Valid Data Code Groups				
Data Byte	Data Byte	Bits	Current RD -	Current RD +
Name	Value	HGF EDCBA	abcdei fghj	abcdei fghj
D1.3	61	011 00001	011101 0011	100010 1100
D2.3	62	011 00010	101101 0011	010010 1100
D3.3	63	011 00011	110001 1100	110001 0011
D4.3	64	011 00100	110101 0011	001010 1100
D5.3	65	011 00101	101001 1100	101001 0011
D6.3	66	011 00110	011001 1100	011001 0011
D7.3	67	011 00111	111000 1100	000111 0011
D8.3	68	011 01000	111001 0011	000110 1100
D9.3	69	011 01001	100101 1100	100101 0011
D10.3	6A	011 01010	010101 1100	010101 0011
D11.3	6B	011 01011	110100 1100	110100 0011
D12.3	6C	011 01100	001101 1100	001101 0011
D13.3	6D	011 01101	101100 1100	101100 0011
D14.3	6E	011 01110	011100 1100	011100 0011
D15.3	6F	011 01111	010111 0011	101000 1100
D16.3	70	011 10000	011011 0011	100100 1100
D17.3	71	011 10001	100011 1100	100011 0011
D18.3	72	011 10010	010011 1100	010011 0011
D19.3	73	011 10011	110010 1100	110010 0011
D20.3	74	011 10100	001011 1100	001011 0011
D21.3	75	011 10101	101010 1100	101010 0011
D22.3	76	011 10110	011010 1100	011010 0011
D23.3	77	011 10111	111010 0011	000101 1100
D24.3	78	011 11000	110011 0011	001100 1100
D25.3	79	011 11001	100110 1100	100110 0011
D26.3	7A	011 11010	010110 1100	010110 0011
D27.3	7B	011 11011	110110 0011	001001 1100
D28.3	7C	011 11100	001110 1100	001110 0011
D29.3	7D	011 11101	101110 0011	010001 1100
D30.3	7E	011 11110	011110 0011	100001 1100
D31.3	7F	011 11111	101011 0011	010100 1100
D0.4	80	100 00000	100111 0010	011000 1101
D1.4	81	100 00001	011101 0010	100010 1101

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	Tal	ole 8 Valid Da	ta Code Grou	ps
Data	Data	Bits	Current RD -	Current RD +
Byte Name	Byte Value	HGF EDCBA	abcdei fghj	abcdei fghj
D2.4	82	100 00010	101101 0010	010010 1101
D3.4	83	100 00011	110001 1101	110001 0010
D4.4	84	100 00100	110101 0010	001010 1101
D5.4	85	100 00101	101001 1101	101001 0010
D6.4	86	100 00110	011001 1101	011001 0010
D7.4	87	100 00111	111000 1101	000111 0010
D8.4	88	100 01000	111001 0010	000110 1101
D9.4	89	100 01001	100101 1101	100101 0010
D10.4	8A	100 01010	010101 1101	010101 0010
D11.4	8B	100 01011	110100 1101	110100 0010
D12.4	8C	100 01100	001101 1101	001101 0010
D13.4	8D	100 01101	101100 1101	101100 0010
D14.4	8E	100 01110	011100 1101	011100 0010
D15.4	8F	100 01111	010111 0010	101000 1101
D16.4	90	100 10000	011011 0010	100100 1101
D17.4	91	100 10001	100011 1101	100011 0010
D18.4	92	100 10010	010011 1101	010011 0010
D19.4	93	100 10011	110010 1101	110010 0010
D20.4	94	100 10100	001011 1101	001011 0010
D21.4	95	100 10101	101010 1101	101010 0010
D22.4	96	100 10110	011010 1101	011010 0010
D23.4	97	100 10111	111010 0010	000101 1101
D24.4	98	100 11000	110011 0010	001100 1101
D25.4	99	100 11001	100110 1101	100110 0010
D26.4	9A	100 11010	010110 1101	010110 0010
D27.4	9B	100 11011	110110 0010	001001 1101
D28.4	9C	100 11100	001110 1101	001110 0010
D29.4	9D	100 11101	101110 0010	010001 1101
D30.4	9E	100 11110	011110 0010	100001 1101
D31.4	9F	100 11111	101011 0010	010100 1101
D0.5	A0	101 00000	100111 1010	011000 1010
D1.5	A1	101 00001	011101 1010	100010 1010
D2.5	A2	101 00010	101101 1010	010010 1010

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Table 8 Valid Data Code Groups						
Data Byto	Data Byto	Bits	Current RD -	Current RD +	2	
Name	Value	HGF EDCBA	abcdei fghj	abcdei fghj	3	
D3.5	A3	101 00011	110001 1010	110001 1010	4 5	
D4.5	A4	101 00100	110101 1010	001010 1010	6	
D5.5	A5	101 00101	101001 1010	101001 1010	7	
D6.5	A6	101 00110	011001 1010	011001 1010	8	
D7.5	A7	101 00111	111000 1010	000111 1010	9	
D8.5	A8	101 01000	111001 1010	000110 1010	10	
D9.5	A9	101 01001	100101 1010	100101 1010	11	
D10.5	AA	101 01010	010101 1010	010101 1010	12	
D11.5	AB	101 01011	110100 1010	110100 1010	13 14	
D12.5	AC	101 01100	001101 1010	001101 1010	15	
D13.5	AD	101 01101	101100 1010	101100 1010	16	
D14.5	AE	101 01110	011100 1010	011100 1010	17	
D15.5	AF	101 01111	010111 1010	101000 1010	18	
D16.5	В0	101 10000	011011 1010	100100 1010	19	
D17.5	B1	101 10001	100011 1010	100011 1010	20	
D18.5	B2	101 10010	010011 1010	010011 1010	21	
D19.5	В3	101 10011	110010 1010	110010 1010	22	
D20.5	B4	101 10100	001011 1010	001011 1010	24	
D21.5	В5	101 10101	101010 1010	101010 1010	25	
D22.5	B6	101 10110	011010 1010	011010 1010	26	
D23.5	B7	101 10111	111010 1010	000101 1010	27	
D24.5	B8	101 11000	110011 1010	001100 1010	28	
D25.5	B9	101 11001	100110 1010	100110 1010	29	
D26.5	BA	101 11010	010110 1010	010110 1010	30	
D27.5	BB	101 11011	110110 1010	001001 1010	32	
D28.5	BC	101 11100	001110 1010	001110 1010	33	
D29.5	BD	101 11101	101110 1010	010001 1010	34	
D30.5	BE	101 11110	011110 1010	100001 1010	35	
D31.5	BF	101 11111	101011 1010	010100 1010	36	
D0.6	C0	110 00000	100111 0110	011000 0110	37	
D1.6	C1	110 00001	011101 0110	100010 0110	38	
D2.6	C2	110 00010	101101 0110	010010 0110	39 70	
D3.6	C3	110 00011	110001 0110	110001 0110	40 41	
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Table 8 Valid Data Code Groups						
Data	Data	Bits	Current RD -	Current RD +		
Byte Name	Byte Value	HGF EDCBA	abcdei fghj	abcdei fghj		
D4.6	C4	110 00100	110101 0110	001010 0110		
D5.6	C5	110 00101	101001 0110	101001 0110		
D6.6	C6	110 00110	011001 0110	011001 0110		
D7.6	C7	110 00111	111000 0110	000111 0110		
D8.6	C8	110 01000	111001 0110	000110 0110		
D9.6	C9	110 01001	100101 0110	100101 0110		
D10.6	CA	110 01010	010101 0110	010101 0110		
D11.6	CB	110 01011	110100 0110	110100 0110		
D12.6	CC	110 01100	001101 0110	001101 0110		
D13.6	CD	110 01101	101100 0110	101100 0110		
D14.6	CE	110 01110	011100 0110	011100 0110		
D15.6	CF	110 01111	010111 0110	101000 0110		
D16.6	D0	110 10000	011011 0110	100100 0110		
D17.6	D1	110 10001	100011 0110	100011 0110		
D18.6	D2	110 10010	010011 0110	010011 0110		
D19.6	D3	110 10011	110010 0110	110010 0110		
D20.6	D4	110 10100	001011 0110	001011 0110		
D21.6	D5	110 10101	101010 0110	101010 0110		
D22.6	D6	110 10110	011010 0110	011010 0110		
D23.6	D7	110 10111	111010 0110	000101 0110		
D24.6	D8	110 11000	110011 0110	001100 0110		
D25.6	D9	110 11001	100110 0110	100110 0110		
D26.6	DA	110 11010	010110 0110	010110 0110		
D27.6	DB	110 11011	110110 0110	001001 0110		
D28.6	DC	110 11100	001110 0110	001110 0110		
D29.6	DD	110 11101	101110 0110	010001 0110		
D30.6	DE	110 11110	011110 0110	100001 0110		
D31.6	DF	110 11111	101011 0110	010100 0110		
D0.7	E0	111 00000	100111 0001	011000 1110		
D1.7	E1	111 00001	011101 0001	100010 1110		
D2.7	E2	111 00010	101101 0001	010010 1110		
D3.7	E3	111 00011	110001 1110	110001 0001		
D4.7	E4	111 00100	110101 0001	001010 1110		

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Table 8 Valid Data Code Groups						
Data Byte	Data Byte	Bits	Current RD -	Current RD +		
Name	Value	HGF EDCBA	abcdei fghj	abcdei fghj		
D5.7	E5	111 00101	101001 1110	101001 0001		
D6.7	E6	111 00110	011001 1110	011001 0001		
D7.7	E7	111 00111	111000 1110	000111 0001		
D8.7	E8	111 01000	111001 0001	000110 1110		
D9.7	E9	111 01001	100101 1110	100101 0001		
D10.7	EA	111 01010	010101 1110	010101 0001		
D11.7	EB	111 01011	110100 1110	110100 1000		
D12.7	EC	111 01100	001101 1110	001101 0001		
D13.7	ED	111 01101	101100 1110	101100 1000		
D14.7	EE	111 01110	011100 1110	011100 1000		
D15.7	EF	111 01111	010111 0001	101000 1110		
D16.7	F0	111 10000	011011 0001	100100 1110		
D17.7	F1	111 10001	100011 0111	100011 0001		
D18.7	F2	111 10010	010011 0111	010011 0001		
D19.7	F3	111 10011	110010 1110	110010 0001		
D20.7	F4	111 10100	001011 0111	001011 0001		
D21.7	F5	111 10101	101010 1110	101010 0001		
D22.7	F6	111 10110	011010 1110	011010 0001		
D23.7	F7	111 10111	111010 0001	000101 1110		
D24.7	F8	111 11000	110011 0001	001100 1110		
D25.7	F9	111 11001	100110 1110	100110 0001		
D26.7	FA	111 11010	010110 1110	010110 0001		
D27.7	FB	111 11011	110110 0001	001001 1110		
D28.7	FC	111 11100	001110 1110	001110 0001		
D29.7	FD	111 11101	101110 0001	010001 1110		
D30.7	FE	111 11110	011110 0001	100001 1110		
D31.7	FF	111 11111	101011 0001	010100 1110		

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- 40
- 41 42

	Table	9 Valid Spe	cial Code Gro	oups
Data Byte	Special Byte	Bits	Current RD -	Current RD +
Name	Value	HGF EDCBA	abcdei fghj	abcdei fghj
K28.0	1C	000 11100	001111 0100	110000 1011
K28.1	3C	001 11100	<u>001111 1</u> 001	<u>110000 0</u> 110
K28.2	5C	010 11100	001111 0101	110000 1010
K28.3	7C	011 11100	001111 0011	110000 1100
K28.4	9C	100 11100	001111 0010	110000 1101
K28.5	BC	101 11100	<u>001111 1</u> 010	<u>110000 0</u> 101
K28.6	DC	110 11100	001111 0110	110000 1001
K28.7	FC	111 11100	<u>001111 1</u> 000	<u>110000 0</u> 111
K23.7	F7	111 10111	111010 1000	000101 0111
K27.7	FB	111 11011	110110 1000	001001 0111
K29.7	FD	111 11101	101110 1000	010001 0111
K30.7	FE	111 11110	011110 1000	100001 0111

Note: Underlined special code-groups contain the comma bit patterns 0011111 or 1100000. This pattern is not found in any valid Data code group or combination of Data code-groups, and is used for symbol synchronization.

Note: Codes that are not contained in the above two tables are considered invalid and **shall** generate a code violation error.

5.2.3 RUNNING DISPARITY RULES

Running disparity **shall** be calculated using the following rules. Calculations on code groups that have been transmitted will yield a transmitter's running disparity. Similarly, calculations on code groups that have been received will yield a receiver's running disparity.

Running disparity for a code-group is calculated on the basis of subblocks, where the first six bits (abcdei) (<u>Table 10</u> and <u>Table 12</u>) form one six-bit sub-block, and the second four bits (fghj) (<u>Table 11</u> and <u>Table 13</u>) form the other four-bit sub-block. Running disparity at the beginning of the six-bit sub-block is the running disparity at the end of the previous codegroup. Running disparity at the beginning of the four-bit sub-block is the running disparity at the end of the six-bit sub-block. Running disparity at the end of the code-group is the running disparity at the end of the four-bit sub-block.

Running disparity for the sub-blocks is calculated as follows:

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	1)	Running disparity at the end of any sub-block is po block contains more ones than zeros. It is also po the six-bit sub-block if the six-bit sub-block is 0007 positive at the end of the four-bit sub-block if the fo 0011;	ositive if the sub- sitive at the end of I11. It is likewise our-bit sub-block is
	2)	Running disparity at the end of any sub-block is no block contains more zeros than ones. It is also neg the six-bit sub-block if the six-bit sub-block is 1110 ative at the end of the four-bit sub-block if the four 1100;	egative if the sub- gative at the end of 000. It is also neg- -bit sub-block is
	3)	Otherwise, running disparity at the end of the sub- as at the beginning of the sub-block.	block is the same
	NC ne the 00 gir	DTE-All sub-blocks with equal numbers of zeros and utral. In order to limit the run length of 0's or 1's bet 8B/10B transmission code rules specify that sub-b 0111 or 0011 are generated only when the running uning of the sub-block is positive; thus, running disp	I ones are disparity ween sub-blocks, blocks encoded as disparity at the be- barity at the end of

these sub-blocks is also positive. Likewise, sub-blocks containing 111000 or 1100 are generated only when the running disparity at the beginning of the sub-block is negative; thus, running disparity at the end of these sub-blocks is also negative.

Table	e 10 5B/6B Co	ding for Data	Characters	23
Data Byte	unencoded Bits	Current RD -	Current RD +	25
Name	EDCBA	abcdei	abcdei	26
D0	00000	100111	011000	27
D1	00001	011101	100010	20
D2	00010	101101	010010	30
D3	00011	110001	110001	31
D4	00100	110101	001010	32
D5	00101	101001	101001	33
D6	00110	011001	011001	34
D7	00111	111000	000111	35
D8	01000	111001	000110	36
D9	01001	100101	100101	37
D10	01010	010101	010101	38
D11	01011	110100	110100	39
D12	01100	001101	001101	40
D13	01101	101100	101100	41
				42

Table 10 5B/6B Coding for Data Characters

Data Buto	unencoded Bits	Current RD -	Current RD +	2
Name	EDCBA	abcdei	abcdei	3 4
D14	01110	011100	011100	5
D15	01111	010111	101000	6
D16	10000	011011	100100	7
D17	10001	100011	100011	8
D18	10010	010011	010011	9
D19	10011	110010	110010	10
D20	10100	001011	001011	11
D21	10101	101010	101010	12
D22	10110	011010	011010	13
D23	10111	111010	000101	14
D24	11000	110011	001100	15
D25	11001	100110	100110	16
D26	11010	010110	010110	17
D27	11011	110110	001001	10
D28	11100	001110	001110	20
D29	11101	101110	010001	20
D30	11110	011110	100001	22
D31	11111	101011	010100	23

Table 11 3B/4B Coding for Data Characters

Data Byte	Unencoded Bits	Current RD -	Current RD +
Name	HGF	fghj	fghj
0	000	1011	0100
1	001	1001	1001
2	010	0101	0101
3	011	1100	0011
4	100	1101	0010
5	101	1010	1010
6	110	0110	0110
7	111	1110/0111	0001/1000

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Tabla	12	5B/6B	Codina	for	Spacial	Charactore
lable	12	3D/0D	Coung	101	Special	Characters

Data Byte	Unencoded Bits	Current RD -	Current RD +
Name	EDCBA	abcdei	abcdei
K28	11100	001111	110000
K23	10111	111010	000101
K27	11011	110110	001001
K29	11101	101110	010001
K30	11110	011110	100001

Table 13 3B/4B Coding for Special Characters

Data Bvte	Unencoded Bits	Current RD -	Current RD +
Name	HGF	fghj	fghj
0	000	1011	0100
1	001	0110	1001
2	010	1010	0101
3	011	1100	0011
4	100	1101	0010
5	101	0101	1010
6	110	1001	0110
7	111	0111	1000

5.2.4 GENERATING CODE-GROUPS

The byte to be encoded and current value of the transmitter's running disparity **shall** be used to select the code-group from its <u>Table 8</u> or <u>Table 9</u>. For each code-group transmitted, a new value of the running disparity is calculated. This new value is used as the transmitter's current running disparity for the next byte to be encoded and transmitted.

5.2.5 CHECKING THE VALIDITY OF RECEIVED CODE-GROUPS

The following rules **shall** be used to determine the validity of received code groups:

- The columns in <u>Table 8</u> and <u>Table 9</u> corresponding to the current value of the receiver's running disparity **shall** be searched for the received code-group.
- 2) If the received code-group is found in the proper column according to the current running disparity, then the code-group **shall** be con-

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		sidered valid and the associated data byte de data code-groups.	etermined (decoded) for	1
	3)	If the received code-group is not found in tha group shall be considered invalid.	t column, then the code-	2 3 4
	4)	Independent of the code-group's validity, the shall be used to calculate a new value of run value shall be used as the receiver's current next received code-group.	received code-group nning disparity. The new running disparity for the	5 6 7
	De co va dis the	etection of an invalid code-group does not nece de-group in which the invalid code-group was lid code-groups may result from a prior error w sparity of the bit stream but which did not resul e code-group in which the error occurred.	essarily indicate that the detected is in error. In- hich altered the running t in a detectable error at	0 9 1 1 1
5.3 CONTROL SYMBOLS AND C) RD	ERED-SETS		1
	Th an	e InfiniBand link uses the Control Symbols and data symbols to implement:	Ordered-Sets of control	1
	1)	packet delimiters,		1
	2)	ordered-set delimiters,		1
	3)	packet padding;		2
	4)	clock tolerance compensation.		2
	C! <u>C!</u>	5-2: This compliance statement is obsolete and 5-2.2.1:	d has been replaced by	
	C: TS de	5-2.2.1: All ports shall use the control symbols 32 ordered-sets specified in <u>Section 5.3, "Cont</u> <u>red-Sets," on page 95</u> for link/phy control and	and the SKIP, TS1, and rol Symbols and Or- communication.	
	o5 Sig fie lin	-2.2.1: All ports claiming compliance with Infini gnaling shall also use the TS3, HRTBT, and T d in <u>Section 5.3, "Control Symbols and Ordere</u> k/phy control and communication.	Band Rel. 1.2 Enhanced S-T ordered-sets speci- ed-Sets," on page 95 for	
				0 0
				3
				1
				-
				2

5.3.1 CONTROL SYMBOLS

The IB control symbols have been chosen from the 8B/10B special code-2 groups and shall be used as defined in Table 14 below. The control code-3 groups are non-data symbols that are uniquely identifiable. Of the twelve 4 available special code-groups, seven are used as control symbols, one is 5 provided for vendor specific use, and four are reserved. 6

Symbol	Encoding	Description	
СОМ	K28.5	Comma, character boundary alignment symbol.	
SDP	K27.7	Start of Data Packet Delimiter	
SLP	K28.2	Start of Link Packet Delimiter	
EGP	K29.7	End of Good Packet Delimiter	
EBP	K30.7	End of Bad Packet Delimiter	
PAD	K23.7	Packet padding symbol	
SKP	K28.0	Skip symbol	
	K28.1 K28.7	Reserved control symbols. These symbols have "comma" characteristics.	
	K28.3 K28.4	Reserved control symbols.	
	K28.6	Vendor specific control symbol.	

Table 14 Link Control Symbols

5.3.1.1 COMMA CONTROL SYMBOL (COM)

The comma control symbol (K28.5) is used by the physical lane receiver logic to identify symbol boundaries. Comma symbols are required to synchronize the receive logic when the links are being trained. The comma symbol is also used as the start of ordered-set delimiter.

5.3.1.2 START OF DATA PACKET DELIMITER (SDP)

The Start of Data Packet Delimiter symbol (K27.7) is transmitted to identify the start of a data packet. Packet formatting rules specify which physical lanes may be used by the "SDP" control symbol. (See Section 5.5 on page 111)

5.3.1.3 START OF LINK PACKET DELIMITER (SLP)

The Start of Link Packet Delimiter symbol (K28.2) is transmitted to identify the start of a link control packet. Packet formatting rules specify which physical lanes may be used by the "SLP" control symbol. (See Section 5.5 on page 111)

5.3.1.4 END OF GOOD PACKET DELIMITER (EGP)

The End of Good Packet Delimiter symbol (K29.7) is used to mark the end of each packet as it is transmitted by the originating port. Packet length

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rules restrict which physical lanes may be used to transmit the "EGP" control symbol. (See <u>Section 5.5 on page 111</u>)

5.3.1.5 END OF BAD PACKET DELIMITER (EBP)

The End of Bad Packet Delimiter symbol (K30.7) is used to mark the end of a bad packet forwarded by a switch or router node. When an error (e.g.: decode error, CRC error, etc.) is detected in a data packet it is marked bad by replacing the original "EGP" symbol with a "EBP" packet symbol. Receiving end nodes are required to recognize either EGP or EBP as the end of packet delimiter. Any data packet terminated with "EBP" symbol must be treated as if it had a CRC error.

5.3.1.6 PADDING SYMBOL (PAD)

The Padding symbol (K23.7) is used on the 8x and 12x physical link to align the physical lanes. Alignment is required at the end of any packet that does not end (EGP or EBP) in physical lane eleven (11) on a 12x physical link, or physical lane seven (7) on an 8x link. (See Section 5.5.5 on page 115 and Section 5.5.6 on page 117) Pad symbols are also used by the retiming repeaters to forward error conditions (See Section 5.10 on page 161).

5.3.1.7 SKIP SYMBOL (SKP)

The "Skip" symbol (K28.0) is used as part of the SKIP ordered-set which is used for clock tolerance compensation. (See <u>Section 5.9 on page 160</u>)

5.3.1.8 RESERVED CONTROL SYMBOLS

Four of the special code-groups listed in <u>Table 14</u> are reserved for future use by the IB standard. Special symbols K28.1, K28.3, K28.4, and K28.7 are reserved. For this version of the IB standard, the following rules apply to reserved control symbols:

- 1) The use of these control symbols **may** be defined in a future revision of this specification.
- Devices based on this version of the specification shall not transmit these control symbols.
- When a device based on this version of the specification receives a reserved control symbol a symbol coding error shall be reported. (See <u>Section 5.4.2 on page 107</u>)

5.3.1.9 VENDOR SPECIFIC CONTROL SYMBOL

The IB standard reserves a special control symbol (K28.6) for vendor specific use. The function and use of this symbol is vendor-defined and interoperability between vendors is not guaranteed. The vendor negotiation process for the use of this symbol is not defined by this specification.

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	The following rules apply to the use of the vendor bols:	-specific control sym-	1
	 The use of the vendor-specific control symbols vendor unique function. 	s may be defined for	2 3 4
	 Devices supporting the vendor-specific control transmit the symbol until both ends have nego 	symbol shall not	5
	 When an unsupported or un-negotiated vendo symbol is detected, a coding error shall be rep <u>5.4.2 on page 107</u>) 	r-specific control ported. (see <u>Section</u>	3
5.3.2 CONTROL ORDERED-SET	S	1	0
	In addition to the individual control symbols descri control ordered-sets. The ordered-sets are used fo tolerance compensation. The first symbol of all ord	bed above, IB defines r link training and clock lered-sets shall be the	12 13 14

tolerance compensation. The first symbol of all ordered-sets **shall** be the "COM" symbol, with additional symbols unique to the set type. When ordered-sets are transmitted, the ordered-set **shall** be transmitted on all physical lanes.

The defined ordered-sets are illustrated in Figure 11 below.

Γ	Ordered Set Formats - per Lane										
Byte	SKIP	TS1	TS2	TS3	HRTBT	TS-T					
0	СОМ	СОМ	СОМ	СОМ	COM	СОМ					
1	SKP	LANE ID	LANE ID	LANE ID	LANE ID	Reserved					
2	SKP	D10.2 (4Ah)	D5.2 (45h)	D13.2 (4Dh)	D1.2 (41h)	D17.2 (51h)					
3	SKP	D10.2 (4Ah)	D5.2 (45h)	D13.2 (4Dh)	D1.2 (41h)	D17.2 (51h)					
4		D10.2 (4Ah)	D5.2 (45h)	D13.2 (4Dh)	D1.2 (41h)	D17.2 (51h)					
5		D10.2 (4Ah)	D5.2 (45h)	D13.2 (4Dh)	OpCode	D17.2 (51h)					
6		D10.2 (4Ah)	D5.2 (45h)	D13.2 (4Dh)	Reserved	D17.2 (51h)					
7		D10.2 (4Ah)	D5.2 (45h)	D13.2 (4Dh)	PortNum	D17.2 (51h)					
8		D10.2 (4Ah)	D5.2 (45h)	SpeedActive	GUID[63-56]	Speeds					
9		D10.2 (4Ah)	D5.2 (45h)	HBR/ADD	GUID[55-48]	Test Opcode					
10		D10.2 (4Ah)	D5.2 (45h)	DDSV/DDS	GUID[47-40]	Reserved					
11		D10.2 (4Ah)	D5.2 (45h)	Reserved	GUID[39-32]	Reserved					
12		D10.2 (4Ah)	D5.2 (45h)	Reserved	GUID[31-24]	TxCfg[15-8]					
13		D10.2 (4Ah)	D5.2 (45h)	Reserved	GUID[23-16]	TxCfg[76-0]					
14		D10.2 (4Ah)	D5.2 (45h)	Reserved	GUID[15-8]	RxCfg[15-8]					
15		D10.2 (4Ah)	D5.2 (45h)	Reserved	GUID[7-0]	RxCfg[76-0]					

Figure 11 Ordered-Sets

5.3.2.1 SKIP ORDERED-SET (SKIP)

When transmitted the Skip sequence (SKIP) is a four symbol ordered-set comprised of a comma (COM) and three consecutive "Skip" (SKP) sym-

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bols. A SKIP ordered-set may be inserted or repeated by a retiming repeater in the link. (See <u>Section 5.10 on page 161</u>).

5.3.2.2 TRAINING SEQUENCE ONE ORDERED-SET (TS1)

Link Training Sequence One (TS1) is a sixteen symbol ordered-set composed of a comma (COM), a lane identifier data symbol, and fourteen data symbols unique to training sequence one. The lane identifiers used for TS1 and TS2 **shall** use the definitions found in <u>Table 15</u> below.

Table 15 Lane Identifiers

Lane Identifier	Hex number	8B/10B Encoding	Description
0	00	D00.0	Physical lane 0 used by 1x, 4x 8x, and 12x links
1	01	D01.0	Physical lane 1 used by 4x 8x, and 12x links
2	02	D02.0	Physical lane 2 used by 4x 8x, and 12x links
3	04	D04.0	Physical lane 3 used by 4x 8x, and 12x links
4	08	D08.0	Physical lane 4 used by 8x and 12x links
5	0F	D15.0	Physical lane 5 used by 8x and 12x links
6	10	D16.0	Physical lane 6 used by 8x and 12x links
7	17	D23.0	Physical lane 7 used by 8x and 12x links
8	18	D24.0	Physical lane 8 used by 12x links
9	1B	D27.0	Physical lane 9 used by 12x links
10	1D	D29.0	Physical lane 10 used by 12x links
11	1E	D30.0	Physical lane 11 used by 12x links

The TS1 unique data symbol is D10.2 (or 4Ah), and the 10-bit encoded value is a toggling pattern (010101 0101) for both the positive and negative running disparity.

5.3.2.3 TRAINING SEQUENCE TWO ORDERED-SET (TS2)

Link Training Sequence Two (TS2) is a sixteen symbol ordered-set composed of a comma (COM), a lane identifier data symbol, and fourteen data symbols unique to training sequence two. The lane Identifiers used by TS2 are the same as for TS1 and are defined in <u>Table 15</u> above.

The TS2 unique data symbol is D5.2 (or 45h), and the 10-bit encoded value is the same pattern (101001 0101) for both the positive and negative running disparity.

5.3.2.4 TRAINING SEQUENCE THREE ORDERED-SET (TS3)

Link Training Sequence Three (TS3) is a sixteen symbol ordered-set composed of a comma (COM), a lane identifier data symbol, six data symbols unique to training sequence three, a bit map of the active speeds, a bit map requesting transmitter de-emphasis and/or link heartbeat enabling, and a byte describing the transmitter de-emphasis setting which should be used, followed by five reserved bytes. The lane Identifiers used by TS3 are defined in <u>Table 15</u>. The format of the TS3 ordered-set is shown in <u>Figure 12 on page 100</u> below. The use of the TS3 ordered-set is described in <u>Section 5.6.4.6</u>, "Configuration States - Enhanced Signaling." on page 133.

Byte	TS3								
0	СОМ								
1	LANE ID								
2	D13.2 (4Dh)								
3	D13.2 (4Dh)								
4	D13.2 (4Dh)								
5	D13.2 (4Dh)				Bi	its			
6	D13.2 (4Dh)	7	6	5	4	3	2	1	0
7	D13.2 (4Dh)								
8	SpeedActive			Rsvd			QDR	DDR	SDR
9	HBR/ADD			Rs	vd			HBR	ADD
10	DDSV/DDS	DSSV		Rsvd			DI	DS	
11	Reserved								
12	Reserved	ADD =	Adap	otive Dri	ver De	e-emp	hasis R	leques	t
13	Reserved	HBR =	Hear	tbeat R	eques	ted			
14	Reserved	DDSV	= DD	S Valid	(1 = V)	alid, C) = DDS	S not va	alid)
15	Reserved	DDS =	Drive	er De-er	nphas	is Set	ting to ι	use	

Figure 12 TS3 Ordered-Set: Detailed Format

Symbol 8, the **SpeedActive** link speed identifier, is used to identify and advertise the speeds at which the link/phy is enabled to operate, which the link medium supports. The enumerated values used for advertising enabled link speeds are the same as described for the **SM.PortInfo(Link-SpeedEnabled)** field.

Symbol 9 indicates whether the sender is requesting adaptive driver deemphasis (ADD), and whether heartbeat is enabled and requested (HBR).

Symbol 10 indicates whether the transmitter of the TS3 is requesting a driver de-emphasis setting different from the default setting on its peer transmitter, and a 4-bit identifier for the driver de-emphasis setting requested. The transmitter driver may therefore have 17 de-emphasis settings - a default de-emphasis setting (DDSV = 0), and up to 16 adaptive driver de-emphasis settings (DDSV=1, DDS specifies a driver de-emphasis setting number). Driver de-emphasis is described in <u>Section 6.3.2</u>, <u>"Equalization." on page 143</u>.

Symbols 11 to 15 are Reserved. They are transmitted as D00.0, and valid Dxx.y symbols are ignored at the receiver.

The TS3 unique data symbol is D13.2 (or 4Dh), and the 10-bit encoded value is the same pattern (101001 0101) for both the positive and negative running disparity.

5.3.2.5 LINK HEARTBEAT ORDERED-SET (HRTBT)

Link Heartbeat ordered-set (HRTBT) is a sixteen symbol ordered-set composed of a common (COM), a lane identifier data symbol, three data symbols unique to the Link Heartbeat ordered-set, a 1-symbol OpCode, a 1-symbol Reserved field, a 1-symbol PortNum value (only used for switch ports), and an eight-symbol Globally Unique ID (GUID). The format of the HRTBT ordered-set is shown in Figure 13 on page 101 below. The use of the HRTBT ordered-set is described in Section 5.11.1, "Operation of Link Heartbeats," on page 167



Figure 13 HRTBT Ordered-Set: Detailed Format

Symbol 5 is an OpCode, which signifies whether the Heartbeat is a Send Heartbeat (SND, OpCode = 5Dh), or an acknowledgement (ACK, OpCode = ACh).

Symbol 7 and Symbols 8-15 indicates the port number and the GUID or the port that the SND heartbeat came from, and which port the ACK is going back to, and Symbols

The Link Heartbeat unique data symbol is D1.2 (or 41h), and the 10-bit encoded value is either 011101 0101 for negative running disparity, or 100010 0101 for positive running disparity.

5.3.2.6 TRAINING SEQUENCE FOR TEST ORDERED-SET (TS-T)

The Training Sequence for Test is a sixteen symbol ordered-set composed of a comma (COM), a reserved symbol replacing the usual Lan ID symbol, six data symbols unique to Training Sequence for Test, a bit map of the speed at which test phase is to occur (SDR, DDR, or QDR), a symbol indicating which of several defined test modes to use, and 2 16bit transmitter configuration and receiver configuration fields, which define, in a vendor-dependent way, how the transmitter and receiver are configured during the test. The lane Identifiers used by TS-T are defined in <u>Table 15</u>. The format of the TS-T ordered-set is shown in <u>Figure 14</u> below. The use of the TS-T ordered-set is described in <u>Section 5.12</u>, <u>"Physical Laver Compliance Testing," on page 169</u>.



Figure 14 TS-T Ordered-Set: Detailed Format

The Training Sequence for Test (TS-T) is only generated by test equipment. There is no need for an InfiniBand device to be able to generate this ordered-set - only the need to recognize it and behave appropriately when 8 contiguous and valid copies of TS-T arrive at the receiver port on one or more lanes.

Symbol 8 of a TS-T, the link speed identifier, is used to identify the speed at which the test equipment requests the IB device to operate. At least one bit of this bit map must be asserted to 1. If multiple bits are asserted, the test will be conducted at the highest *LinkSpeedEnabled* speed. This allows testing at the highest enabled speed by simply asserting all bits in this symbol.

Symbol 9 of a TS-T allows the test equipment to determine which testing mode the port will be placed in. The following values are defined.

0: SKIP-less Idle Data

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	Each transmitter lane transmits a pseud data symbols, generated by the 11th or with no insertion of SKIP ordered-sets.	o-random sequence of der LFSR = $X^{11} + X^9 + 1$
	1: SKIP-less back-to-back TS1s	
	Each transmitter lane transmits an unb dered-sets, with no insertion of SKIP or	roken string of TS1 or- rdered-sets.
	2: Receiver test.	
	On each lane, the transmitter sends an i of the data received on the correspond	ndication of the validity ing receiver lane.
	VALID DATA: For each received symbol codes to a valid 8b/10b code point with the corresponding transmitter lane trans 0101) character.	bl on a lane which de- good running disparity, smits a D10.2 (010101
	LOGICAL ERROR: For each received s decodes with a logical error (e.g., bit err error), the corresponding transmitter la D00.0 pair of symbols.	symbol on a lane which or, or running disparity ne transmits a K28.5
	LOSS OF SIGNAL: For each received s indicates an inadequate signal (e.g., ina all 0s, all 1s, or noise), the correspondi transmits a K28.5 D01.0 pair of symbol	symbol on a lane which adequate signal swing, ng transmitter lane Is.
	3-255: Optional Vendor-dependent opcode modes.	s to allow other testing
	Symbol 10 and Symbol 11 of a TS-T are reserved. as D00.0 and valid Dxx.y symbols are ignored at t	. They are transmitted he receiver.
	Symbols 12 and 13 allow the test equipment to op transmitter in one of 65,536 vendor-dependent sta and 15 allow the test equipment to configure the re- vendor-dependent states. The values 0000h are id "default" operation, so that test equipment can be and correct operation when these fields are set to are optional and vendor-dependent. Typically only these states will be valid and will provide specific to	tionally configure the ates, and symbols 14 ceiver in one of 65,536 lentified for "normal" or expected to get good 0. Values other than 0 a very small subset of unique behaviors.
	The TS-T unique data symbol is D17.2 (or 51h), and value is the pattern (100011 0101) for both the posining disparity.	nd the 10-bit encoded sitive and negative run-
5.3.3 PACKET LOGICAL INTERF	ACES	
	This section describes the logical interfaces of the section is not intended to describe an actual imple but rather to explain the logical interface between p	Link/Phy layer. This mentation of a device protocol layers. This in-

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	terface may or may not be implemented as an internal o interface.	r external device	1
	The logical interface section defines three logical interfa	ices:	3
	1) Data/Status interface to the upper layer, Link to Link	/Phy,	4
	2) Interface to the lower layer, Link/Phy to Physical;		6
	3) Control and Status interface to the Link/Phy layer.		/ 8
5.3.3.1 LOGICAL LINK TO LINK/P	HY DATA INTERFACE		9
	The logical Link to Link/Phy data interface is defined in the chitecture Specification, Volume 1, Chapter 6: Physical	the InfiniBand Ar- Layer Interface.	10 11
5.3.3.2 LOGICAL LINK/PHY TO PH	IYSICAL INTERFACE		12
	The Link/Phy to Physical interface consists of the following	na loaical sianals:	14
			15
	1) <u>PhyTxData[11:0]</u> - Transmit bit stream(s) 1x, 4x, 8x	or 12x.	16
	2) <u>PhyRxData[11:0]</u> - Receive bit stream(s) 1x, 4x, 8x of	or 12x.	17
5.3.3.3 LINK/PHY CONTROL AND	STATUS INTERFACE		19
	The Link/Phy control and status interface consists of the signals:	following logical	20 21
	1) PowerOnReset - Port Power on Reset input,		22
	2) LinkPhyReset - Link Physical Reset control input,		23
	3) LinkPhyRecover - Link Physical Recovery control in	put;	25
	4) LinkPhyStat - Link Physical State (up or down) statu	s output.	26
5.4 MANAGEMENT DATAGRAM	CONTROL AND STATUS INTERFACE		27
	The Management Datagram Control and Status interfact into two sub-sections: Control Inputs, and Status Output	e is subdivided ts.	29 30 31
	Implementation Note		32 33
	Designers should not rely on the absence or character tures or commands marked "reserved" or "undefined". Band SM Trade Association reserves these for future de	istics of any fea- The Infini- efinition.	34 35 36
	C5-3: This compliance statement is obsolete and has be <u>C5-3.2.1:</u> .	een replaced by	37 38 39
	C5-3.2.1: All ports shall implement the control and state interface defined by <u>Section 5.4, "Management Datagra</u>	us management m Control and	40 41 42

	Status Interface." on page 104, excluding DDR/QDR interoperability, 8x interoperability, PhyTest compliance testing, and LinkRoundTripLatency.	1 2
	o5-3.2.1: All ports claiming compliance with InfiniBand Rel. 1.2 Enhanced Signaling shall implement the control and status management interface defined by <u>Section 5.4</u> , " <u>Management Datagram Control and Status Interface</u> ," on page 104, including DDR/QDR interoperability, 8x interoperability, PhyTest compliance testing, and LinkRoundTripLatency.	3 4 5 6 7
5.4.1 CONTROL INPUTS (MAD	SET)	8 9
	Specific implementations may provide control information via proprietary mechanisms.	10 11 12
	Multiple commands may be sent in the same <i>SM.PortInfo(component)</i> Management Datagram. Simultaneous commands, one of which changes the state of the Port Training State machine, shall set the other associated state variable(s) before the port training state change occurs.	13 14 15 16
	The Control Input interface consists of the following Management Data- gram to variable or logical signal mappings:	17 18 19
	 A Management Datagram SM.PortInfo(PortPhysicalState) set shall cause the Port Training State machine to transition state based on the following enumerated values: 	20 21 22
	0: No State Change (NOP)	23
	1: Sleeping	24
	2: Polling	26
	3: Disabled	27
	4-15: Reserved (Janored)	28
	Poter to Section 5.4.2 for fields returned by the MAD get operation	29
	The default value following power on shall be set to Polling.	31
	2) A Management Datagram <i>SM.PortInfo(LinkDownDefaultState)</i> set	32
	shall set the logical signal <u>LinkDownDefaultState</u> based on the following enumerated values:	33 34
	0: No State Change (NOP)	35
	1: Sleeping	36
	2: Polling	37
	3-15: Reserved (Japored)	39
	Poter to Section 5.4.2 for fields returned by the MAD set exercises	40
	The default value following power on shall be set to Polling.	41

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3	A Management Datagram SM.PortInfo shall set the LinkWidthEnabled variable upon the variable until the Port Training the Configuration state. The port shall link to width(s) based on the following er	(LinkWidthEnabled) set e. No action shall be taken State machine transitions to only attempt to configure the numerated values:
	0: No State Change (NOP)	5
	1: 1x	6
	2: 4x	8
	3: 1x or 4x	9
	4: 8x	1
	5: 1x or 8x	1
	6: 4x or 8x	1
	7: 1x or 4x or 8x	1
	8: 12x	1
	9: 1x or 12x	1
	10: 4x or 12x	1
	11: 1x, 4x or 12x	1
	12:8x or 12x	2
	13: 1x or 8x or 12x	2
	14: 4x or 8x or 12x	2
	15: 1x or 4x or 8x or 12x	2
	16-254: Reserved (Ignored)	2
	255: Set to <i>LinkWidthSupported</i> va	lue 2
	Refer to <u>Section 5.4.2</u> for fields returned The default value following power on sha	by the MAD get operation. all be set to <i>LinkWidthSup</i> -
Λ	A Monogoment Detegrom SM Bertinfo/	inkenandEnabled) act
4	shall set the LinkSpeedEnabled variab	le. No action shall be taken
	upon the variable until the Port Training	State machine transitions to ³
	link to a speed based on the following er	numerated values: 3
	0: No State Change (NOP)	3
	1: 2.5 Gb/s	3
	3: 2.5 or 5.0 Gb/s (SDR or DDR)	3
	5: 2.5 or 10.0 Gb/s (SDR or QDR)	4
	7: 2.5 or 5.0 or 10.0 Gb/s (SDR or DI	DR or QDR) 4

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2, 4, 6, 8-14: Reserved (ignored)

15: Set to *LinkSpeedSupported* value

Note that the SDR speed (2.5 Gb/s) must always be enabled, since link initialization occurs at this speed. Refer to <u>Section 5.4.2</u> for fields returned by the MAD get operation. The default value following power on **shall** be set to *LinkSpeedSupported.*

Implementation Note

MAD responders are required to respond to a **SM.PortInfo Set()** command with a **GetResp()** MAD. (*InfiniBand Architecture Specification*, <u>Volume 1, Section 13.4.6.1</u>) The **SM.PortInfo(PortPhysicalState)** set will cause the port training state machine to down the port when implementing the command. When this MAD is received on the port affected by the port state change command, the **GetResp()** MAD may not be transmitted before the port responds to the command. When a command is issued in this manner, the requestor should not expect a **Get-Resp()** MAD. Command execution can be verified by observing the state change at the other end of the link.

Implementation Note

Subnet Manager software designers should be aware that when a powered port is commanded to the Disabled State, the port will no longer respond to received packets or beacons. The port can only be re-enabled by using an alternate path, a second port on the same node, or some out-of-band connection. If there is no alternate path, the port must be reset to recover normal operation. For example, a single port IB device without an out-of-band management path would have to be physically reset to exit the Disable State.

5.4.2 STATUS OUTPUTS (MAD GET)

Specific implementations may provide status via proprietary mechanisms. 34

The Status Output interface consists of the following Management Datagram to variable or logical signal mappings: 37

- A Management Datagram *SM.PortInfo(PortPhysicalState)* get shall return the Port Training State machines current state as one of the following enumerated values:
 38 39 40
 - 1: Sleeping

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		2: Polling		_
		3: Disabled		2
		4: Configuration		3
		5: LinkUp		4
		6: Recovery		5
		7: Phy Test		7
		0, 8-15: Reserved		8
:	2)	A Management Datagram <i>SM.PortInfo(LinkD</i> shall return the <u>LinkDownDefaultState</u> current following enumerated values:	ownDefaultState) get value based on the	9 10 11
		1: Sleeping		12
		2: Polling		14
		0, 3-15: Reserved		15
:	3)	A Management Datagram SM.PortInfo(LinkW shall return the previously written LinkWidthE on the following enumerated values:	<i>(idthEnabled)</i> get Inabled value based	16 17 18
		1: 1x		19
		2: 4x		20
		3: 1x or 4x		22
		4: 8x		23
		5: 1x or 8x		24
		6: 4x or 8x		26
		7: 1x or 4x or 8x		27
		8: 12x		28
		9: 1x or 12x		29
		10: 4x or 12x		31
		11: 1x, 4x or 12x		32
		12: 8x or 12x		33
		13: 1x or 8x or 12x		34 35
		14: 4x or 8x or 12x		36
		15: 1x or 4x or 8x or 12x		37
		0, 16-255: Reserved		38
	4)	A Management Datagram <i>SM.PortInfo(LinkSj</i> shall return the previously written <i>LinkSpeedE</i> on the following enumerated values:	peedEnabled) get Enabled value based	39 40 41
		J		42
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---	----	--	--	----------------
		1: 2.5 Gb/s		_
		3: 2.5 or 5.0 Gb/s (SDR or DDR)		2
		5: 2.5 or 10.0 Gb/s (SDR or QDR)		3
		7: 2.5 or 5.0 or 10.0 Gb/s (SDR or DDR or QDR)	4
		0. 2. 4. 8-15: Reserved	,	5
	5)	A Management Datagram <i>SM.PortInfo(LinkWidth</i> shall return the supported width(s) based on the fol merated values:	Supported) get lowing enu-	6 7 8
		1: 1x		9
		3: 1x or 4x		11
		7: 1x 4x or 8x		12
		11: 1x, 4x, or 12x (not valid for products support hanced Signaling)	ing Rel. 1.2 En-	13 14 16
		15: 1x, 4x, 8x or 12x		16
		0, 2, 4-6, 8-10,12-14, 16-255: Reserved		17
	6)	A Management Datagram <i>SM.PortInfo(LinkWidth,</i> return the Port Training State machines currently co based on the following enumerated values:	Active) get shall Infigured width	18 19 20
		1: 1x		21
		2: 4x		24
		4: 8x		24
		8: 12x		25
		0, 3, 5-7, 9-255: Reserved		26
	7)	A Management Datagram <i>SM.PortInfo(LinkSpeed</i> shall return the supported speeds based on the foll merated values:	S upported) get owing enu-	21 28 29
		1: 2.5 Gb/s		31
		3: 2.5 or 5.0 Gb/s (SDR or DDR)		32
		5: 2.50 or 10.0 Gb/s (SDR or QDR)		33
		7: 2.5 or 5.0 or 10.0 Gb/s (SDR or DDR or QDR)	34
		0, 2, 4, 6, 8-15; Reserved	/	35
	8)	A Management Datagram <i>SM.PortInfo(LinkSpeed</i> return the Port Training State machines currently co based on the following enumerated values:	Active) get shall infigured speed	37 38 39
		1: 2.5 Gb/s		4(
		2: 5.0 Gb/s (DDR)		41
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4: 10 Gb/s (QDR)

0, 3, 5-15: Reserved

9) A Management Datagram SM.PortInfo(LinkRoundTripLatency) get shall return the minimum measured round trip link latency from the port to the connected port on the opposite side of the link. The Link-RoundTripLatency is a 32-bit value representing the minimum measured time for a bit in Link Heartbeat ordered-set to traverse the link in both directions, and can take on the following values:

0xFFFF_FFFF: Link round-trip latency not yet measured, following reset on entry to LinkDownDefaultState.

Others (0x0000_0000 to 0xFFFF_FFE): Link round-trip latency between when a SND HEARTBEAT is transmitted and it's corresponding ACK HEARTBEAT is returned, reported in 4 nanosecond intervals.

Measurement of LinkRoundTripLatency using HRTBT ordered-sets is described in Section 5.11.1, "Operation of Link Heartbeats," on page 167.

5.4.3 PORT PERFORMANCE COUNTERS

Each port implements the following performance counters. These counter 21 are accessed using the Performance Management command defined in 22 InfiniBand Architecture Specification, Volume 1, Section 15.2. The Link 23 Physical Performance Counters shall implement both the get and set per-24 formance management methods. These counters do not rollover but shall stop at there maximum count. At set, operation is required to re-enable 25 error counting. Specific implementations may provide performance infor-26 mation via proprietary mechanisms. The Performance Management inter-27 face shall consist of the following performance counters: 28

- 1) A Management Datagram *Perf.PortCounters(SymbolError-*Counter) read shall return the current value of the 16-bit counter SymbolErrorCounter. This counter is incremented each time an error is detected on one or more lanes. (See Section 5.7.2, "Minor Link Physical Errors Events," on page 157)
- 34 2) A Management Datagram Perf.PortCounters(LinkErrorRecovery-Counter) read shall return the current value of the 8-bit counter 35 LinkErrorRecoveryCounter. This counter is incremented each time 36 the Port Training State machine successfully completes the link error 37 recovery process. (See Section 5.6.4.8, "Link Error Recovery States," 38 on page 144) 39
- 3) A Management Datagram Perf.PortCounters(LinkDowned-Counter) read shall return the current value of the 8-bit counter 41 LinkDownedCounter. This counter is incremented each time the

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	Port Training State machine fails the link error downs the link. (See <u>Section 5.6.4.8, "Link Er</u> <u>on page 144</u>). This counter is also incremente Heartbeat error returns the Link Training State DownDefaultState. (See <u>Section 5.11.2, "Hea</u>	r recovery process and ror Recovery States," ed each time a Link a Machine to the Link- rtbeat Error Handling," 1 2 2 3 4 7 7 7 7 7 7 7 7 7
	<u>on page 168</u>).	5
5.5 PACKET FORMATS FOR SI	NGLE AND MULTI LANE SUPPORT	7
	This section describes the distribution and transla packet byte stream to the physical lanes.	ation of the Link Layer 9 10 11
	In addition to the control ordered-sets defined ear used as the payload of link and data packets and data symbols are framed by start of packet symbol end of packet symbols EGP and EBP. Idle data sy link or data packet and are not framed by packet	rlier, data symbols are 12 as link idle data. Packet 13 ols SDP and SLP and 14 ymbols are not part of a 15 delimiters symbols. 16
5.5.1 LINK PACKET ORDERING		18
	The upper layers of the Protocol provide a stream in the stream are composed of:	of packets. The packet 20
	1) A Local Routing Header and other optional he	eaders. 23
	2) A packet payload, type dependent.	24 25
	3) A Invariant CRC, type dependent.	26
	4) And a Variant CRC.	27 28
	The combined length of packet header(s), payload a multiple of four bytes. Two bytes of a Variant CI limiter and packet end delimiter ensure that all pac bytes in length. See <i>InfiniBand Architecture Spec</i> <u>Chapters 6 & 7</u> for complete details of internal pa Link/Physical layer forwards these packets in the quired, the Link/Physical layer will insert SKIP or packets. (See <u>Section 5.9.2</u>) An example of pack is depicted below in <u>Figure 15</u> . When there is no p sets set to transmit the Link/Physical layer will fill pseudo-random sequence of data symbols (idle of	I, and Invariant CRC are29RC plus packet start de-30ket are a multiple of four31 <i>ification, Volume 1,</i> 32cket formatting. The32order received. As re-32dered-sets between35et ordering on a 4x link36backet or SKIP ordered-36the link Idle with a36data).36
	C5-4: All ports shall implement link packet orderi Section 5.5.1, "Link Packet Ordering," on page 11	ng as defined by 41 11. 42

	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	2 3 4 5 6 7 8 9 10 11 12 13 14 15
	Data	16
	Figure 15 Packet Ordering Example	18
5.5.1.1 PACKET ORDERING RULES		19
1)	Packets contain un-interruptible packet data content and delimiters. Ordered-sets and control symbols shall not be inserted into a packet's data content except as described in rule 4 below.	20 21 22
2)	Packets received from the upper layers shall be transmitted in the order received.	23 24 25
3)	Scheduled SKIP ordered-sets shall only be inserted between packets for clock tolerance compensation.	26 27
4)	To initiate the error recovery process, TS1 ordered-sets shall be in- serted at any symbol boundary, possibly interrupting the current packet.	28 29 30
5)	When the link is idle (no packets or control ordered-sets to transmit), a pseudo-random sequence of data symbols (idle data) shall be transmitted on all lanes.	31 32 33
6)	The link idle pseudo-random data sequence shall be generated by the 11th order LFSR = $X^{11} + X^9 + 1$.	34 35 36
7)	Each lane may start the link idle pseudo-random data pattern at an arbitrary valid value. No lane-to-lane dependence is specified for the link idle pseudo-random data pattern.	37 38 39
8)	Idle data shall be terminated at any time there is a packet or control ordered-set to transmit.	40 41 42

5.5.2 PACKET FORMATS

	Pao of t	ckets including start and end delimiters are formed by the upper layers he protocol. This stream of packets is striped across the available	1 2 3
	physical lane(s) (1x, 4x, 8x, or 12x).		
	C5 Sec	-5: All ports shall implement packet formatting as defined by ction 5.5.2, "Packet Formats," on page 113.	5 6 7
5.5.2.1 PACKET FORMATTING RUL	.ES		8
	1)	Total length of data packets including packet delimiter symbols shall be integer multiples of four symbols.	9 10 11
	2)	Data packets shall have SDP symbol as the first symbol of the packet.	12 13
	3)	The link packets shall be eight symbols long including the packet de- limiter symbols.	14 15
	4)	Link packets shall have a SLP symbol as the first symbol of the packet.	16 17
:	5)	When transmitted, all packets shall be terminated by an EGP or EBP symbol.	18 19
	6)	There are no per-lane even or odd alignment restrictions. Packets are not required to start with even or odd alignments. Comma symbols do not force even alignment.	20 21 22
	7)	The starting running disparity of packet delimiters and ordered-sets is not specified; a packet or ordered-set may start with positive or negative disparity. The disparity of all symbols shall comply with 8B/10B encoding rules. (See <u>Section 5.2.3</u>)	23 24 25 26
5.5.3 1x PACKET FORMAT			27 28
	The syn	e 1x link is composed of a single physical lane. The combined packet nbol stream is serialized into a single stream of symbols. The SKIP or-	29 30
	der	ed-set is inserted between packets as needed for clock tolerance com-	31
	and	d idle data) is encoded using the 8B/10B code defined in <u>Section 5.2</u>	33
	abo	ove. A 1x symbol stream containing data packets, link packet, idle data, I SKIP ordered-sets is illustrated in Figure 16 below.	34
			35
	C5	-6: All 1x ports and 4x and 12x ports when configured as a 1x port shall blement packet formatting as defined by Section 5.5.3, "1x Packet	37
	For	mat," on page 113	38
	o5-	6.2.1: All 8x ports when configured as a 1x port shall implement	39
	pac pac	ket formatting as defined by <u>Section 5.5.3, "1x Packet Format," on</u>	40 41 42



5.5.4 4X PACKET FORMAT

The 4x link is composed of four physical lanes (0 through 3). The comstriped across physical lanes 0 through 3. In the 4x configuration, the start packet delimiters will always be transmitted on physical lane 0 and the end SKIP ordered-sets are needed for clock tolerance compensation, they are inserted between packets simultaneously on all physical lanes. The four symbol streams composed of packets, SKIP ordered-sets, and idle data are individually encoded using the 8B/10B code defined in Section 5.2 above. The 4x symbol streams containing data packets, link packets, and SKIP ordered-sets is illustrated in Figure 17 below.

C5-7: All 4x ports and 12x ports when configured as a 4x port shall implement packet formatting as defined by Section 5.5.4, "4x Packet Format," on page 114.

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	o5-7.2.1: All 8x ports when configured as a 4x port shall imp packet formatting as defined by <u>Section 5.5.4, "4x Packet Fopage 114</u> .	lement rmat," on
	Physical Lanes #0 #1 #2 #3 Data Packet Data Packet	
	Data Packet Figure 17 4x Packet Formats	
5.5.4.1 4x PACKET FORMATTING I	Rules	
	1) The start of packet delimiters (SDP & SLP) shall be trans lane zero (0) only.	mitted in
	2) The end of packet delimiters (EGP & EBP) shall be trans lane three (3) only.	mitted in
	3) SKIP ordered-sets shall be transmitted on all (4) lanes si neously.	multa-
	4) When the idle data is placed on the link, the idle data patter inserted on all four(4) lanes simultaneously.	ern shall be
	5) The pseudo-random idle data for each lane should start point in the sequence.	a different
5.5.5 8x Packet Format		
	The 8x link is composed of eight physical lanes (0 through 7) bined data and link packet symbol stream (control and data) striped across physical lanes 0 through 7. In the 8x configurat packet delimiters will always be transmitted on physical lane end packet delimiters will always be transmitted on physical I The link will be padded (PAD control symbols) as necessary the start of packet alignment rule. When SKIP ordered-sets a	. The com- are byte ion the start 0, and the ane 3 or 7. to maintain are needed

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for clock tolerance compensation, they are inserted between packets simultaneously on all physical lanes. The eight symbol streams composed of packets, SKIP ordered-sets, and idle data are individually encoded using the 8B/10B code defined in <u>Section 5.2</u> above.The 8x symbol streams containing data packets, link packets, and SKIP ordered-sets is illustrated in <u>Figure 18</u> below.

o5-7.2.1: All 8x ports and 12x ports when configured as a 8x port **shall** implement packet formatting as defined by <u>Section 5.5.5, "8x Packet</u> Format," on page 115.





5.5.5.1 8x PACKET FORMATTING RULES

- 1) The start of packet delimiters (SDP & SLP) **shall** be transmitted in lane zero (0) only.
- 2) The end of packet delimiters (EGP & EBP) **shall** be transmitted in lane three or seven (3 or 7) only.
- 3) When the currently transmitted packet does not end on lane 7, four PAD control symbols **shall** be inserted to align the link for the next transmit operation.
- 4) SKIP ordered-sets **shall** be transmitted on all eight (8) lanes simultaneously.
- 5) When the idle data is placed on the link, the idle data pattern **shall** be inserted on all eight (8) lanes simultaneously.

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6) The pseudo-random idle data for each lane **should** start at a different point in the sequence.

5.5.6 12x PACKET FORMAT

4 The 12x link is composed of twelve physical lanes (0 through 11). The 5 combined data and link packet symbol stream (control and data) are byte striped across physical lanes 0 through 11. In the 12x configuration the 6 start packet delimiters will always be transmitted on physical lane 0, and 7 the end packet delimiters will always be transmitted on physical lane 3, 7, 8 or 11. The link will be padded (PAD control symbols) as necessary to 9 maintain the start of packet alignment rule. When SKIP ordered-sets are 10 needed for clock tolerance compensation, the link is padded as necessary 11 to allow all twelve SKIP ordered-sets to start on the same clock. SKIPS 12 are inserted between packets simultaneously on all physical lanes. The twelve symbol streams, composed of packets, SKIP ordered-sets, and 13 idle data are individually encoded using the 8B/10B code defined in Sec-14 tion 5.2. The 12x symbol streams containing data packets, link packet, idle 15 data and SKIP ordered-sets is illustrated in Figure 19 below. 16

C5-8: All 12x ports **shall** implement packet formatting as defined by Section 5.5.6, "12x Packet Format," on page 117.

#0	#1	#2	#3	Physi #4	cal La #5	anes #6	#7	#8	#9	#10	#11
				Data	Packe	t Pay	load				
				Data	Packe	t Pay	load				
				Data	Packe	t Pay	load				
				Idle I	Data						
					Pala						

Figure 19 12x Packet Formats

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5.5.6.1 12x PACKET FORMATTING RULES

1) The start of packet delimiters (SDP & SLP) **shall** be transmitted in lane zero (0) only.

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	2)	The end of packet delimiters (EGP & EBP) shall be tran lane three, seven, or eleven (3, 7, or 11) only.	smitted in	1
	3)	When the currently transmitted packet does not end on a or eight PAD control symbols shall be inserted to align the next transmit operation.	lane 11, four ne link for the	2 3 4
	4)	SKIP ordered-sets shall be transmitted on all twelve(12) taneously.) lanes simul-	5 6 7
	5)	When the idle data is placed on the link, the idle data pat inserted on all twelve(12) lanes simultaneously.	tern shall be	8 9
	6)	The pseudo-random idle data for each lane should start point in the sequence.	at a different	10 11
5.6 LINK INITIALIZATION AND TH	2 A IN	ING		12
	Th	s saction defines the link/nhysical control process that as	nfiguros and	13
	init	alizes a link for normal operation. A fully-powered port imp	plements this	14
	pro	cess by accomplishing the following:		16
				17
	1)	Waking a remote port on auxiliary power.		18
	2)	Configuring and initializing the link.		19
	3)	Supporting normal packet transfers		20
	4)	Recovering from transient link errors.		21
	Wa atii loc full en sci <u>6:1</u> Arc me Du oth	king a remote port is a special case operation with the long fully-powered and the remote port operating on auxiliar al port polls (See <u>Section 5.6.4.2, "Polling States," on page</u> te port. The remote port detects the presence of this signal y-powered operation. In this special case the signal detect operating on auxiliary power is referred to as a beacon. ibed further in <i>InfiniBand Architecture Specification, Volum</i> High Speed Electrical Signaling - 2.5, 5.0, & 10.0 Gb/s and chitecture Specification, <i>Volume</i> 2, Chapter 14: OS Powe nt.	cal port oper- y power. The <u>e 127</u>) the re- l and initiates cted by the Its use is de- ne 2, Chapter in InfiniBand r Manage-	22 23 24 25 26 27 28 29 30 31 32 33 34 35
	, 2)	Link speed (SDR-2.5 Gb/s. DDR-5.0 Gb/s. or QDR-10.0	Gb/s).	36 36
	-) 3)	Optional correction of lane reversal		37
	4)	Optional correction of inverted received serial data (cros ential signals).	sed differ-	38 39
	C5 <u>C5</u>	-9: This compliance statement is obsolete and has been -9.2.1:	replaced by	40 41 42

C5-9.2.1: All ports **shall** implement link initialization and training as defined by <u>Section 5.6</u>, "Link Initialization and Training," on page 118. Ports are not required to implement the lane reversal and serial data inversion options. Implementations that do not support Enhanced Signaling must use the Link Training State Machine described in Figure 21: Link Training State Machine - Legacy, and **shall not** implementation any Enhanced Signaling functions related to TS3 ordered-sets, Heartbeat ordered-sets, LinkRoundTripLatency, TS-T ordered-sets, or PhyTest compliance testing.

o5-9.2.1: All ports that claim compliance with the Rel. 1.2 Enhanced Signaling **shall** implement link initialization and training as defined by <u>Section 5.6. "Link Initialization and Training." on page 118</u> and **shall** implement all functions related to TS3 ordered-sets, heartbeat ordered-sets, LinkRoundTripLatency measurement, TS-T ordered-sets, or PhyTest compliance testing,

o5-1: This compliance statement is obsolete and has been replaced by <u>o5-9.2.1:</u>.

o5-9.2.1: Ports that implement the serial data inversion option **shall** implement the following:

Section 5.6.7.3, "RxCMD = EnConfig," on page 152 rules #2.

o5-2: This compliance statement is obsolete and has been replaced by <u>o5-9.2.1:</u>.

o5-9.2.1: All 4x, 8x and 12x ports that implement the lane reversal option **shall** implement the following:

<u>Section 5.6.4.6.3, "Config.WaitRmt State," on page 139</u> rule #7 and <u>Section 5.6.4.6.4, "Config.TxRevLanes State," on page 140</u> all rules and <u>Section 5.6.7.3, "RxCMD = EnConfig," on page 152</u> rule #4.

5.6.1 LINK DE-SKEW AND TRAINING SEQUENCE

The terms link de-skew and training sequence are used throughout this section. Both are briefly explained below. Additionally, the characteristics of the training sequence ordered-sets (TS1, TS2, and TS3) are summarized herein.

Link de-skew: A multi-lane link (4x, 8x and 12x) may have many sources of lane to lane skew. These sources include but are not limited to chip I/O drivers and receivers, printed wiring boards, electrical and optical cables, serialization and de-serialization logic, and retiming repeaters. Although symbols are transmitted simultaneously on all lanes, they cannot be expected to arrive at the receiver without lane-to-lane skew. The lane-to-lane skew may include components which are less than a bit time, bit time units (400ps at SDR, 200ps and 100ps at DDR and QDR, respectively),

or full symbol time units (4ns at SDR, 2ns and 1ns at DDR and QDR, respectively) of skew caused by the retiming repeaters' insert/delete operations. A link may have up to two retiming repeaters. Each repeater operates independently on multiple lanes. Because of this independent operation, they may insert or delete a skip symbol independently on each lane. Refer to <u>Section 5.10 on page 161</u> for a complete description of retiming repeaters. The receiving node is required to remove this lane-tolane skew in order to receive and process data on all lanes simultaneously. This process is called "link de-skew". Receivers use TS1, TS2, and TS3 ordered-sets to perform link de-skew functions.

TS1 and TS2: The training sequences TS1 and TS2 provide three fundamental types of information:

- Lane-to-lane skew: Information is provided by the unique structure and length of the of the two training sequences and the fact that they are transmitted without lane-to-lane skew. Both training sequences' (TS1 and TS2) sixteen symbol length (comma and 15 data symbols) allows unambiguous de-skew of up to seven symbol times of skew.
- 2) Lane Identification: The second symbol of the training sequence contains the lane number information. The lane number uniquely identifies each of the twelve possible lanes.
- 3) Lane serial data polarity: The TS1 and TS2 data symbols contain serial data polarity information. When the bit stream on a lane is inverted, the comma and lane number symbols swap running disparity but still decode to the same value. The TS1 data symbol changes from a D10.2 (4Ah) to a D21.5 (B5h), and the TS2 data symbol changes from a D5.2 (45h) to a D26.5 (BAh) providing a clear indication of lane serial data polarity inversion.

TS3: The training sequence TS3 provides the same three fundamental types of information provided by TS1 and TS2. In addition, it provides the following types of information:

- 1) Enabled and Supported Link Speeds: Information is provided by a Link/Physical layer about the speed or speeds that the layer supports and is enabled to operate at. This information is provided in the Symbol 8, the SpeedActive symbol, of the sixteen symbols of the TS3 training sequences. During link training, each Link/Physical layer transmits a series of TS3 training sequences to the Link/Physical layer on the other side of its associated link, as part of the link speed auto-negotiation procedure. A link always operates at the highest speed that is supported and enabled on both ends and supported by the physical channel.
- 2) Link Heartbeat Enabled: The Link Heartbeat function is required at DDR and QDR speeds, and expected at SDR speed. A port may disable use of the Link Heartbeat function, e.g., for interoperation

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with legacy devices at SDR speed. Link Heartbeat will only be put into effect when both ports on a negotiation exchange support and enable it.

- 3) Adaptive Driver De-emphasis Request: Allows a port to request handshake for a simple adaptive driver de-emphasis setting for equalization, with either a default driver de-emphasis setting or one of 16 adaptive driver de-emphasis settings negotiated between transmitter and receiver.
- 4) **Driver De-emphasis Setting request**: Allows a receiver to transmit to its peer transmitter the requested driver de-emphasis setting out of the 17 possible settings.

5.6.2 LINK INITIALIZATION AND TRAINING OPTIONS

Two independent optional features are defined as part of link initialization and training. Both are intended to allow on chip logic to correct non-optimum pin assignments which may occur when connecting an IBA link chip-to-chip or chip-to-connector. These options can eliminate the two common printed wiring board (PWB) layout issues of crossed differential pair and bus bow ties. Implementing these optional features allows the PWB layout to focus on signal integrity with simplified connections.

5.6.2.1 INVERTED SERIAL DATA CORRECTION (OPTIONAL)

The inverted serial data correction feature allows the receiver logic to correct a receive differential pair that is crossed in the PWB layout. Such a receiver will need to test the polarity of the received training sequences and correct inverted data as part of link configuration. This option does not provide the capability to correct the polarity of transmit data.

To be inter-operable with ports that do not implement inverted serial data correction, the polarity at the transmitting connector must be as specified in the InfiniBand *Architecture Specification*, <u>Chapter 7: Copper Cable</u> and <u>Chapter 10: Backplane Connector Specification</u>.

5.6.2.2 LANE REVERSAL CORRECTION (OPTIONAL)

31 The lane reversal feature allows a PWB layout to connect 4x, 8x or 12x ports in reversed lane number order. The receiver logic uses the lane 32 number symbol in the training sequences (TS1 or TS2) to detect and cor-33 rect the reversed lane connections in the PWB layout. When the remote 34 port is incapable of correcting receive lane reversal (link width is less than 35 the local port or the port does not implement this option) the local port will 36 reverse its transmit lane as part of its configuration process. (see 37 Section 5.6.4.6, "Configuration States - Enhanced Signaling," on 38 page 133)

5.6.3 INTERACTIONS WITH OTHER ENTITIES

Link training is an involved process that requires interactions with other entities. This section briefly describes these interfaces and refers the reader to other sections for more detailed information. <u>Figure 20</u> illustrates all entities that interact with the link training state machine in the link initialization and configuration process.



Figure 20 Link Training State Machine Interactions

The interface between the link layer and the link/phy layer is comprised of the signals LinkPhyRecover and LinkPhyStat. These logical signals are described in <u>Section 5.3.3</u>, "Packet Logical Interfaces," on page 103.

The link training state machine and the unit's management entity communicate over a set of logical signals. Although this logical interface is not defined completely in this specification, functions that need to be carried out over this interface are defined. The management messages related to the link training state machine operations are described in <u>Section 5.4, "Management Datagram Control and Status Interface," on page 104</u>.

The link training state machine also interfaces to the transmitter and receiver logic to coordinate the link initialization and configuration operations. The interface to the transmitter is in the form of commands (TxCMD) for the transmitter to perform. Similarly, the receiver interface has a set of commands (RxCMD) or configurations and a set of receiver status (Rx-Status) values.

These commands and status conditions are listed in <u>Table 16</u> below and are described in detail in <u>Section 5.6.6</u> and <u>Section 5.6.7</u>. The receiver status conditions (RxStatus) are not mutually exclusive conditions.

Table 16 Transmitter and Receiver Interface

Transmitter		Receiver			
TxCMD	Speed	RxCMD	Status (RxStatus)		
Disable		Disable			
SendTS1, SendTS2, SendTS3	SPEED = MinEnabledSpeed, SPEED = MaxBothActive	WaitTS1,WaitTS2, WaitTS3	RcvdTS1, RcvdTS2, RcvdTS3		
RevLanes		EnConfig, EnDeSkew	RxTrained		
SendIdle		WaitIdle	Rcvdldle		
Enable		Enable	RxMajorError, RxHeartbeatError		
		WaitTS-T	RcvdTS-T		

5.6.4 LINK TRAINING STATE MACHINE

Link initialization, configuration, and link error recovery operations are performed by the link training state machine. This state machine is described in this section in the form of hierarchical states. As depicted in Figure 22, the link training state machine has seven primary states. Some of these states are super states composed of two or more states.

The link training state machine has the following primary states:

- 1) **Disabled**: Port drives its outputs to quiescent levels and does not respond to received data.
- 2) **Sleeping**: In this super state, the port drives its outputs to quiescent levels and responds to received training sequences.
- 3) **Polling**: In this super state, the port transmits training sequences and responds to received training sequences. This is the default state following power on.
- 4) **Configuration**: A transient super state with both the transmitter and receiver active. The port is attempting to configure and transition to the LinkUp state.
- 5) **LinkUp**: This is the normal link operation state. The port is available to transfer packets.
- 6) **Recovery**: The recovery super state attempts to re-synchronize the link and return it to normal operation. This state is entered when a port experiences loss of link synchronization, a major error, or when a link layer error triggers error recovery.
- 7) **Phy Test**: The Physical Layer test state allows simplified testing to determine compliance of physical layer transmitter driver and receiver circuitry with specified requirements. This state is defined for

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Enhanced Signaling, and is not implemented in products not supporting Enhanced Signaling.

These primary states directly map to the enumerated port states defined in <u>Section 5.4, "Management Datagram Control and Status Interface," on</u> <u>page 104</u>.

The status of the link training state machine is also reported to the link layer in a more abstract fashion. The "LinkPhyStat" logical signal over this interface provides the values "Up" and "Down". This logical signal is given the "Up" value when this state machine is in the LinkUp state. It is given the "Down" value in all other states.

The initial or post-reset state of the link training state machine is **Polling**. This insures that a newly connected and powered on port will be recognized by any remote port. Management commands can force the link training state machine to the following states: **Disabled**, **Polling**, or **Sleeping**. Management commands also set a default state for link down. All other state transitions are under the control of the link training state machine. Test equipment can control the transition in and out of the **Phy Test** state by injecting patterns in the port's receiver.

<u>Figure 21</u> shows the Link Training State Machine for products not supporting Enhanced Signaling. <u>Figure 22</u> shows the Link Training State Machine for products that support Enhanced Signaling, which adds the **Phy Test** state, and additional substates within the **Configuration** super state.

In <u>Figure 22</u>, all state transition events are based on management commands, delay events, or receiver status. These receiver status conditions are described later in <u>Section 5.6.7 on page 151</u>.

Operations in certain states involve delays or time-out periods. These events are denoted the state diagrams as state transitions labeled with DelayTimeOut (time). These time-out periods start as the state is entered and cleared when a transition to a different state is taken. Time-out periods cannot be re-started within a state. (See Section 5.6.5 on page 147)



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Figure 22 Link Training State Machine - Enhanced Signaling

5.6.4.1 DISABLED STATE

As the state name implies, there is no physical layer activity in this state, and both the transmitter and receiver are disabled. The transmitter outputs are forced to a quiescent condition, and receiver inputs are ignored. Entrance to and exit from the Disabled state are controlled by manage-

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	ment commands. In the Port Disabled State the followin mands shall be active:	g rules and com- 1
	1) TxCMD = Disable	3
	2) RxCMD = Disable	4
	3) LinkPhyStat = Down	5
	4) SymbolErrorCounter is inhibited	7
5.6.4.2 POLLING STATES		8
	ration. The link training state machine cycles between the These states are transmitting repeated TS1(s) for 2ms is followed by 100ms of a quiescent output in Polling.Quies the port's receiver is configured to detect TS1 ordered-se received, the link training state machine transfers control ration Super State. The states of the Polling Super State the state graph shown in Figure 23.	ne two states. n Polling.Active t. In both states, ets. When TS1 is of to the Configu- are expanded in 1
		1
	CMD = Polling or LinkPhyReset or PowerOnReset Polling.Active	ry Failed) 1 Illing 2 2 2 2 2
	SPEED=MinEnabledSpeedRcvdTS-TxCMD = SendTS1RcvdTS1RxCMD = WaitTS1, WaitTS-TRcvdTS1	r 2 2 2
	DelayTimeOut (2ms)	2 2 2 2
	Polling.Quiet	3
	TxCMD = Disable RxCMD = WaitTS1, WaitTS-T	3
		3
		3
	1	3
	▼ [To Configuration State] [To F	Phy Test State]
	Figure 23 Polling Super State (Expand	ed) 3
		3
		4

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5.6.4.2.1 POLLING.ACTIVE STATE

	The Polling.Active state sends a stream of TS1s and at the same time en- ables detection of TS1s on all receiver lanes. The transmitter speed is set to the minimum enabled speed. In the Polling.Active state the following rules and commands shall be active:				
	1) SPEED = MinEnabledSpeed	6			
	2) TxCMD = SendTS1	7			
	3) RxCMD = WaitTS1, WaitTS-T	9			
	4) LinkPhyStat = Down	10			
	5) SymbolErrorCounter is inhibited.	11			
	6) LinkSpeedActive = LinkSpeedEnabled	12			
	 7) TS1 and SKIP ordered-sets are transmitted on all lanes 	14			
	8) If RyStatus – RoydTS1, the next state is Configuration	15			
	a) If Prestatus - RevertS T, the part state is Doringulation.	16			
	$\frac{1}{2} = \frac{1}{2} = \frac{1}$	18			
	TO) Else il Delay TimeOut(2ms), the next state is Polling.Quiet	19			
5.6.4.2.2 POLLING.QUIET STATE		20			
	The Polling.Quiet state inhibits the transmitter and continues to enable de- tection of TS1 on all receiver lanes. When TS1 is detected, configuration can be started. In the Polling.Quiet state, the following rules and com- mands shall be active:	21 22 23 24			
	1) TxCMD = Disable	25 26			
	2) RxCMD = WaitTS1	27			
	3) LinkPhyStat = Down	28			
	4) SymbolErrorCounter is inhibited	29			
	$= \int \mathbf{U} \mathbf{U} \mathbf{U} \mathbf{U} \mathbf{U} \mathbf{U} \mathbf{U} \mathbf{U}$	31			
	(a) If PxStatus = RevolTST; the next state is Configuration	32			
	6) If RXStatus = RCV01S-1, the next state is Phy lest T_{1} =	33			
	7) Else if Delay I meOut(100ms), the next state is Polling. Active	34			
5.6.4.3 SLEEPING STATES		36			
	The Sleeping states are used to deactivate a link without powering off the	37			
	port. When a port enters the sleeping state, it first disables its transmitter and receiver and then delays, allowing all link activity to cease. Following the delay the receiver is enabled to detect TS1 ordered-sets. When a TS1				
	is detected, port configuration is started. The states of the Sleeping Super State are expanded in the state graph shown in Figure 24.	40 41 42			



InfiniBand TM Architecture Release 1.2 VOLUME 2 - PHYSICAL SPECIFICATIONS		Link/Phy Interface	October, 2004 FINAL	-
	2)	TxCMD = Disable		_
	3)	RxCMD = WaitTS1, WaitTS-T		1
	4)	LinkPhyStat = Down		3
	5)	SymbolErrorCounter is inhibited		4
	6)	LinkSpeedActive = LinkSpeedEnabled		5
	7)	If RxStatus = RcvdTS1, the next state is Configur	ation	7
	8)	If RxStatus = RcvdTS-T, the next state is Phy Tes	t	8
5.6.4.4 PHY TEST STATE				9
	Th tes tio <u>Co</u> a T foll	e Phy Test state allows the transmitter and receive sted by external test equipment for compliance with over specifications. This state is not used for norma n of this state is described further in <u>Section 5.12</u> . <u>Section 5.12</u> . <u>Section 5.12</u> . <u>Section 5.12</u> . <u>Section 5.12</u> .	r circuitry to be transmitter and re- l operations. Opera- <u>'Physical Layer</u> occurs on receipt of Phy Test state, the	10 11 12 13 14 15 16
	1)	SPEED = Value determined in TS-T ordered-set		17 18
	2)	RxCMD = WaitTS1		19
	3)	Transmitted signals will follow rules defined in <u>Sec</u> <u>Layer Compliance Testing," on page 169</u> .	tion 5.12, "Physical	20 21
	4)	If RxStatus = RcvdTS1, the next state is the LinkI (Polling or Sleeping)	DownDefaultState	22 23
5.6.4.5 CONFIGURATION STATES	- Le	GACY OPERATION		24
	Th the mւ	e Configuration Super State controls the configurate link. A low level protocol using TS1, TS2, and Idle l inicate the state of the two ports on the link.	tion and training of Data is used to com-	26 27 28
	Th tha ph	e first step is to send a extended stream of TS1 ord at the port has started the configuration process. Thi ysical connection to stabilize (debounce delay).	ered-sets indicating s allows time for the	29 30 31
	Fo the col cei de sei (tra	llowing the delay, the second step of configuration e receivers to auto-configure and de-skew. The ren mpleted receiver training and be transmitting TS2 o ever can auto-configure and de-skew while receiving red-sets. The transmitter continues to send a streat ts and waits for the receiver to complete configurat aining).	begins by enabling note port may have rdered-sets. The re- ig TS1 or TS2 or- im of TS1 ordered- ion and de-skew	32 33 34 35 36 37 38 39
	Th tra the	e third step starts when the receiver has completed nsmitter begins to send a stream of TS2 ordered-s e local receiver is trained. A delay is started, and th	d training, and the lets indicating that le port waits for the	40 41 42

remote port to indicate that its receiver has completed training. While waiting the received training sequences are checked for lane order errors.

At the end of the delay, if the remote port has not indicated that it is trained, a port implementing the optional lane reversal will reverse its transmit lanes, start a short delay, and continue to wait for the remote port to report that its receiver has completed training. While waiting the received training sequences are checked for lane order errors. If both ports are not trained at the end of the delay(s), configuration has failed. If the port completes training before the end of the delay(s), the final step of configuration starts when the port is both sending and receiving TS2 ordered-sets.

The final step of link configuration transmits the idle data stream and waits to receive idle data. When the port is both sending idle data and receiving idle data, configuration is complete, and the link is up. While waiting for idle data the receivers continue to verify TS2 lane order. Receiving TS1 in this state will force the restart of link configuration.

The states of Configuration Super State are expanded in the state graph shown in <u>Figure 25</u>.

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5.6.4.6 CONFIGURATION STATES - ENHANCED SIGNALING

In this release of this specification, additional functions are added to the Configuration states to support enhanced signaling capabilities of the links, including higher speed operation at DDR (5.0 Gb/s) and QDR (10.0 Gb/s) bit rates, Link Heartbeat function (described in <u>Section 5.11, "Link Heartbeat," on page 166</u>), and support for transmitter and receiver equalization to better enable operation at higher bit rates over a variety of media. Several additional states and an additional training sequence (TS3) are added for the purpose of negotiating common use of these enhanced capabilities between the two peer ports on a link.

The first three steps of link initialization are the same as for legacy devices: a TS1 exchange assures that both transmitters are active, a TS2 exchange assures that both receivers are trained, and lane reversal assures correct polarity at each end of the link.

Following these steps, both ports transmit a TS3 training-set, indicating which enhanced capabilities they are enabled to support (DDR/QDR, Equalization, and Link Heartbeat). Each transmitter compares its own capabilities with the capabilities indicated in the TS3 received from the other end of the link. When both sides have sent and received TS3s, indicating agreement on common enhanced capabilities, they act to enable those capabilities. These negotiations occur at the lowest enabled speed, which will generally be the SDR speed.

The TS3 exchange for negotiating link speed operates by having each port send a bit map of the active speeds, in the format used in the *SM.PortInfo(LinkSpeedEnabled)*, and *SM.PortInfo(LinkSpeedSupported)* MADs. The first time the ports traverse the states negotiating enhanced capabilities, they send TS3 ordered-sets indicating the link speeds enabled by the SM (*LinkSpeedEnabled*). If, however, a particular speed is attempted, and found to be unsupportable (for example, link attenuation is too high for intact data transmission), the bit corresponding to this speed is cleared to 0 in the *LinkSpeedActive* field, and in the following TS3 ordered-sets. A logical AND operation on the transmitted and received fields is used to determine the speed(s) supported on both ports, and further operation is attempted at the highest speed that is active on both.

A link pair will go through TS3 exchange at least twice, to ensure that the supported capabilities on both ends of the link are consistent, and supported by the link media. Links will always be **Active** at the highest speed which is **Enabled** in both ports driving the link, and supported by the link transmission medium. During the negotiation phase of the configuration super state, multiple speeds bits may be set to 1 in the **LinkSpeedActive** bit map exchanged in TS3 ordered-sets, but once consistent and correct operation has been established, only one **LinkSpeedActive** bit will be set

to 1. Links always operate at the same speed in both directions, and a port always configures its transmitter and receiver to operate at the same speed.

The TS3 exchange is also used to establish whether adaptive driver deemphasis equalization training is requested. If either side requested adaptive equalization, both sides will participate. For equalization training, each transmitter sends idle data at the maximum speed commonly active in both ports (typically DDR or QDR, but possibly SDR as well), for a 100 millisecond period. The 100 ms. period is split into a 36 ms period where data is sent with a default transmitter equalization setting, for receivers which don't support adaptive equalization, and 16 separate adaptive transmitter equalization setting slots, of 4ms duration each. On each 4 ms. slot, the transmitter sends data using one of a set of vendor-dependent pre-emphasis settings. The receiver, on each slot, attempts to receive intact data, optionally adjusting a receiver equalization setting. The receiver determines which is the first slot that provides a signal good enough to be equalized at the receiver.

Implementation Note

On definition of the terms *Enabled*, *Supported*, and *Active*, in the context of describing link widths and speeds:

The set of *Enabled* widths or speeds is determined by the subnet manager, and will be equal to the set of or a subset of the widths or speeds *Supported* by the design and implementation of the port. The *Active* width or speed is determined by a combination of the implemented capabilities in the two ports of a link, and by the link used to connect them. For example, a pair of ports sharing a link may both *Support* and be *Enabled* for SDR/DDR/QDR operation (7), but the cable over which they are connected may only allow intact data transmission at SDR speed. In this case, the port Link/Phy logic would set the *LinkSpeed-Active* value to 1 on both ports. The actual operating link speed or link width, as determined by the Link/Phy logic during the Configuration super state, is reflected in the *Active* fields.

Implementation Note:

Equalization is used to compensate for signal distortion (attenuation or dispersion) that occurs in the medium between transmitter and receiver. The distortion being compensated for may take a variety of forms, including attenuation of high-frequency components, frequency-dependent crosstalk, or frequency-dependent reflections. Signal-processing circuitry in the transmitter, or the receiver, or (typically) both, can equalize out some of the effect of some distortions. This equalization may, for example, take the form of emphasizing high frequencies (fast toggles) or de-emphasizing low frequencies (strings of 1s or 0s), or of de-emphasizing high frequencies, in cases where frequency-dependent crosstalk is the major distortion. The equalization circuitry should therefore be adaptive to the characteristics of the particular link medium.

Achieving ideal adaptive equalization over the wide variety of copper and optical media of the various distances used for InfiniBandTM links is very complex problem. The algorithm described here (16 different adaptive driver de-emphasis settings, which the receiver selects from, after attempting adaptive receiver equalization on each) provides a mechanism for both transmitter and receiver equalization with moderate complexity. The algorithm also allows interoperability with ports that don't implement adaptive equalization.

Since the maximum physical length of an InfiniBand cable this release using long wavelength optical fiber links is 10 km, with speed-of-light round-trip latency on the order of 100 microseconds (0.1 ms), the two ends of a link may be un-synchronized with each other by this much. This synchronization period determines, along with the (-1us/ +126us) clock tolerance and 100 ppm variation in clock frequency described in <u>Section 5.6.5, "State Machine Delays and Timeouts," on page 147</u>, the window of proper transmitter-equalized data within the 4ms slot period, and must be taken into account at the receiver when determining transmitter equalization setting slots.

Following attempted transmission at the maximum speed that is active on both ports, including transmitter and receiver adaptive equalization, the ports then transition through an WaitCfgMaxBothActive state, to ensure that both ports have completed attempting operation at the maximum active speed, and then do another round of TS3 exchange. This round allows both ports to indicate whether they were able to receive intact data at the attempted speed, and if so, to allow each port's receiver to indicate to its peer port's transmitter which of the 16 4 ms slots was the first that had a transmitter equalization setting with good enough signal for receiver data recovery. The use of the first good slot allows the transmitter/receiver pair to optimize the link's overall power usage.

The TS3 exchange also establishes the use of Link Heartbeat. Link Heartbeat is used (a) to determine that both receivers on a link are receiving data from their peer transmitters rather than from crosstalk, and (b) to determine the link round-trip latency for data to traverse the link in both directions. Link Heartbeat is required at DDR and QDR speeds, due to the small received signal swings and lack of a signal detect capability at the higher bit rates. Link Heartbeat is also useful at SDR speed, and is required for devices supporting Enhanced Signaling, even if they only support SDR. A bit in the exchanged TS3 indicates that Link Heartbeat is requested. If both ports request the use of Link Heartbeat, it is used when the link transitions to the LinkUp state. Further details on Link Heartbeat may be found in <u>Section 5.11, "Link Heartbeat," on page 166</u>.

Once both ports on a link have exchanged consistent TS3s, and assured correct operation at the highest commonly-*Active* speed, they will transition to the Config.WaitCfgEnhanced state, to indicate completion of configuration for enhanced operation, and from there to Config.LinkUp.

On connection with a port that does not support Enhanced Signaling, or during legacy operation, the port state machine would traverse the states directly from top to bottom, at SDR rate, bypassing the Config.Test, Config.WaitRmtTest, and Config.WaitCfgEnhanced states.

The states of Configuration Super State for ports supporting <u>Chapter 5</u>: operation are expanded in the state diagram shown in <u>Figure 26</u>.

A simplified diagram of the State graph is shown in <u>Figure 27</u>, along with a typical control flow through the states, showing negotiation from SDR up to higher speed operation.

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5.6.4.6.1 CONFIG.DEBOUNCE STATE

In the debounce state (Config.Debounce), the transmitter sends a series of TS1 ordered-sets on all lanes. The receiver status is not checked in this state. In receivers with adaptive receiver equalization, the 100 ms duration of this state may optionally be used for determining receiver equalization settings. Operation in Config.Debounce is always at SDR speed. In the Config.Debounce state, the following rules and commands **shall** be active:

		38
1)	TxCMD = SendTS1	39
2)	RxCMD = WaitTS1	40
3)	LinkPhyStat = Down	41
-)		42

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	4)	TS1 and SKIP ordered-sets are transmitted on all la	nes	-
	5)	SymbolErrorCounter is inhibited		2
	6)	If DelayTimeOut(100ms), next state is Config.RcvrC	fg.	3
5.6.4.6.2 CONFIG.RCVRCFG STATE				4
	In str or all co Th Co	the Receiver Configure (Config.RcvrCfg) state, the tra- eam of TS1 ordered-sets on all lanes. The receiver us TS2 ordered-sets to identify the width of the remote p y correct lane reversal and inverted lane data. When the mpleted configuration and training, it reports Receiver the transmitter speed is set to the minimum enabled sp onfig.RcvrCfg state, the following rules and commands	nsmitter sends a ses received TS1 ort and to option- the receiver has r Trained status. eed. In the s shall be active:	
	1)	SPEED = MinEnabledSpeed		
	2)	TxCMD = SendTS1		
	3)	RxCMD = EnConfig		
	4)	LinkPhyStat = Down		
	5)	TS1 and SKIP ordered-sets are transmitted on all la	nes	
	6)	SymbolErrorCounter is enabled		
	7)	LinkSpeedActive = LinkSpeedEnabled		
	8)	If the RxStatus = RxTrained, the next state is Config	.WaitRmt.	
	9)	Else if DelayTimeOut (150 ms) the next state is the L State (Polling or Sleeping).	.inkDownDefault-	
5.6.4.6.3 CONFIG.WAITRMT STATE				
		the Wait Remote (Config.WaitRmt) state, the transmitter TS2 ordered-sets on all lanes. The receiver monitors ysical lanes waiting for a transition from TS1 to TS2 of ting the remote port has completed its configuration. If tion is supported and the delay has timed out, the next e port's transmit lanes. If the lane reversal option is no e delay has timed out, the next state will be retry receive the Config.WaitRmt state the following rules and com tive:	er sends a series the configured ordered-sets indi- the lane reversal state will reverse of supported and ver configuration. mands shall be	
	1)	TxCMD = SendTS2 (minimum of 16 TS2s)		
	2)	RxCMD = WaitTS2		
	3)	LinkPhyStat = Down		
	4)	TS2 and SKIP ordered-sets are transmitted on all la	nes	
	5)	SymbolErrorCounter is enabled		
	6)	If received "lane order error" the next state is Config	.RcvrCfg.	4

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	7)	Else If the RxStatus = RcvdTS2, the next stat hanced for ports implementing Rel. 1.2 Enha bility. For ports implementing only legacy func- is Config.Idle.	te is Config.CfgEn- nced Signaling capa- ctionality, the next state
	8)	Else If "Lane Reversal Option" and DelayTim state is Config.TxRevLanes.	eOut(2ms), the next
	9)	Else if not "Lane Reversal Option" and Delay state is Config.RcvrCfg.	TimeOut(2ms), the next $\frac{6}{7}$
5.6.4.6.4 CONFIG.TXREVLANES STA	TE		ç
	In rev all a t co rul	the reverse transmit lanes (Config.TxRevLane verses its lanes and continues to sends a series lanes. The receiver monitors the configured pl ransition from TS1 to TS2 ordered-sets, indica mpleted its configuration. In the Config.TxRevL es and commands shall be active:	s) state, the transmitter of TS2 ordered-sets on hysical lanes waiting for ting the remote port has anes state, the following
	1)	TxCMD = SendTS2 (minimum of 16 TS2s)	1
	2)	TxCMD = RevLanes	1
	3)	RxCMD = WaitTS2	1
	4)	LinkPhyStat = Down	2
	5)	TS2 and SKIP ordered-sets are transmitted of	on all lanes
	6)	SymbolErrorCounter is enabled	2
	7)	If received "lane order error" the next state is	Config.RcvrCfg
	8)	Else If the RxStatus = RcvdTS2, the next stat hanced.	te is Config.CfgEn-
	9)	Else If DelayTimeOut(2ms), the next state is	Config.RcvrCfg.
5.6.4.6.5 CONFIG.CFGENHANCED ST	ATE	- RELEASE 1.2 ENHANCED SIGNALING	3
	In tra wit sc <u>on</u> to	the Configure Enhanced Capabilities state (Consmitter sends TS3 (Training Sequence 3) or other the link peer port what enhanced capabilities ribed in <u>Section 5.3.2.4, "Training Sequence Therappage 99</u> , a TS3 ordered-set includes fields whindicate	onfig.CfgEnhanced) the lered-sets to negotiate s will be used. As de- <u>ree Ordered-Set (TS3).</u> " ich allow the transmitter
	•	which link speeds may be attempted (in a for <i>SM.PortInfo(LinkSpeedEnabled)</i> and <i>SM.P Supported</i>) fields described in <u>Section 5.4.2 get)," on page 107</u>),	m consistent with the PortInfo(LinkSpeed- , "Status Outputs (MAD

• whether or not adaptive transmitter pre-emphasis is requested, and

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	•	whether or not the LINK HEARTBEAT functionality and QDR operation as described in <u>Section 5.11</u> , " on page 166, is enabled, and	, required for DDR <u>Link Heartbeat,"</u>	1
	•	which transmitter equalization setting should be us training has already occurred in the Config.Equaliz	ed, if equalization ation state.	3
	In be	he Config.CfgEnhanced state the following rules and active:	d commands shall	5 6 7
	1)	TxCMD = SendTS3		8
	2)	RxCMD = WaitTS3		9
	3)	LinkPhyStat = Down		1
	4)	TS3 and SKIP ordered-sets are transmitted on all	anes	1
	5)	SymbolErrorCounter is inhibited		1:
	6)	If RxStatus = RcvdTS3, and the exchanged TS3 in request for equalization on either port, OR (b) Max changed from previous visit (i.e., first time on state Config.RcvrCfg, or equalization failed on one of the state is Config.Test. Also, <i>LinkSpeedActive</i> is set of the current <i>LinkSpeedActive</i> and the SpeedAct ceived TS3 to determine the speed(s) active on bo	dicate both (a) a BothActive since e peers), the next equal to the AND tive field of the re- oth ports.	1 1 1 1 1 1 2
	7)	Else if RxStatus = RcvdTS3, and either no further of quested AND MaxBothActive has not changed from and <i>LinkSpeedActive</i> is set to the highest bit set of next state is Config.WaitCfgEnhanced.	equalization is re- n previous visit, on both peers, the	2 2 2 2
	8)	Else If RxStatus = RcvdIdle (indicating the port is c legacy device port), the next state is Config.Idle.	onnected to a	2
		• For legacy compatibility, an 8x device should a Rcvdldle if it receives Idles on only lanes 03, <u>Section 5.6.7.7</u> , "RxCMD = WaitIdle," on page	ssert RxStatus = as described in <u>154</u> .	2 2 2
		 After following this transition, since the port is of acy device, all Rel. 1.2 Enhanced Signaling car (DDR/QDR, heartbeat, etc.) are inactivated. Fur device reverting to legacy operation shall oper link width, with only lanes 0-3 or lane 0 configured 	connected to a leg- pabilities Irthermore, an 8x ate with 4x or 1x red.	3 3 3 3
	9)	Else if DelayTimeOut (2 ms), the next state is Cont	iig.RcvrCfg.	3
5.6.4.6.6 CONFIG.TEST STATE - RELI	EASE	1.2 ENHANCED SIGNALING		3
	In at 10 de	the Configure Test state (Config.Test) the transmitter the maximum speed indicated in the <i>LinkSpeedAc</i> 0 millisecond period. The 100 ms. period is split into fault transmitter equalization time, and 16 separate a	will send idle data tive bit map, for a a 36 ms period of daptive transmitter	3 3 3 4

equalization setting slots of 4ms duration each. On each 4 ms slot, the transmitter sends one of a vendor-dependent set of adaptive equalization

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settings. The receiver, on each slot, attempts to receive intact data (valid and supported 8b/10b code groups, with correct running disparity), while optionally adjusting receiver equalization settings.

The receiver equalization techniques and settings used are vendor-dependent, don't require transmitter/receiver handshaking across a link. Therefore, the receiver equalization is unspecified here.

Once the 100 ms period of the Config.Test state is over, the receiver decides which of the 16 adaptive transmitter equalization settings was the first usable one. This request is indicated in the TS3 ordered-sets transmitted in the Config.CfgEnhanced state following this Config.Test state.

Transmitter and receiver adaptive equalization capabilities are optional, and may not be implemented in some devices. In this case, the non-implementing device will return a TS3 with DDSV and the DDS bits all cleared to 0, and the attached device will use the default equalization setting of the first 36 ms.

In the Config. Test state the following rules and commands shall be active:

- 1) SPEED = MaxBothActive
- 2) TxCMD = SendIdle
- 3) RxCMD = WaitIdle
- 4) Idle and SKIP ordered-sets are transmitted on configured lanes
- 5) LinkPhyStat = Down
- 6) SymbolErrorCounter is enabled
- 7) If DelayTimeOut(100 ms), next state is Config.WaitRmtTest.
 - If the receiver was unable to recover data from the received signal without incurring any minor link errors, the bit indicating the currently-active speed, MaxBothEnabled, should be cleared to 0 in *LinkSpeedsActive*. This modified Speeds mask, indicating that the current speed is not supported, is reflected in further transmitted TS3 ordered-sets.
 - A receiver MAY use SKIP ordered-sets to ensure that the requirement of total link skew of 6 symbol times (60 UI) or less has been met. Please see <u>Table 28</u>, <u>Table 41</u>, <u>Table 60</u>, <u>Table 61</u>, and <u>Table 62</u>. If the total link skew is measured to be more than 6 symbol times, the bit indicating the currently-active speed, MaxBothEnabled, should be cleared to 0 in LinkSpeedsActive. This modified Speeds mask, indicating that the current speed is not supported, is reflected in further transmitted TS3 ordered-sets.

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5.6.4.6.7 CONFIG.WAITRMTTEST STATE - RELEASE 1.2 ENHANCED SIGNALING

In the Configure Wait for Remote Test state (Config.WaitRmtTest) the transmitter sends a series of TS2 ordered-sets at the MinEnabledSpeed transmitter speed to indicate to the link peer that it has completed at-tempting operation at the maximum speed commonly active in both ports, with attempted equalization training. In the Config.WaitRmtTest state the following rules and commands **shall** be active:

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- 1) SPEED = MinEnabledSpeed
- 2) TxCMD = SendTS2
- 3) RxCMD = EnDeskew
- 4) LinkPhyStat = Down
- 5) TS2 and SKIP ordered-sets are transmitted on all lanes at the currently-active transmitter speed.
- 6) SymbolErrorCounter is inhibited
- 7) If DelayTimeOut (2 ms), the next state is Config.CfgEnhanced

5.6.4.6.8 CONFIG.WAITCFGENHANCED STATE - RELEASE 1.2 ENHANCED SIGNALING

In the Configure Wait Remote Configure Enhanced state (Config.WaitCfgEnhanced) the transmitter sends a series of TS2 ordered-sets at the currently-active transmitter speed to indicate to the link peer that it has (a) completed TS3 exchange for negotiating enhanced capabilities, and (b) committed to operation at the speed negotiated in the Config.CfgEnhanced TS3 exchange and attempted in a previous Config.Test state. In the Config.WaitCfgEnhanced state the following rules and commands shall be active:

- 1) SPEED = MaxBothActive
- 2) TxCMD = SendTS2
- 3) RxCMD = EnDeSkew
- 4) LinkPhyStat = Down
- 5) TS2 and SKIP ordered-sets are transmitted on all lanes at the currently-active transmitter speed.
- 6) SymbolErrorCounter is inhibited
- 7) If DelayTimeOut (2 ms), the next state is Config.Idle.

5.6.4.6.9 CONFIG.IDLE STATE

In the configuration idle (Config.Idle) state, both the local and remote ports have completed configuration and training. The port now transmits link idle data at the configured active speed. The receiver monitors the configured physical lanes, waiting for a transition from TS2 ordered-sets to Idle Data. When Link Idle Data is received the link is up. In the Config.Idle state, the following rules and commands **shall** be active: 42

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	1) TxCMD = SendIdle	1	1
	2) RxCMD = WaitIdle	2	2
	3) LinkPhyStat = Down	3	3
	4) Idle data and SKIP ordered-sets are transmitted only.	l on configured lanes 5	4 5
	5) SymbolErrorCounter is enabled	6) 7
	 If RxStatus = RcvdTS1 or If DelayTimeOut(2ms) Config.RcvrCfg.), the next state is	3
5.6.4.7 LINKUP STATE		1	10
	The LinkUp state is the normal operational state of vided by the Link Layer are transmitted, and receive warded to the Link Layer. This is the only state in whogical status signal LinkPhyStat is assigned the valuthe link is available to transfer packets. In the LinkUp error handling is enabled. The Physical Link Error Heror Section 5.7, "Link Physical Error Handling," on page state the following rules and commands shall be added	the port. Packets pro- ed packets are for- nich the Link Physical e "Up", indicating that p state, Physical Link landling is defined in <u>e 156</u> . In the LinkUP ttive:	1 2 3 4 5 6 7
	1) TxCMD = Enable	1	19
	2) RxCMD = Enable	2	20 21
	3) LinkPhyStat = Up	2	22
	4) The SymbolErrorCounter is enabled	2	23
	5) If RxStatus = RxMajorError or LinkPhyRecover, covery.	the next state is Re-	24 25
	6) If RxStatus = RxHeartbeatError,	2	20 27
	a) The <i>LinkDownedCounter</i> is incremented	2	28
	a) The <i>LinkRoundTripLatency</i> value is reset	to 0xFFFF FFFF 2	29
	b) The next state is the LinkDownDefaultState	(Polling or Sleeping)	30 21
5.6.4.8 LINK ERROR RECOVERY	STATES	3	32 32
	The Link Error Recovery Super State controls port error process is triggered when an error is detected Link/Physical Layer. The Physical Layer error handle minor errors and, when a rate threshold is reached or is detected, triggers recovery. (See Section 5.7 on process)	rror recovery. The re- d by the Link Layer or ling logic monitors or when a major error page 156)	34 35 36 37
	The recovery process starts by sending a stream of trigger error recovery at the remote port. When TS1 the local receiver, it will use the current configuration serial data inversion, and speed) to retrain.	TS1 ordered-sets to or TS2 is received by (width, lane reversal, 4	39 39 10 11 12
The second step of recovery starts when the receiver has completed retraining. The port starts sending a stream of TS2 ordered-sets. The port then waits for the remote port to complete retraining. When the port is both sending and receiving TS2, both receivers have been retrained, and the second step of recovery is complete.

In the final step of link recovery, the port transmits an idle data stream and waits for idle data. When the port is both sending and receiving idle data, recovery is complete, and the link is up.

If the recovery process fails at any step, the Link/Physical Layer state machine returns to its link down default state. 10

The states of Recovery Super State are expanded in the state graph shown in Figure 28.



manded to send a series of TS1 ordered-sets using the currently configured lanes. The receiver is enabled to reacquire symbol sync and then to

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5.6.4.8.1 RECOVERY.RETRAIN STATE

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	de-skew the lanes. In the Recovery.Retrain state the commands shall be active:	following rules and 1
	1) TxCMD = SendTS1 (minimum of 16 TS1s)	3
	2) RxCMD = EnDeSkew	4
	3) LinkPhyStat = Down	5
	4) TS1 and SKIP ordered-sets are transmitted on co	onfigured lanes only. 7
	5) The port SymbolErrorCounter is enabled.	8
	6) If the RxStatus = RxTrained, the next state is Rec	overy.WaitRmt.
	7) Else if DelayTimeOut(2ms),	11
	a) The <i>LinkDownedCounter</i> is incremented	12
	b) The <i>LinkRoundTripLatency</i> value is reset to	0xFFFF FFFF 13
	c) The next state is the LinkDownDefaultState (F	¹⁴ olling or Sleeping)
5.6.4.8.2 RECOVERY.WAITRMT STAT		16
	In the Recovery Wait Remote state (Recovery.WaitRm commanded to send a series of TS2 ordered-sets on lanes. The receiver monitors the receive streams on th In the Recovery.WaitRmt state the following rules and active:	17), the transmitter is the configured 18 the configured lanes. commands shall be 21
	1) TxCMD = SendTS2 (minimum of 16 TS2s)	22
	2) RxCMD = WaitTS2	23
	3) LinkPhyStat = Down	25
	4) TS2 and SKIP ordered-sets are transmitted on co	onfigured lanes only 26
	5) The port SymbolErrorCounter is enabled.	27
	6) If the RxStatus = RcvdTS2, the next state is Reco	overy.Idle.
	7) Else if DelayTimeOut(2ms)	30
	a) The <i>LinkDownedCounter</i> is incremented	31
	b) The <i>LinkRoundTripLatency</i> value is reset to	$0 \text{ 0xFFFF FFFF} = \frac{32}{32}$
	c) The next state is the LinkDownDefaultState (F	³⁰ ³⁰ ³⁰ ³⁰ ³⁰ ³⁰
5.6.4.8.3 RECOVERY.IDLE STATE		35
	 In the Recovery Idle state (Recovery.Idle), both ports the transmitter is commanded to send on the configure idle data. In the Recovery.Idle state, the following rule shall be active: 1) TxCMD = SendIdle (minimum of 16 symbol times) 	have retrained, and red lanes. The re- d lanes waiting for ⇒s and commands 40 41 () 42

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	2) RxCMD = WaitIdle	4
	3) LinkPhyStat = Down	1
	4) Idle Data and SKIP ordered-sets are transmitt only.	ed on configured lanes 3
	5) The port SymbolErrorCounter is enabled.	5
	6) If RxStatus = RcvdIdle,	6
	a) The <i>LinkErrorRecoveryCounter</i> is increm	mented 8
	b) The next state is LinkUp.	9
	7) Else If DelayTimeOut(2ms),	10
	a) The <i>LinkDownedCounter</i> is incremented	11
	b) The <i>LinkRoundTripLatency</i> value is rese	et to 0xFFFF FFFF 13
	c) The next state is the LinkDownDefaultStat	e (Polling or Sleeping) 14
5.6.5 STATE MACHINE DELAYS	AND TIMEOUTS	1
	Operations in certain states involve delays or time	e-out periods. These
	time-out periods start as the state is entered and a	re cleared when a tran-
	Sition to a different state is taken.	19
	C5-10: All ports shall use the delays and tolerand <u>Section 5.6.5, "State Machine Delays and Timeou</u>	ces defined in20ts." on page 147.21
	The delay timeouts used by the link training state r following tolerances:	22 nachine shall have the 23 24
	1) DelayTimeOut (2ms): 2ms (-1us/ +126us) 25
	2) DelayTimeOut (100ms): 100ms (-1us/ +126us) 20
	3) DelayTimeOut (150ms): 150ms (-1us/ +126us) 28
	4) DelayTimeOut (400ms): 400ms (-1us/ +126us) 29
	Note: The delay tolerances specified above do no	t include plus/minus
	100ppm allocated to the clock oscillator. The two tive (delay telerance + oscillator telerance)	tolerances are cumula-
		33
5.6.6 TRANSMITTER INTERFACE	AND BEHAVIOR	34
	The link training state machine controls the transmost of transmitter commands (TxCMD). The transmost as TxStatus. The expected behavior of each common following paragraphs.	nitter behavior using a mitter reports its status nand is specified in the 33
	C5-11: All ports shall implement the transmitter b <u>Section 5.6.6, "Transmitter Interface and Behavio</u> not required to implement the optional lane revers	ehaviors defined in <u>r," on page 147</u> but are sal function. 33 40 41 42 44 44 44 44 44 44 44 44 44

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	o5-3: All ports that implement the optional lane reimplement the behavior as defined in <u>Section 5.6.6.6</u> <u>Lanes," on page 150</u> .	versal function shall <u> <u> </u> , "TxCMD = Rev-</u> 2 3
5.6.6.1 TXCMD = DISABLE		4
	When transmit command is "disabled", the transmitter all physical lanes shall be driven to a quiescent cond	er output signals on 6 dition. 7
5.6.6.2 TxCMD = SENDTS1		8
	The SendTS1 command instructs the transmitter to a training sequence one ordered-sets (TS1). When co TS1 ordered-sets, the transmitter shall implement the	send a sequence of 9 mmanded to send 10 ne following rules: 11
	 The first TS1 ordered-set shall be transmitted at ordered-set or symbol boundary. The packet curr mitted may be terminated abnormally to send TS trigger error recovery. 	the next available rently being trans- 14 51 ordered-sets that
	2) The first TS1 ordered-set transmitted should for running disparity in all lanes to the same value (p	ce the current 17 positive or negative)
	 The SKIP ordered-sets have the highest transmir scheduled, a SKIP ordered-set shall be transmit dered-set boundary 	t priority. When 19 ted at the next or-
	4) Complete TS1 ordered-sets shall be transmitted long as the SendTS1 command is active.	back-to-back as
	5) At a minimum, sixteen (16) TS1 ordered-sets sh	all be transmitted. 24
	6) In the Polling and Configuration Super States:	25
	 a) The SKIP ordered-sets shall be transmitted or cal lanes. 	on all enabled physi-
	b) The TS1 ordered-sets shall be transmitted o cal lanes.	n all enabled physi-
	7) In the Recovery Super State:	30
	 a) The SKIP ordered-sets shall be transmitted ophysical lanes. 	only on configured 32
	 b) The TS1 ordered-sets shall be transmitted o physical lanes. 	nly on configured 34 35
	 c) Lanes not included in the configured link widt forced to a quiescent condition. 	h (unused) shall be 36 37
5.6.6.3 TxCMD = SENDTS2		38
	The SendTS2 command instructs the transmitter to a training sequence two ordered-sets (TS2). When con TS2 ordered-sets, the transmitter will implement the	send a sequence of mmanded to send following rules.

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	1)	The first TS2 ordered-set shall be transmitted at the ordered-set boundary.	next available	1
	2)	Complete TS2 ordered-sets shall be transmitted bac long as the SendTS2 command is active.	k-to-back as	2 3 4
	3)	At a minimum, sixteen (16) TS2 ordered-sets shall b	e transmitted.	5
	4)	The SKIP ordered-sets have the highest transmit prices scheduled, a SKIP ordered-set shall be transmitted a packet or ordered-set boundary.	ority. When at the next	6 7 8
	5)	In the Config.WaitRmt and Config.TxRevLane States	:	9
		a) The SKIP ordered-sets shall be transmitted on a cal lanes.	ll enabled physi-	1
		b) The TS2 ordered-sets shall be transmitted on all cal lanes.	enabled physi-	1
	6)	In the Recovery.WaitRmt, the Config.WaitRmtTest, a Config.WaitCfgEnhanced State:	nd the	1
		a) The SKIP ordered-sets shall be transmitted only physical lanes.	on configured	1
		b) The TS2 ordered-sets shall be transmitted only of physical lanes.	on configured	1
		c) Lanes not included in the configured link width (u forced to a quiescent condition.	nused) shall be	2 2
5.6.6.4 TXCMD = SENDTS3				2
	Th tra TS	e SendTS3 command instructs the transmitter to send ning sequence three ordered sets (TS3). When comm 3 ordered-sets, the transmitter will implement the follo	a sequence of nanded to send owing rules:	2 2 2 2
	1)	The first TS3 ordered set shall be transmitted at the ordered-set boundary.	next available	2
	2)	Complete TS3 ordered sets shall be transmitted bac long as the SendTS3 command is active.	k-to-back as	3 3 3
	3)	At a minimum, sixteen (16) TS3 ordered sets shall b	e transmitted.	3
	4)	The SKIP ordered sets have the highest transmit prices scheduled a SKIP ordered set shall be transmitted at or ordered set boundary.	prity. When the next packet	3 3 3 3
	5)	The SKIP ordered-sets shall be transmitted on all er lanes.	nabled physical	3 3
	6)	The TS3 ordered-sets shall be transmitted on all enallanes.	abled physical	4 4 4

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5.6.6.5 TxCMD = SENDIDLE		1
	The SendIdle command instructs the transmitter to send the link idle data sequence. When commanded to send idle data, the transmitter shall im-	2
	plement the following rules.	3
	 The SKIP ordered-sets have the highest transmit priority. When scheduled, a SKIP ordered-set shall be transmitted as soon as pos- sible by interrupting link idle data sequence transmission. 	5 6 7
	 The SKIP ordered-sets shall be transmitted only on configured physical lanes. 	8 9
	 The link idle data sequence shall be transmitted only on configured physical lanes. 	10 11
	 Lanes not included in the configured link width (unused) shall be forced to a quiescent condition. 	12 13
	5) At a minimum, sixteen (16) symbols times of link idle data shall be transmitted on each physical lane.	14 15 16
5.6.6.6 TxCMD = RevLanes		17
	The Reverse Lanes command is an optional modifier to the SendTS2 command. The RevLanes command instructs the transmitter to reverse he order of its transmit lanes. When commanded to reverse lanes, the ransmitter shall implement the following rules.	18 19 20 21
	1) The operation of the SendTS2 command shall not be interrupted.	22
	 The lane swap shall not cause the remote receiver to detect an error. 	23 24
	3) Four wide (4x) port shall reverse lanes causing the following lane swaps: 0 to 3, 1 to 2, 2 to 1, and 3 to 0.	25 26 27
	4) Eight wide (8x) port shall reverse lanes causing the following lane swaps: 0 to 7, 1 to 6, 2 to 5, 3 to 4, 4 to 3, 5 to 2, 6 to 1, and 7 to 0.	28 28 29
	5) Twelve wide (12x) port shall reverse lanes causing the following lane swaps: 0 to 11, 1 to 10, 2 to 9, 3 to 8, 4 to 7, 5 to 6, 6 to 5, 7 to 4, 8 to 3, 9 to 2, 10 to 1, and 11 to 0.	30 31 32
5.6.6.7 SPEED = MAXBOTHACTIV	E	33
	This command configures the transmitter to transmit data at the maximum rate commonly enabled on both ports of the link that is also supported by he link medium.	34 35 36
5.6.6.8 SPEED = MINENABLEDS	EED	37
	This command configures the transmitter to transmit data at the minimum speed enabled on the port, generally the SDR rate.	38 39 40

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5.6.6.9 TXCMD = ENABLE

This command enables the normal operation condition of the transmitter. 2 When enabled, the transmitter will implement the following rules. 3

1) The transmission of SKIP ordered-sets, link heartbeats, packets, and link idle data **shall** be restricted to the configured link width.

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- 2) Physical lanes not included in the configured link width (unused) shall be forced to a quiescent condition.
- 3) SKIP ordered-sets have the highest transmit priority. When scheduled, a SKIP ordered-set shall be transmitted as soon as possible at the next packet boundary, at the next ordered-set boundary, or by interrupting link idle transmission.
- On ports that implement Rel. 1.2 Enhanced Signaling capability, Link Heartbeat Ordered-Sets have the second highest transmit priority. When a Link Heartbeat ordered-set is available for transmission, it shall be transmitted as soon as possible at the next packet boundary, at the next ordered-set boundary, or by interrupting link idle transmission.
- 5) Packets have the next highest transmit priority. When a packet is available for transmission, it shall be transmitted as soon as possible at the next packet boundary, at the next ordered-set boundary, or by interrupting link idle transmission.
- 6) When there are no SKIP ordered-sets, link heartbeats, or packets to transmit, the transmitter **shall** transmit the link idle data pattern.

5.6.7 RECEIVER INTERFACE AND BEHAVIOR

The link training state machine controls the receiver behavior using a set of receiver commands (RxCMD). The receiver reports its status as Rx-Status. The expected behavior of the receiver in response to each command is described in the following paragraphs. Receiver status conditions 28 are defined as part of receiver command definition. 29

C5-12: All ports shall implement the Receiver behaviors defined in 31 Section 5.6.7. "Receiver Interface and Behavior." on page 151 but are not 32 required to implement the optional lane reversal function or correction of 33 inverted serial data. 34

o5-4: All ports that implement the optional correction of inverted serial data shall implement the behavior as defined in Section 5.6.7.3, "RxCMD = EnConfig," on page 152 rule 2.

05-5: All ports that implement the optional lane reversal function shall implement the behavior as defined in Section 5.6.7.3, "RxCMD = En-Config," on page 152 rule 4.

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5.6.7.1 RXCMD = DISABLE When the receiver is disabled, the receiver shall implement the following 2 rules: 3 4 1) The receiver shall not forward packets to the upper layer protocols. 5 2) The receiver **shall not** update the port error counters. (See Section 6 5.4.3 on page 110) 7 8 5.6.7.2 RxCMD = WAITTS1 9 This command instructs the receiver to look for TS1 on all physical lanes 10 independently. When commanded to WaitTS1, the receiver shall imple-11 ment the following rules. 12 13 1) Symbol synchronization **shall** be enabled on all lanes. 14 2) The receiver status shall be RcvdTS1 when at least one complete 15 and error free TS1 or TS2 ordered-set is detected in one or more 16 physical lanes. 17 3) The training sequence ordered-set lane number shall not be 18 checked. 19 5.6.7.3 RxCMD = ENCONFIG 20 21 When the receiver is commanded to enable auto-configure, the receiver 22 will attempt to configure the port as restricted by port capability and by capabilities enabled by management commands (See Section 5.4.1 on page 23 105). When commanded to enable auto-configure, the receiver will imple-24 ment the following rules: 25 26 1) The receiver **shall** only attempt to configure the link to speeds en-27 abled by the LinkSpeedEnabled variable. (Auto-configuration of link 28 speed is supported under Rel. 1.2 Enhanced Signaling, but not supported by legacy devices). 29 30 2) The receiver **may** optionally correct inverted receiver data. 31 3) The receiver **shall** verify proper lane polarity using the training se-32 quence data (symbols 3 through 16 of both TS1 and TS2) in the re-33 ceived training sequence. If the lane polarity is not correct (or cannot 34 be corrected), the receiver shall not report RxTrained. 35 4) The receiver **may** optionally correct reversed lanes. 36 5) The receiver **shall** verify proper lane order using the lane number 37 symbol (the second symbol in both TS1 and TS2) in the received 38 training sequence. If proper lane ordering is not present (or cannot be 39 corrected), the port shall not report RxTrained. 40 6) The receiver **shall** only attempt to configure the link to widths en-41 abled by the LinkWidthEnabled variable.

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	a)	When the 12x width is enabled, the receiver sha synchronization on twelve physical lanes (11-0) that all twelve lanes are receiving TS1 or TS2 or	II attempt symbol and shall verify rdered-sets.	1 2
	b)	When the 8x width is enabled, the receiver shal synchronization on eight physical lanes (7-0) and all eight lanes are receiving TS1 or TS2 ordered	I attempt symbol d shall verify that I-sets.	3 4 5 6
	c)	When the 4x width is enabled, the receiver shal synchronization on four physical lanes (3-0) and all four lanes are receiving TS1 or TS2 ordered-	I attempt symbol I shall verify that sets.	7 8 0
	d)	When the 1x width is enabled, the receiver shal synchronization on physical lane (0) and shall v ceiving TS1 or TS2 ordered-sets.	I attempt symbol rerify that it is re-	9 10 11
	7) Tł pl wi	ne receiver shall use widest enabled and verified I etion of link training and report that width as the co idth.	ink width for com- onfigured link	13 14 15
	8) Th er	ne receiver shall use the sixteen symbol long TS1 ence for link de-ske <mark>w operatio</mark> ns.	or TS2 as ref-	16 17
	9) Th sy	ne receiver shall be capable of de-skewing a mini mbol times of total link skew.	mum of six	18 19
	10) Af cc by re	ter successful link de-skew, the receiver shall reconsecutive error free TS1 or TS2 (all TS1, all TS2 (TS2) ordered-sets simultaneously on all configur porting RxTrained status.	eive eight (8) or TS1 followed ed lanes before	20 21 22 23
5.6.7.4 RxCMD = ENDESKEW				24
	When follow	the receiver is commanded to enable de-skew, it v ing rules:	vill implement the	26 27
	1) Th er	ne receiver shall use the sixteen symbol long TS1 nce for link de-skew operations.	or TS2 as refer-	28 29 30
	2) Tł sy	ne receiver shall be capable of de-skewing a mining mining a mi	mum of six	31 32
	3) Af cc by re	ter successful link de-skew, the receiver shall rec onsecutive error free TS1 or TS2 (all TS1, all TS2 v TS2) ordered-sets simultaneously on all configur porting RxTrained status.	eive eight (8) or TS1 followed ed lanes before	33 34 35 36
5.6.7.5 RxCMD = WAITTS2				37
	This c mote transr ceiver	command instructs the receiver to confirm configure port. When the remote port configures its receiver nit TS2 ordered-sets. When commanded to wait for r shall implement the following rules:	ration of the re- ; it starts to or TS2, the re-	39 40 41 42

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	1)	The receiver shall ignore data on the lanes the configured link width (unused).	that are not included in	1
	2)	The receiver shall ignore properly formatted sets.	TS1 and SKIP ordered-	2 3 4
	3)	The receiver shall receive eight (8) consecu properly lane ordered TS2 or TS3 ordered-se configured lanes before reporting RcvdTS2 s	tive error free and ets simultaneously on all status.	5 6 7
5.6.7.6 RxCMD = WAITTS3				8
	The spe cei to v	e WaitTS3 command instructs the receiver to deed of the remote port. When the far port has ving idle data it starts to transmit TS3 ordered-wait for TS3, the receiver shall implement the	determine the advertised finished sending and re- sets. When commanded following rules:	9 10 11 12
	1)	The receiver shall ignore data on lanes that configured link width (unused).	are not included in the	13 14 16
	2)	The receiver shall receive eight (8) consecu dered sets simultaneously on all configured RcvdTS3 status.	tive error free TS3 or- lanes before reporting	16 16 17 18
	3)	The receiver shall ignore error free idle data	and SKIP ordered-sets	19
	4)	The Receiver shall compare the link speed is ceived TS3 ordered-sets with the link speed transmitted TS3 ordered-sets. The highest c saved and passed to the transmitter for use further data.	ndicator from the re- indicator from the links ommon speed will be in the transmission of	20 21 22 23
5.6.7.7 RxCMD = WAITIDLE				24 25
	Thi sha cor idle sha	s command instructs the receiver to confirm reake necessary to complete the link training pro offirms proper configuration of the near port, it data pattern. When commanded to wait for i all implement the following rules:	eception of the final hand- ocess. When the far port starts to transmit the link dle data, the receiver	26 27 28 29 30
	1)	The receiver shall ignore properly formatted sets.	TS2 and SKIP ordered-	31 32
	2)	The receiver shall assert Rcvdldle after rece error free symbol times of link idle data seque lanes (i.e. eight (8) per lane).	ption of at least eight (8) ence on all configured	33 34 35
5.6.7.8 RXCMD = ENABLE				30 37
	Thi imp	s command enables the normal receiver ope plement the following rules:	ration. The receiver will	38 39
	1)	Received packets shall be transferred to the tocol (link layer).	e upper layers of the pro-	40 41 42

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	2) Link error detection shall be enabled. (See Section 5	.7 on page 156)	
	3) If Rel. 1.2 Enhanced Signaling capabilities are impler	nented, 2)
	a) detection of Heartbeat SND Ordered Sets shall b	e enabled, and 3	;
	b) detection of Heartbeat Errors shall be enabled.	4	
5.6.7.9 RxCMD = WAITTS-T		5	
	This command enables the receiver to detect the TS-T or receiver will implement the following rules:	rdered set. The 7 8	
	 The receiver status shall be RcvdTS-T when at least and error free TS-T ordered-set is detected in one or lanes. 	one complete 9 more physical 1	C 1
5.6.7.10 RxStatus = RcvdTS1		1:	2
	The received TS1 status is valid at any time TS1 is received status PovdTS1 is defined in Section 5.6.7.2 "PxCMD =	ed. The receiver	4
	page 152.	1:	5
		1	6
5.0.7.11 KASTATUS = KATRAINEI	The receiver trained status is valid only when the RxCMF) is EnConfig or 1	7 8
	EnDeSkew. The receiver status RxTrained is defined in $\frac{1}{5}$ "RxCMD = EnDeSkew," on page 153.	Section 5.6.7.4. 11	9
5.6.7.12 RXSTATUS = RCVDTS2		2	1
	The received TS2 status is valid at any time TS2 is received status RcvdTS2 is defined in <u>Section 5.6.7.5, "RxCMD = page 153</u> .	ed. The receiver 2 <u>WaitTS2," on</u> 2	23
5.6.7.13 RxStatus = RcvdTS3		2	:6
	The received TS3 status is valid only when the RxCMD is receiver status RcvdTS3 is defined in <u>Section 5.6.7.6. "R</u> <u>WaitTS3," on page 154</u> .	s WaitTS3. The 2 <u>xCMD =</u> 2 2	7 8 9
5.6.7.14 RxStatus = RcvdTS-1	-	3	0
	The received TS-T status is valid only when the RxCMD is receiver status RcvdTS-T is defined in <u>Section 5.6.7.9, "F</u> <u>WaitTS-T," on page 155</u> .	s WaitTS-T. The 3 RxCMD = 3	233
5.6.7.15 RXSTATUS = ROVDIDIE		3	5
	The received idle status is valid when the RxCMD is Waitle	dle and in states $\frac{3}{3}$	6
	where a received Idle causes a state transition. The rece dIdle is defined in <u>Section 5.6.7.7</u> , "RxCMD = WaitIdle," of	iver status Rcv- ³ on page 154. ³	8
		3	9
		4	.1
		4	2

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5.6.7.16 RxStatus = RxMajorError					
	Receiver Major Error status can be asserted by ceiver status RxMajorError is defined in <u>Section</u> ical Errors Events," on page 158.	r multiple sources. The re- <u>1 5.7.4. "Major Link Phys-</u> 3 4			
5.6.7.17 RxStatus = RxHeart	BEATERROR	5			
	Receiver Heartbeat Error status can be asserted receiver status RxMajorError is defined in <u>Section Error Handling," on page 168</u> .	d by multiple sources. The ⁶ ion 5.11.2. <u>"Heartbeat</u> 7 8			
5.7 LINK PHYSICAL ERROR HA	NDLING	9			
	This section describes link error detection and l mented in the Link/Physical layer.	link error recovery imple- 11 12			
	The Link/Physical layer does not interpret pack framing, or CRCs. These errors are detected at described in Volume 1.	et payloads, packet t the Link Layer Protocol 15 16			
	C5-13: All ports shall implement link physical er <u>Section 5.7, "Link Physical Error Handling." on</u>	rror handling as defined in 17 page 156. 18			
5.7.1 LINK PHYSICAL ERRORS	Events	19 20			
	Link/Physical errors stem from two fundamental and protocol violations. Bit errors may appear a tions, running disparity violations, or incorrect be groups. Bit errors which result in incorrect but v detected as protocol errors or as CRC errors wh layers of the protocol. Burst errors may severel groups on one or more lanes. These major error tiple coding violations, protocol errors, loss of lar of symbol synchronization. Protocol errors may errors, or they may be the result of some other errors are handled in several basic ways:	I sources: link bit errors as 8B/10B coding viola- but valid 8B/10B code valid code groups may be then checked by the upper y corrupt multiple code r events may result in mul- the to lane de-skew, or loss be the result of simple bit event. Receiver-detected 30			
	 Minor error events which do not significantly layer processing shall be marked and forward When minor error events occur simultant 	y impact link/physical 32 arded to the upper layers. 32 33 34			
	they shall be treated as a single minor e	error event. 36			
	 Major error events shall result in a link erro link/physical error recovery. 	r event which triggers 38			
		40			

The error threshold logic described in <u>Section 5.7.3 on page 157</u> monitors minor error events and may trigger a major event if the rate is too high.

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5.7.2 MINOR LINK PHYSICAL ERRORS EVENTS

	Mir <u>tior</u> tior	nor error events are input to the error threshold logic described in <u>Sec-15.7.3 on page 157</u> and to the SymbolErrorCounter described in <u>Sec-15.4.2</u> . The following errors are counted as minor error events:	2 3 4 5
	1)	Invalid 8B/10B codes groups and running disparity errors shall be counted as minor error events. (See <u>Section 5.2</u>).	6 7
	2)	Unsupported or disabled valid code groups shall be counted as minor error events. (See <u>Section 5.3.1.8</u> and <u>Section 5.3.1.9</u>).	8 9 10
	3)	Start or End Packet Delimiter in the wrong lane of a multi-lane link shall be counted as a minor error event. (See <u>Section 5.5.4</u> , <u>Section 5.5.5</u> , and <u>Section 5.5.6</u>).	11 12 13
	4)	Any control symbol within the boundaries of a packet shall be counted as a minor error event.	14 15 16
	5)	PAD symbols on a non-12x and non-8x link shall be counted as minor error events. (See <u>Section 5.5.5</u> and <u>Section 5.5.6</u>).	17 18 19
	6)	On an 8x or 12x link, PAD symbols not preceded by a End of Packet Delimiter shall be counted as minor error events. PAD symbols in the wrong lane shall also be counted as minor error events. (See <u>Section</u> 5.5.5, <u>Section 5.5.6</u> and <u>Section 5.10.3</u>)	20 21 22 23 24 25
5.7.3 LINK PHYSICAL ERROR T	HRE	SHOLD ALGORITHM	26 27
	To an def	detect an excessive number of minor errors (see <u>Section 5.7.2</u> above), error threshold algorithm is implemented. The threshold shall be set to sect an error rate of four (4) or more minor errors within sixteen (16) modultimes. Both the "leaky bucket algorithm" and "sliding window algo-	28 29 30 31

symbol times. Both the "leaky bucket algorithm" and "sliding window algo-32 rithm" implementations are sufficient. The error threshold function will im-33 plement the following rules:

- 35 1) The error threshold shall be enabled only when the link training state 36 machine is in the LinkUp state. 37
- 2) The error threshold shall be disabled and cleared when the link training state machine is not in the LinkUp state.

40 The following implementation notes describe leaky bucket and sliding 41 window error threshold algorithms. 42

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Implementation Note:

The error threshold counter which employs the "leaky bucket algorithm" **should** implement with the following rules:

- 1) When a minor error is detected, the error threshold counter is incremented.
- 2) The error threshold counter is decremented every sixteen (16) symbol times.
- 3) The decrement event may be a free-running symbol time counter that is not synchronized to any specific link state or error condition.

An error threshold event will be reported when the error threshold counter is value is four (4) or greater.

Implementation Note:

The error threshold counter which employs the "sliding window algorithm" **should** implement with the following rules:

- 1) Logic tracks the minor error status of the most recent 16 symbol times.
- An error threshold event will be reported when four (4) or more minor errors are present in the in the most recent 16 symbol time of history

5.7.4 MAJOR LINK PHYSICAL ERRORS EVENTS

Major error events trigger the link error recovery process of the Link30Training State Machine. These error events are not counted directly. How-
ever, successful error recovery attempts are counted by the LinkErrorRe-
coveryCounter and failed error recovery attempts are counted by the
LinkDownedCounter. Both counters are defined in Section 5.4.3, "Port
Performance Counters," on page 110. The following errors events will
start the link error recovery process:30

- Training Sequence one or two (TS1 or TS2) received in the linkup state shall trigger link error recovery. (TS1 indicates that the remote port has initiated the link error recovery process)
- 2) The assertion of LinkPhyRecover from the Link Layer **shall** trigger link error recovery.

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	3)	Loss of symbol(s) caused by elastic buffer overflow shall trigger link error recovery.	v or underflow	1
	4)	The absence of 4 expected SKIP ordered-sets sho error recovery.	ould trigger link	2 3 4
	5)	Clear loss of lane-to-lane de-skew should trigger l	link error recovery.	5
	6)	A minor error threshold event should trigger link e	rror recovery.	6
5.7.5 HEARTBEAT ERROR				7 8
	A I Lir D o	Heartbeat Error error event triggers a transition to the the Training State Machine. These error events are co bwnedCounter . The following error event is a Heart	default state in the ounted by the <i>Link</i> - beat Error event:	9 10 11
	•	4 HEARTBEAT transmission periods (8 ms) elapse valid HEARTBEAT ACK ordered-sets simultaneous lanes.	e without receiving sly on all active	12 13 14
	Th <u>Se</u> va	e characteristics of a valid HEARTBEAT ordered-se action 5.3.2.5, "Link Heartbeat Ordered-Set (HRTBT lid Link Heartbeat ordered-set has the following cha	et are described in <u>)." on page 101</u> . A racteristics:	15 16 17
	•	Error-free reception of 8b/10b symbols on all config	gured lanes.	18 10
	•	Lane IDs match the lanes on which they were rece	eived.	20
	•	Opcode of either 5Dh (SND) or ACh (ACK).		21
	•	Received GUID on a SND HRTBT that doesn't ma port's own GUID. Matching SND GUID is interprete ter/receiver crosstalk on SND transmission from a the same device.	tch the receive ed as transmit- port transmitter on	22 23 24 25
	•	Received GUID and PortNum on an ACK HRTBT receive port's own GUID and PortNum. Mismatche Portnum is interpreted as transmitter/receiver crost transmission.	that matches the ed ACK GUID and stalk on ACK	26 27 28 29
5.8 INTERNAL SERIAL LOOPBA	ск			30
	Th Int wit	e Internal Serial Loopback is optional and is not req ernal serial loopback allows a port to receive its trans hout the need for external support. The internal seria intended for self-test and fault isolation use only.	uired on all ports. mitted data stream I loopback function	31 32 33 34 35
	o5 me	-6: All ports that implement internal serial loopback ent it as defined in <u>Section 5.8, "Internal Serial Loopb</u>	option shall imple- back." on page 159.	36 37
	Th	e following rules apply to the internal serial loopbac	k:	38 39
	1)	When disabled, the internal serial loopback shall h port operation.	nave no effect on	40 41 42

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	2)	When enabled, internal serial loopback shall connect the transmit serial data output to the receive serial data input as close to the chip I/O cells as is practical.	
	3)	When internal serial loopback is enabled, the receive data from the receiver input pins shall be blocked.	
	4)	When internal serial loopback is enabled, the chip's transmitter output pins shall be forced to a quiescent condition.	
5.9 CLOCK TOLERANCE COMP	ENS	ATION	
	Ea lize tig ree str ree oth	ich end of a 1x link (or each physical lane on 4x, 8x and 12x links) uti- es a transmitter and a receiver. The transmitter logic operates using a htly controlled reference clock called the "transmit clock". Likewise, the ceiver logic operates using a clock recovered from the incoming bit ream called the "receive clock". Once the link is trained, the recovered ceive clock operates at the same frequency as the transmit clock at the her end of the link.	
	Th Ta tra fre cu at wc pe	The UI _D parameter in <i>InfiniBand Architecture Specification</i> , <u>Volume 2</u> , <u>ble 17 Driver Characteristics for 2.5 Gb/s on page 185</u> specifies the insmit clock accuracy as +/- 100 ppm (parts per million). The worst-case equency difference between the transmit and receive clocks of a link ocris when one of the transmitters is at the +100 ppm and the other one is the -100 ppm tolerance, resulting in a 200 ppm difference. In other ords, the transmit and receive clocks can shift by as much as one clock eriod every 5000 clocks.	
	A o tra the for dro in clo	common design practice is to clock most of the receive path logic in the insmit clock domain. This is accomplished by using an "elastic buffer" in a very early stages of the receive path. The elastic buffer compensates the differences between the transmit and receive clock domains by opping or inserting symbols. The input side of the elastic buffer operates the receive clock domain, and the output side operates in the transmit ock domain.	
	To sa Th	perform the compensation function, the elastic buffer needs to identify fe zones in the incoming symbol sequence to insert or drop a symbol. is zone is provided by the "SKIP ordered-set".	
	C5 in	5-14: All ports shall implement clock tolerance compensation as defined <u>Section 5.9, "Clock Tolerance Compensation," on page 160</u> .	
5.9.1 TRANSMITTER "SKIP" REQUIREMENTS			

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The transmitters are required to transmit SKIP ordered-sets periodically, 40 complying with the following rules: 42

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	 The SKIP ordered-set shall be scheduled for in every 4608 symbol times. 	sertion at least once 1
	 The SKIP ordered-set shall be scheduled for in every 4352 symbol times. 	sertion at most once 3
	3) A scheduled SKIP ordered-set shall be inserted ordered-set boundary.	t at the next packet or $\begin{bmatrix} 5 \\ 6 \\ 7 \end{bmatrix}$
5.9.2 RECEIVER "SKIP" REQU	REMENTS	8
	The receivers are required to receive and process s riodically, complying with the following rules:	9 SKIP ordered-sets pe- 10 11
	 The receivers shall recognize received SKIP of comprised of one (1) comma (COM) symbol fol five (5) skip (SKP) symbols. 	rdered-sets that are lowed by one (1) to
	2) The receivers shall be tolerant to receive and p sets at an average rate of once in every 4352 to	rocess SKIP ordered- 16 0 4608 symbol times. 17
	3) The receivers shall be tolerant to receive and p sets separated from each other at least 128 syr sured as the distance between the leading com	rocess SKIP ordered- nbol times mea- ma (COM) symbols.
	4) The receivers shall be tolerant to receive and p sets separated from each other at most 8832 sy sured as the distance between the leading com	rocess SKIP ordered-22 /mbol times mea-23 ma (COM) symbols.22
5.10 RETIMING REPEATERS		25
	The InfiniBand TM Architecture allows for the use of " recover from potentially weakened signal strength a tween two end nodes of a link.	retiming repeaters" to and built-up jitter be-
	There are two types of retiming repeater: "SKIP or retiming repeaters, which use the SKIP ordered-set quency difference, and "transparent" retiming repea pend on or use the SKIP ordered-set, but operate a frequency for both transmission and reception.	dered-set dependent" to compensate for fre- iters, which do not de- at a single common 34
	This section describes, in general, the operation of pendent retiming repeaters, except where transpare are specifically mentioned. Both types of retiming remeet the signaling requirement specified in (<i>InfiniBa ification</i> , <i>Volume 2</i> , Chapter 6: High Speed Electrica & 10.0 Gb/s).	SKIP ordered-set de- ent retiming repeaters 38 peater reset jitter and 39 and Architecture Spec- al Signaling - 2.5, 5.0, 42 42

Implementation Note:

The major difference between the two types of retiming repeaters is in whether the retiming repeater uses an internal clock, or uses a clock recovered from the received data stream, for transmitting the repeated data. A SKIP ordered-set dependent retiming repeater will typically have its own internal clock, with the usual +/- 100 ppm frequency tolerance, and may need to insert or remove SKIP symbols to compensate for frequency differences with the originating port. A transparent retiming repeater will typically transmit the repeated data using a clock recovered from the received data.

Transparent retiming repeaters will typically be more generally useful, since they are not dependent on the specific InfiniBand link/phy protocol's use of the SKIP ordered-set.

C5-15: All retiming repeaters **shall** implement functions as defined in <u>5.10: Retiming Repeaters</u>.

The following general rules apply to retiming repeaters:

- 1) Retiming repeaters **shall** reset the jitter budget.
- 2) Not more than two SKIP ordered set-dependent retiming repeaters **shall** be allowed between two protocol-aware ports.
- 3) Retiming repeaters **may** join dissimilar physical media such as copper-to-fiber optic links.
- 4) Retiming repeaters are not in-band-addressable devices. Hence they cannot be managed through in-band management messages.

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5.10.1 RETIMING REPEATER FUNCTIONS

Figure 29 below depicts a block diagram of a conceptual retiming repeater. This figure is provided as a visual aid to help explain the fundamental functions of retiming repeaters.



Figure 29 A Conceptual Retiming Repeater Block Diagram

Retiming repeaters are fairly simple devices. A 1x retiming repeater con-21 sists of two ports. It simply transmits every symbol received on one port to the other port. The receiver circuitry on each port operates from its own recovered receive clock (Rx Clock) domain. However, the transmit circuitry operates on a locally generated transmit clock (Tx Clock) domain, which may have a different frequency than the frequency of the incoming data. In order to compensate for the differences in the receive and transmit clock domains, elastic buffers are used in each direction. Transparent retiming repeaters transmit the data using the clock recovered from the received data, and have less requirement for elastic buffers.

Retiming repeaters are not link-protocol-aware devices. In other words, they do not recognize link and data packets. However, SKIP ordered-set dependent retiming repeaters do recognize two kinds of ordered-sets in the incoming symbol stream:

- SKIP ordered-set
- TS1 and TS2 Training Sequence ordered-sets

SKIP ordered-sets are both recognized in the incoming symbol stream 39 and used in the elasticity operations performed in each direction. Elasticity 40 operations performed by the retiming repeaters are specified in Section 41 5.10.2 later in this chapter. 42

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During Link Training, repeated training sequence ordered-sets are transmitted between two end points. Repeaters use the periodic comma (COM) symbols in this stream to detect symbol boundary misalignment.

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5.10.2 CLOCK TOLERANCE COMPENSATION

SKIP ordered-set dependent retiming repeaters perform clock tolerance compensation during SKIP sequences. The SKIP sequence -- as observed by repeaters -- is comprised of one comma (COM) symbol followed by two to four skip (SKP) symbols. Repeaters are allowed to insert or delete one skip symbol in this ordered-set in order to compensate for the differences between the receive and transmit clock frequencies.

SKIP ordered-set dependent retiming repeaters **shall** use the following rules to insert or delete a skip symbol in a SKIP ordered-set:

- When necessary, the retiming repeaters shall insert a skip (SKP) symbol after the comma (COM) symbol within the current SKIP ordered-set.
- When necessary, the retiming repeaters shall delete any skip (SKP) symbol after the comma (COM) symbol in the current SKIP orderedset.

5.10.3 ERROR HANDLING CONSIDERATIONS

Retiming repeaters **shall not** check for code violations (i.e. decode and disparity errors). Symbols received on one port with or without transmission errors are simply transmitted by the other port.

The elastic buffers are not expected to underflow or overflow. However, when these conditions are detected, these rules apply:

- 1) When an underflow condition is detected, the retiming repeaters **shall** insert a pad (PAD) symbol.
- When an overflow condition is detected, the retiming repeaters shall replace two arbitrary but consecutive symbols with a pad (PAD) symbol.

5.10.4 SYMBOL BOUNDARY ALIGNMENT

When protocol-aware nodes detect link errors (including loss-of-symbol synchronization), they initiate error recovery (see <u>Section 5.7 on page</u> <u>156</u>) by sending training sequences that contain the commas needed for symbol synchronization. Retiming repeaters cannot initiate training sequences on their own. Instead, they detect periodic unaligned comma (COM) symbols within this sequence to determine the loss-of-symbol boundary alignment.

The following rules define the symbol boundary alignment process used 41 by retiming repeaters:

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	1)	Periodic comma symbols (COM) in TS1, TS2 or shall be used to acquire symbol boundary synch	SKIP ordered-sets ronization.
	2)	SKIP ordered-set dependent retiming repeaters symbol boundary synchronization when three co aligned comma symbols are detected. A misalign is the 0011111 or 1100000 symbol pattern which of current symbol boundary.	shall reacquire nsecutive mis- ned comma symbol loes not begin at the
		• SKIP ordered-set dependent retiming repeate bit comma bit pattern 1100000 or 0011111 to rather than the full 10-bit comma symbol patt	ers may use the 7- acquire alignment, ern.
	3)	Retiming repeaters shall disable their symbol bo	undary synchroni-

symbols (COM) are detected.

5.10.5 MULTI-LANE REPEATER CONSIDERATIONS

Multi-lane retiming repeaters are used by multi-lane (4x, 8x and 12x) links. Like protocol aware ports, retiming repeaters are required to use a common clock source for all lanes in the link. The logic within a retiming repeater is not required to synchronize lane to lane operation. Multi-lane retiming repeaters can be shared by multiple links that use a subset of the retiming repeater's lanes. For example, a 4x retiming repeater can be used by up to 4 1x links. The 12x retiming repeater can be used by multiple combinations of 1x, 4x, and 8x links.

zation circuitry when five consecutive instances of aligned comma

The following rules apply to operation of multi-lane retiming repeaters:

- 1) For each direction all lanes of multi-lane retiming repeaters **shall** have a common transmit clock source.
- 2) The lanes in opposed directions **may** have independent transmit clock sources.
- 3) Each lane of multi-lane retiming repeaters **shall** operate independently of the other lanes.
- 4) Multi-lane retiming repeaters may implement lane to lane de-skew.

5.10.6 POWER STATE CONSIDERATIONS

The retiming repeaters are not protocol-aware devices. Hence they cannot be managed through in-band management packets. However, they are expected to be managed by either:

- 1) the Management Entity of the chassis of which they are part, or
- the Management Entity of the InfiniBand module of which they are part.

The retiming repeaters that are managed using one of these schemes are also said to be "proxy-managed."

During normal operation, a neighboring node may transition to $X_{Standby}$ or X_{Sleep} state. In these states, the node drives the link to "quiescent" state. Similarly, when the neighboring node transitions to the $X_{Polling}$ state, the link will be driven to its "quiescent" state periodically. Retiming repeaters are expected to detect the link going to "quiescent" state at its receiver on either side and to propagate this link "quiescent" state on the transmitter of the other side.

When the neighboring node transitions to X_{On} state, the link goes from "quiescent" to "active" state. Similarly, when the neighboring node transitions to the $X_{Polling}$ state, the link will transition from "quiescent" to "active" state periodically. The retiming repeaters are expected to detect this link state change on its receiver at either side and to propagate it to the transmitter on the other side.

Proxy managed retiming repeaters **shall** comply with power states and behavior defined in *InfiniBand Architecture Specification*, <u>Volume 2</u>, <u>Section 14.3</u>, "Port Power Management States," on page 641. Additionally, operation of the retiming repeaters when propagating "quiescent" and "active" link activity are governed by the following rules:

- 1) Retiming repeaters **shall** detect "quiescent" to "active" transition on one side and propagate that state to the other side within 100 microseconds.
- 2) Retiming repeaters **shall** detect "active" to "quiescent" transition on one side and propagate that state to the other side within 100 microseconds.

5.11 LINK HEARTBEAT

At the DDR and QDR link bit rates described for Rel. 1.2 Enhanced Signaling, the lower peak-to-peak received voltage and the consequent lack of a signal detect at the receiver results in higher vulnerability to crosstalk in the receiver logic. It is possible that if a link is disconnected while a port is in the LinkUp state a receiver may interpret crosstalk from its own transmitter as valid data and incorrectly maintain LinkUp status. The link heartbeat function ensures that received data actually originates from the opposite end of a link, rather than from crosstalk from the port's own transmitter.

Link Heartbeats are also used to determine link round-trip latency. Since InfiniBand[™] links use a variety of copper and optical physical layer transmission media, a link may be between a few inches and many kilometers long, causing a wide range of link latency values. Prior releases of the InfiniBand[™] specification allowed no straightforward way for the link layer logic or for a subnet manager to determine the round-trip latency across a link. Link Heartbeats allow the determination of link round-trip latency,

for helping to improve link management and bandwidth allocation algorithms, which is useful for SDR as well as for DDR & QDR link rates.

Implementation Note:

Knowledge of link lengths can be useful for link management functions, e.g., to tell whether optical transceivers or retiming repeaters are likely to be present. A 1 km link, for example, may be assumed to have an optical transceiver inserted, even though, since they are simple devices, and are not in-band-addressable, this information can't be determined using in-band management messages.

Knowledge of link lengths is also useful for congestion control and bandwidth maximization mechanisms, since a long link with high link latency may be throttled in bandwidth due to credit starvation if it is not allocated extra buffering and extra credits. A switch chip, for example, with a combination of long and short links on different ports and with a flexible buffering allocation capability, can move buffer space and credit allocation from a short link to a long link, maximizing usable bandwidth on both.

C5-15.2.1: All ports claiming compliance with InfiniBand Rel. 1.2 Enhanced Signaling **shall** implement link heartbeat functionality as defined by <u>Section 5.11, "Link Heartbeat," on page 166</u>, at all link speeds.

5.11.1 OPERATION OF LINK HEARTBEATS

Each port capable of Rel. 1.2 Enhanced Signaling operation will create regularly transmitted HEARTBEAT ordered-sets when connected to another capable port, at any link speed. A HRTBT ordered-set, described in <u>Section 5.3.2.5, "Link Heartbeat Ordered-Set (HRTBT)," on page 101</u> contains an OpCode identifying it as a SND HEARTBEAT or an ACK HEARTBEAT, along with information identifying its source.

A port schedules for transmission a Link Heartbeat with OpCode=5Dh, indicating SND, once every 100 milliseconds while the port is in the LinkUp state. The SND HEARTBEAT contains the sending port's base GUID and, if applicable, the sending port's switch port number. In the SND HEART-BEAT, the OpCode byte, is set to the value D29.2 (5Dh, encoded as 101110 0101 or 010001 0101).

Upon reception of a valid SND HEARTBEAT the port schedules an ACK (Acknowledge) HEARTBEAT for transmission at the next possible transmission time. The ACK heartbeat is sent with the GUID and switch port

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number contained in the SND heartbeat, i.e., these values are reflected back in the ACK HEARTBEAT ordered-set. In the ACK HEARTBEAT, the OpCode byte, the sixth byte in the ordered-set, is set to the value D12.5 (ACh, encoded as 001101 1010 or 001101 1010).

Upon reception of a valid ACK (acknowledge) HEARTBEAT, the port finds the difference in time between its original SND transmission and the ACK reception. This difference correlates to the link round-trip latency, which correlates to link length.

Both SND HEARTBEAT and ACK HEARTBEAT ordered-sets are transmitted on every active lane simultaneously (like SKP ordered-sets).

SND HEARTBEAT ordered-sets are scheduled once every 100 ms in LinkUp State, to match the minimum DelayTimeOut period. Transmitting this often incurs negligible bandwidth loss and provides prompt notification of changes in link integrity.

Transmission of Link Heartbeat ordered-sets interspersed with other packets and ordered-sets uses the priority scheme described in <u>Section 5.6.6.9</u>, "TxCMD = Enable," on page 151.

5.11.2 HEARTBEAT ERROR HANDLING

Heartbeat errors are detected under the conditions described in <u>Section 5.7.5, "Heartbeat Error," on page 159</u>.

Heartbeat errors indicate that a link has been disconnected, and should result in the Link Training State Machine returning to LinkDownDefault-State (Polling or Sleeping) with the *LinkDownedCounter* being incremented.

5.11.3 HEARTBEAT LATENCY CALCULATION AND REPORTING

Round-trip latency is measured as the time between the end of Heartbeat SND transmission and the end of reception of the corresponding Heartbeat ACK. The longest possible round-trip latency, over a 10 km. single-mode optical link, with roughly 5 ns/meter propagation speed, will be roughly 100 microseconds, and the shortest possible round-trip latency will be less than 100 nanoseconds.

Implementation Note:

Since the fundamental granularity is limited by clock cycle and HEART-BEAT ordered-set lengths to at least 4 nanoseconds, and the maximum round-trip link latency is roughly 100,000 nanoseconds across a 10 km link, a 2-byte counter (e.g., counting to 64K cycles of 4ns. each) should be sufficient. A 3-byte counter, with 4 ns. granularity, would allow accurate round-trip latency measurement of a link roughly 6,700 km. long.

Use of the Heartbeat mechanism allows for a PortInfo value, *SM.Port-Info(LinkRoundTripLatency)*, which is accessible through the subnet management MAD Get mechanism, as described in <u>Section 5.4.2</u>, <u>"Status Outputs (MAD get)," on page 107</u>. This is a 32 bit value representing the round-trip latency of the link, measured in 4 nanosecond intervals. This value is reset to 0xFFFF_FFF upon entry to LinkDownDefaultState. When a SND heartbeat is transmitted, the current time (most likely via a free-running counter) is latched. Upon reception of an ACK heartbeat, the current time is compared against the latched time, and the difference, converted to nanoseconds, is reported as the Link-RoundTripLatency.

Due to delays in scheduling, an ACK may be sent significantly later (by as much as roughly 8 microsec.) than the time that the SND was received, resulting in an erroneously high link latency. Therefore, only the lowest value seen across a set of link latency measurements will indicate the most representative value, and only the lowest measured value should be reported as *SM.PortInfo(LinkRoundTripLatency)*.

The precision of reporting is dependent on how well the link round trip latency has been measured, but is expected to be measured to precision of better than 100 nanoseconds. When a port is brought to the Sleeping, Polling, or Disabled State, the *LinkRoundTripLatency* is re-set to 0xFFFF FFFF.

5.12 PHYSICAL LAYER COMPLIANCE TESTING

The following facilities and procedures are intended to simplify physical layer device characterization and compliance testing to specifications described in <u>Section 6:, "High Speed Electrical Signalling - 2.5Gb/s, 5.0</u> <u>Gb/s, & 10 Gb/s," on page 139</u>, while minimizing the amount of circuity and complexity required in the InfiniBand devices.

C5-15.2.2: All ports claiming compliance with InfiniBand Rel. 1.2 Enhanced Signaling **shall** implement physical layer compliance testing as

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defined by <u>Section 5.12</u>, "Physical Layer Compliance Testing." on page 169, at all link speeds.

5.12.1 COMPLIANCE TESTING OVERVIEW

Device testing is accomplished by attaching the device to test equipment over a link, with the receiver attached to a signal generator such as an arbitrary pattern generator, and the transmitter attached to a signal monitor such as an oscilloscope. Testing at the physical layer does not require intervention by a Subnet Manager. New facilities are included in the port to simplify compliance testing for the high-speed devices, including modification to the Link Training State Machine from the structure shown in Figure 21 to the structure shown in Figure 22, and definition of an orderedset, Training Sequence for Test (TS-T), which is used exclusively for compliance testing. Multiple testing modes are possible, as determined by an Opcode in the TS-T ordered-set.

When the port is placed into the Phy Test state by reception of a TS-T ordered-set from attached test equipment on any lane, it disables all linklevel protocol other than 8b/10b code/decode and TS1 detection, and only enables the physical layer circuitry, including clock and data recovery, link transmitter, driver de-emphasis, and receiver equalization circuitry.

Transmitter testing is accomplished using the TS-T to command the transmitter to transmit particular test patterns, and monitoring the characteristics (jitter, amplitude, rise/fall times, etc.) of the transmitted patterns.

For receiver testing, the test equipment uses the TS-T to command the transmitter to send particular symbols depending on the validity (signal strength, 8b/10b decode correctness as to bit errors, disparity, etc.) of the received data, and then feeding the receiver 8b/10b coded data with various characteristics (signal strength, deterministic jitter, pattern-dependent jitter, etc.) and monitoring the symbols the transmitter sends.

Since there is no link-level logic enabled during this procedure (aside from optional vendor-dependent capabilities which are beyond the scope of this specification), no link-level functions (flow control, CRC, packet framing, etc.) are tested with these procedures. These facilities are intended to test compliance with transmitter and receiver specifications described in <u>Section 6:</u>, "High Speed Electrical Signalling - 2.5Gb/s, 5.0 Gb/s, & 10 Gb/s," on page 139.

5.12.2 COMPLIANCE TESTING FACILITIES

Facilities for physical layer compliance testing include changes to the Link Training State Machine (LTSM), addition of a new Training Sequence for Test (TS-T) ordered-set, and capability for the link to generate patterns specifically used for compliance testing.

5.12.2.1 LINK TRAINING STATE MACHINE MODIFICATIONS FOR COMPLIANCE TESTING

The differences from the legacy Link Training State Machine include the following.

- 1) A new state is defined, "Phy Test", which allows physical layer compliance testing.
- A new training sequence, Training Sequence-Test (TS-T) is added, which allows transitions from the LinkDownDefault State (either Polling or Sleeping) to the Phy Test state.
- 3) Two new transition arcs are added, from Polling and from Sleeping, to the Phy Test state, on reception of TS-T.
- 4) Two new transition arcs are added, from the Phy Test state to the LinkDownDefault state (either Polling or Sleeping), on RcvdTS1. These transitions allow exit from Testing mode, without a power-off of the device. Testing procedures must ensure that no test pattern generates 8 contiguous TS1 patterns before testing is completed.
- 5) Within the Phy Test state, there are three (3) different required modes of operation, as described in <u>Section 5.12.2.2</u>, "Use of the Training <u>Sequence for Test Ordered-Set (TS-T)</u>," on page 171, including (a) a "SKIP-less Idles" mode, of transmitting Idle data without SKIP ordered sets for clock compensation, (b) a "SKIP-less TS1" mode, of transmitting back-to-back TS1 without SKIPs, and (c) a "Receiver Test" mode, of transmitting simple patterns indicating whether the receiver is detecting good data, or is detecting logical bit errors, or is detecting a loss of signal.
- 6) The Phy Test state may optionally also include other test modes, and the TS-T ordered-set allows the transmitter and receiver to optionally be placed in multiple configurations, for optional compliance testing beyond the required modes described above.

The general operation of physical layer compliance testing is described below.

5.12.2.2 Use of the Training Sequence for Test Ordered-Set (TS-T)

The Training Sequence for Test (TS-T) is only generated by test equipment. There is no need for an InfiniBand device to be able to generate this ordered-set - only the need to recognize it and behave appropriately when 8 contiguous and valid copies of TS-T arrive at the receiver port on one or more lanes.

A TS-T may be received on only a single lane, or on multiple lanes. If a multi-lane TS-T ordered-set with different values on different lanes in symbols 8, 9 and 12-15, the port may use any of the received TS-T values.

Symbol 1 of a TS-T (the Lane ID in other ordered-sets) is reserved, so that the test equipment may insert a TS-T on any lane. Symbols 2-7 contain the TS-T unique data symbol, D17.2 (or 51h), whose 10-bit encoded value is the pattern (100011 0101) for both the positive and negative running disparity. Symbols 2-7 may be used by the port to determine the polarity of symbols 8-15, since the test equipment may insert a TS-T of either polarity.

Symbol 8 of a TS-T, the link speed identifier, is used to identify the speed at which the test equipment requests the IB device to operate. At least one bit of this bit map must be asserted to 1. If multiple bits are asserted, the test will be conducted at the highest *LinkSpeedEnabled* speed. This allows testing at the highest enabled speed by simply asserting all bits in this symbol.

Symbol 9 of a TS-T allows the test equipment to determine which testing mode the port will be placed in. The following values are defined.

0: SKIP-less Idle Data

Each transmitter lane transmits a pseudo-random sequence of data symbols, generated by the 11th order LFSR = $X^{11} + X^9 + 1$ with no insertion of SKIP ordered-sets.

1: SKIP-less back-to-back TS1s

Each transmitter lane transmits an unbroken string of TS1 ordered-sets, with no insertion of SKIP ordered-sets.

2: Receiver test.

On each lane, the transmitter sends an indication of the validity of the data received on the corresponding receiver lane.

VALID DATA: For each received symbol on a lane which decodes to a valid 8b/10b code point with good running disparity, the corresponding transmitter lane transmits a D10.2 (010101 0101) character.

LOGICAL ERROR: For each received symbol on a lane which decodes with a logical error (e.g., bit error, or running disparity error), the corresponding transmitter lane transmits a K28.5 D00.0 pair of symbols.

LOSS OF SIGNAL: For each received symbol on a lane which indicates an inadequate signal (e.g., inadequate signal swing, all 0s, all 1s, or noise), the corresponding transmitter lane transmits a K28.5 D01.0 pair of symbols.

3-255: Optional Vendor-dependent opcodes to allow other testing modes.

Symbols 12 and 13 allow the test equipment to optionally configure the transmitter in one of 65,536 vendor-dependent states, and symbols 14

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and 15 allow the test equipment to configure the receiver in one of 65,536 vendor-dependent states. The values 0000h are identified for "normal" or "default" operation, so that test equipment can be expected to get good and correct operation when these fields are set to 0. Values other than 0 are optional and vendor-dependent. Typically only a very small subset of these states will be valid and will provide specific unique behaviors.

Implementation Note:

One particular use of this transmitter and receiver configuration facility may be for measuring transmitter equalization. As described above in <u>Section Chapter 5:</u>, this annex allows transmitters and receivers to negotiate for use of up to 16 different transmitter equalization setting (TES) configurations which may be adapted to the characteristics of the link. Testing of this transmitter equalization facility over various physical links will be an important function. This facility in the TS-T ordered-set can allow the test equipment to configure the transmitter to use a particular TES configuration as it's transmitting the data, in order to see how the different TES settings operate over various media.

Similarly, the facility allows the test equipment to test out various configurations of the receiver circuitry, such as using different receiver equalization setting (RES) configurations.

5.12.3 EXAMPLE COMPLIANCE TEST PROCEDURE

Efficient and fast compliance testing requires a simple and efficient procedure to measure transmitter and receiver characteristics. The proposed procedure described below allows simple testing of the most critical elements of the transmitter and receiver circuitry. More detailed procedures will be used in practice, as this procedure is intended to illustrate use of the facilities described above.

- The Device Under Test (DUT) is powered up, and goes into Polling state, transmitting repeated TS1(s) for 2ms in Polling.Active followed by 100ms of a quiescent output in Polling.Quiet.
- 2) The Test Equipment (TE) (which may be a combination of a sophisticated arbitrary pattern generator and oscilloscope, or a simpler and more application-specific box with FPGAs, simple microprocessors and SERDES circuits) is attached to the DUT by a cable.
- The TE transmits a TS-T to the DUT, with flags set to test a particular device capability (e.g., TS-T with fields set to Speed=QDR, Opcode=0, TxCfg=0000h and RxCfg=0000h).

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	4) The DUT detects the TS-T, transitions to the Phy the values in the TS-T fields to determine the sp	⁷ Test state, and uses becific test mode.
	 If the Opcode in the TS-T was set to 0, indic Data," the DUT transmits Idle data. The TE m such as Rise/Fall Time, Driver Jitter, Transm age, etc., using the wide-spectrum of data co data pattern. 	ating "SKIP-less Idle neasures parameters nitter Peak-Peak volt- ontained in the Idle
	 If the Opcode in the TS-T was set to 1, indic back-to-back TS1s", the DUT transmits TS1 the TE to make similar measurements on a pattern with a combination of high-frequency transition-density (K28.5) elements. 	ating "SKIP-less patterns, allowing much shorter data / (1010) and low-
	 If the Opcode in the TS-T was set to 2, indicative DUT transmits either D10.2, K28.5 D0.0, terns, depending on the validity of the receiver can test the sensitivity of the receiver by variation to the receiver and monitoring the transmitter the TE can test the receiver's sensitivity to in way, to do a full four-corners test of receiver strength and received jitter. 	ating "Receiver Test", or K28.5 D01.0 pat- red signal. The TE ying the signal given d pattern. Similarly, put jitter the same sensitivity to signal
	5) The TE can move the device out of Phy Test sta LinkDownDefaultState (Polling or Sleeping) at a stream of 8 contiguous TS1 ordered-sets on a re	ite and back to the ny time by sending a eceiver lane.
	6) Once the device is back in the Polling state, the mitter under different conditions by sending in a set (e.g., with speed set to DDR instead of QDR 1 instead of 0).	TE can test the trans- new TS-T ordered- , or with TxCfg set to
	 At finish of testing, the TE would send the DUT a dered-sets, placing it back in Polling mode, and t removed. The device is then ready to be connect vices. 	a series of 8 TS1 or- hen the cable can be cted to other IB de-
	There is no cross-dependency between different lar Test state, other from TS1 detection and the requirer erate at the same speed. All lanes of a port move in Test state together. This allows the test procedure de plemented either with serial test equipment, or with n test equipment running multiple lanes at once.	nes during the Phy nent that all lanes op- and out of the Phy scribed here to be im- nore complex parallel
	As described above, the format of the TS-T ordered of the Phy Test state allows various other capabilitie used in a vendor-dependent manner, limited by the c equipment capabilities.	-set and the function to be defined and levice and the testing
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CHAPTER 6: HIGH SPEED ELECTRICAL SIGNALING - 2.5, 5.0, & 10.0 GB/s

6.1 INTRODUCTION

This section describes the signaling that allows for InfiniBand[™] link operation at 2.5Gbits/s (SDR), 5.0 Gbits/s (DDR) and 10 Gbits/s (QDR). Unless otherwise noted, the specifications contained herein apply to all signals of each of the interface width definitions.

The signaling rates are for encoded data on the media, and correspond to 10 bits/Byte. The data rate can also be considered to be 250 MBytes/second/direction for SDR, 500 MB/s for DDR and 1GB/s for QDR for each of the 1, 4, 8, or 12 physical lanes.

6.1.1 BACKGROUND AND REFERENCE MATERIAL

While this specification endeavors to be complete, there is a great deal of background material which is helpful in understanding and correctly implementing this interface that is not included.

Much useful information can be found in books such as "High-Speed Digital Design, A Handbook of Black Magic" by Howard Johnson and Martin Graham and "Digital Systems Engineering" by William J. Dally and John W. Poulton. The web site <u>http://www.t11.org</u> has a great deal of useful information as does the site for 10Gig Ethernet.

The draft 4 Common Electrical Interface (CEI) Interoperability agreement for 6+ and 11+ Gbps I/O from the Optical Internetworking Forum (OIF) was consulted in the preparation of this chapter. At this writing it is document OIF2003.104.5 and is available to members of OIF.

Additional information is available from the IEEE (I&M) subcommittee on Pulse measurement Techniques (SCOPT). Methods of performing pulse amplitude and parametric measurements should be conducted in accordance to IEEE Std.181-2003, and this will be referenced explicitly throughout this chapter.

6.1.2 OVERVIEW AND SUMMARY OF CHANGES FOR THIS SECTION

- 1) Transmit and Channel parameters for DDR and QDR
- Increased total loss and noise budget to 20 dB from 15 dB (DDR/QDR only)
- 3) Required Compliance and Characterization functions
- 4) Receive equalization and pre-emphasis for DDR/QDR

- 5) Transmitter provides training pattern for receive equalizer
- 6) Heartbeat and latency ordered set for connection verification and latency determination
- 7) Channel definition by isolated pulse response and S-parameters
- 8) Common mode changes
- 9) Power is provided to enable "Active Cable" connector receptacles.

Note: Some enhanced functions are defined in other sections of this annex.

6.2 SIGNAL SPECIFICATION

6.2.1 BACKGROUND

This chapter of the InfiniBand[™] specification defines characteristics required to communicate between an InfiniBand output and an InfiniBand input using copper printed wiring on a printed circuit board and optional cabling at signaling rates of 2.5, 5.0, or 10 Gbits/second.

This release of the specification extends and enhances but does not supersede prior releases. Products built using this release will be interoperable with legacy products at SDR rate (2.5 Gbits/second).

Connections are point to point and signaling is unidirectional. By definition, a physical lane comprises a differential pair or fiber in each direction, i.e. a transmit signal and a receive signal at each end.

The characteristic impedance of the cables and printed wiring is nominally 100 ohms differential. The single ended impedance is more variable, depending on the amount of coupling and the package design. The details of properly designing the packaging and interconnect of an InfiniBand link are beyond the scope of this specification and are the responsibility of the designer.

The definition of the DDR and QDR signaling includes a definition of a "Compliance Channel" which represents a worst case connection from driver to receiver. SDR, by contrast, uses a loss budget approach. The compliance channel and the transmitter define the minimum acceptable inputs which the receiver shall be capable of receiving at the specified bit error rate.

A compliant channel is any channel which provides a signal at the receiver which is better than the compliance channel.

An important requirement of InfiniBand is that devices which may be produced by different manufacturers **shall** be inter-operable and hot-pluggable.

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	DDR devices shall be capable of operating in compliance with SDR. QDR devices shall be capable of operating in compliance with SDR and may optionally operate in compliance with DDR. Restrictions on configurations or the use of DC blocking capacitors may be necessary to meet this requirement with respect to prior release backplane ports. Details of the speed negotiation and configuration are specified in <u>Section 5.6</u> , "Link Ini-tialization and Training." on page 118.	1 2 3 4 5 6
	Pluggable devices shall meet the same requirements as other InfiniBand ports.	7 8 9
	Note: The differential amplitude represents the value of the voltage be- tween the true and complement signals. This may be expressed as RMS, peak, or peak-peak. The Peak-Peak value is twice the Peak value. This document uses the IEEE Std.181-2003 terminology in which the value commonly referred to as "peak-peak" is rather called "unsigned ampli- tude".	10 11 12 13 14 15
6.2.2 COMPLIANCE		16 17
	C6-1: This compliance statement is obsolete and has been replaced by <u>C6-1.2.1:</u> .	18 19 20
	C6-1.1.1: This compliance statement is obsolete and has been replaced by $\underline{C6-1.2.2}$.	21 22
	C6-1.2.1: Any device claiming InfiniBand compliance at the slot interface, or copper cable interface shall comply with the requirements of <u>Chapter</u> <u>6: High Speed Electrical Signaling - 2.5, 5.0, & 10.0 Gb/s</u> for Port Type 1 when operating at 2.5 Gb/s (SDR).	23 24 25 26 27
	C6-1.2.2: Any 1x pluggable device claiming InfiniBand compliance at the socket interface shall comply with the requirements of <u>Chapter 6: High</u> <u>Speed Electrical Signaling - 2.5, 5.0, & 10.0 Gb/s</u> for Port Type 2 when operating at 2.5 Gb/s (SDR).	28 29 30 31
	o6-1.2.1: Any device claiming InfiniBand Rel. 1.2 Enhanced Signaling compliance may support data rates higher than SDR. A port may support a non-contiguous set of link speeds, e.g., SDR and QDR without DDR.	32 33 34 35
	o6-1.2.2: Any port claiming InfiniBand Rel. 1.2 Enhanced Signaling compliance at the slot interface, or copper cable interface shall comply with the requirements of <u>Chapter 6: High Speed Electrical Signaling - 2.5, 5.0,</u> <u>& 10.0 Gb/s</u> while operating at 5.0 Gb/s (DDR).	36 37 38 39
	o6-1.2.3: Any port claiming InfiniBand Rel. 1.2 Enhanced Signaling compliance at the slot interface, or copper cable interface shall comply with	40 41 42

the requirements of <u>Chapter 6: High Speed Electrical Signaling - 2.5, 5.0,</u> <u>& 10.0 Gb/s</u> while operating at 10 Gb/s (QDR).

6.3 GENERAL REQUIREMENTS

6.3.1 ESD

C6-2: This compliance statement is obsolete and has been replaced by <u>C6-2.2.1:</u>.

C6-2.1.1: This compliance statement is obsolete and has been replaced by <u>C6-2.2.2:</u>.

C6-2.2.1: InfiniBand signal and power pins **shall** withstand 2000 V of ESD using the human body model and 500 V using the charged device model without damage. Class 2 per JEDEC JESD22-A114-B.

C6-2.2.2: InfiniBand pins **shall** withstand 2000 V of ESD using the human body model and 500 V using the charged device model, Class 2 per JEDEC JESD22-A114-B, with power applied, without damage or non-recoverable error including but not limited to latchup. A recoverable error is one that does not require reset or replacement of the device.

6.3.2 HOT INSERTION AND REMOVAL

C6-3: InfiniBand Devices, including modules and chassis, **shall not** be damaged by unexpected removal or insertion. Removal may occur while the link is operating without damage to either port on the link. Insertion or removal may occur with power on or power off.

6.3.3 ENVIRONMENT

C6-4: This compliance statement is obsolete and has been replaced by <u>C6-4.2.1:</u>.

C6-4.2.1: InfiniBand links **shall** meet all specifications in this chapter when operating in an InfiniBand chassis or other package within the environment as defined in <u>Section 9.5.2</u>, "Cooling Requirements," on page 398. The IB power supply is 12 Volts as defined in <u>Chapter 12</u>: <u>Power / Hot Plug</u>.

Architecture Note

InfiniBand does not specify tolerances or values for the local regulated power supply because the local power supply is regulated locally from the bulk power supply. Only bulk power and aux power are supplied at the IB backplane connector. Regulated Power does not appear at any IB interface.

6.3.4 HIGH SPEED DIFFERENTIAL SHIELD RETURNS

C6-5: The **IB_Sh_Ret** connections are specified on the cable connector to support the isolation of the high speed differential inputs and outputs. These shield returns **shall** be connected to logic ground on the module.

Implementation Note

The primary purpose of these connections is to provide for isolation of the differential signals from each other. These shields also help to insure that the desired impedance of the link is maintained.

C6-6: The bulk shield is used for EMI control and **shall** be connected to chassis ground as defined in <u>Section 7.9.4, "Cable Shield Connections,"</u> on page 192.

6.4 DIFFERENTIAL DRIVER OUTPUTS

The SDR driver characteristics are specified so as to guarantee the specified differential signal characteristics at the receiver as described in <u>Section 6.5, "Differential Receiver Inputs," on page 191</u> within defined InfiniBand topologies. Some driver parameters are not specified, but can be derived from other specified parameters.

SDR, DDR and QDR Driver characteristics **shall** enable the receiver to achieve the specified BER when connected by a compliant channel. Values for driver characteristics are provided but may not be sufficient to guarantee proper operation. In case of conflict, driver characteristics shall be determined from the requirement to achieve the specified BER with a Compliant Channel.

Transmitters are specified at the board side of the backplane or cable connector, TP1 or TP5 in <u>Figure 34</u>. Values at the SERDES (ASIC) pin are informative. **C6-7:** This compliance statement is obsolete and has been replaced by <u>C6-7.2.1:</u>.

C6-7.1.1: This compliance statement is obsolete and has been replaced by <u>C6-7.2.2</u>.

C6-7.2.1: All output ports **shall** comply with the parameters and notes of <u>Table 17 Driver Characteristics for 2.5 Gb/s</u> using appropriate parameters as noted while operating at SDR. The parameters are defined in terms of values at IB port pins.

In addition to the parameters defined for "normal" IB signaling from device to device defined as Port Type 1, additional more restrictive parameters are defined as Port Type 2 for 1x Pluggable Devices such as Optical Transceivers in the Small Form Factor Pluggable (SFP) form factor in order to be compatible with the MSA for that package.

C6-7.2.2: 1x Pluggable ports **shall** meet the jitter J_{T2} and J_{D2} defined for Port Type 2 in addition to the other parameters of <u>Table 17 Driver Characteristics for 2.5 Gb/s</u>.

o6-7.2.1: Any output port claiming InfiniBand Rel. 1.2 Enhanced Signaling compliance **shall** comply with the parameters and notes of <u>Table</u> <u>18 Driver Characteristics for 5.0 Gb/s</u> while operating at DDR.

o6-7.2.2: Any output port claiming InfiniBand Rel. 1.2 Enhanced Signaling compliance **shall** comply with the parameters and notes of <u>Table 19 Driver Characteristics for 10 Gb/s</u> while operating at QDR.

6.4.1 DC BLOCKING

o6-1: This compliance statement is obsolete and has been replaced by <u>o6-7.2.1:</u>

o6-7.2.1: The use of DC blocking capacitors is **optional** for backplane connections at SDR rate.

Explanation: The specified levels and termination allow the direct connection of driver to receiver if desired in environments with a common signal ground reference. Direct connection will minimize cost and maximize signal integrity. At higher speeds, DC blocking capacitors may be required.

C6-8: Cable ports **shall** incorporate DC blocking capacitors located at the receiver.

o6-2: Optionally, additional DC blocking capacitors may be located at the transmitter.
o6-8.2.1: DC blocking capacitors **may** be located at any IB pin (or pin pair).

Any loss or jitter caused by the addition of capacitors must be accounted for as part of the allocation for the printed wiring board on which the capacitors are mounted.

C6-8.2.1: DC blocking capacitors **shall not** be mounted inside the cable assembly.

Capacitor value selection is left to the designer. Capacitors must be large enough to provide a -3dB point below 100 MHz. Impedance and voltage values and measurements below 100 MHz will be affected by the presence of blocking capacitors. Appropriate allowances shall be made when evaluating compliance.

Capacitor DC working voltage is left to the designer. Since the differences in common mode voltage are limited by the power supply voltage and the grounding of the shields, a value of 10 volts should be more than adequate. ESD resistance should be taken into account, since the Cable and Backplane connector pins also need to meet the ESD specifications.

Layout of the mounting pads and vias for the blocking capacitor, and selection of the capacitor value and model must be carefully done in order to minimize impedance discontinuities. At higher speeds, blind or back drilled vias may be required.

6.4.2 EQUALIZATION

The frequency dependent attenuation of the interconnection media degrades the signal and thus produces Inter-Symbol Interference or Data Dependent Jitter which is a component of the Deterministic Jitter. The effects of high frequency attenuation can be reduced by techniques such as:

- Pre-distortion or Pre-emphasis/de-emphasis of the signal produced at the driver.
- Addition of a passive high pass filter network which has a frequency response complementary to that of the interconnect between driver and receiver. This is sometimes called Passive Equalization.
- Adaptive equalization using techniques such as partial response or DFE may be implemented at the receiver.

The method of equalization selected is dependent on the frequency of operation and the generation (version) of the ports. Prior releases of the InfiniBand specification described fixed pre-emphasis or filtering rather than adaptive equalization when operating at 2.5 Gbits/second (SDR) for the first generation backplane interface. A fixed Total Jitter of 0.30 UI is allocated to the interconnect between the transmitter ASIC and the Receiver ASIC. Prior release SDR cables incorporated equalization filters as necessary to limit total jitter.

Ports supporting Rel. 1.2 Enhanced Signaling use a combination of fixed or adaptive transmit equalization and variable receive equalization. The equalization when Enhanced Signaling ports are inter-operating with legacy ports shall be transmit equalization for the ES transmitter and preemphasis or filtering for the legacy transmitter. This may require a new hybrid cable at longer lengths, or an adapter to provide the necessary filtering.

C6-9: This compliance statement is obsolete and has been replaced by <u>C6-9.2.1:</u>.

C6-9.2.1: InfiniBand connection equalization **shall** conform to the following restrictions.

- Backplane connections shall use either a passive equalization network, driver pre-emphasis, or some combination of the two to compensate for the maximum loss as specified in Table 23. This equalization or pre-emphasis shall be provided on the InfiniBand module which contains the transmitter. Backplane connections which exceed the specified loss shall provide additional equalization on the backplane. Note that this pre-emphasis/de-emphasis may cause the subsequent bits in a run to have an amplitude lower than the specified minimum. Figure 30: Waveform with De-emphasis for Backplane and Cable shows examples.
- Equalization filters shall not be provided on Infiniband module cable ports. Equalization for copper cables is provided within the cable assembly (see Section 7.7.3, <u>"Equalization," on page 247</u>). Pre-emphasis/de-emphasis may be provided. Note that this pre-emphasis/deemphasis may cause the subsequent bits in a run to have an amplitude lower than the specified minimum, as shown in Figure 30 Waveform with De-emphasis for Backplane and Cable on page 184.
- Port Type 2 outputs shall not implement pre-emphasis except to a limited extent such that the pre-emphasis shall not cause the amplitude for any bit to violate the maximum or minimum amplitude specifications in <u>Table</u> <u>17</u>.

C6-9.2.2: InfiniBand Rel. 1.2 Enhanced Signaling connection equalization **shall** conform to the following restrictions for ports when operating at 2.5 Gb/s (SDR)

- Backplane connections shall use driver de-emphasis to compensate for the maximum loss as specified in <u>Table</u> <u>23</u>.
- Cable ports **shall** use the specified driver de-emphasis to compensate for the maximum cable loss allowed. This is necessary for compatibility with legacy Receivers.
- Receive equalization may be provided however no training pattern is available other than the SDR initialization sequence as defined in <u>Chapter 5: Link/Phy</u> <u>Interface</u>.
- Equalization for copper cables **may** be provided external to the transmitter for those connections with legacy transmitters.

C6-9.2.3: InfiniBand Rel. 1.2 Enhanced Signaling connection equalization **shall** conform to the following restrictions for ports which may operate at 5.0 Gb/s (DDR) or 10 Gb/s (QDR)

- The transmitter **shall** provide the specified de-emphasis or equalization.
- The transmitter shall transmit a training pattern for the receive equalizer as defined in <u>Chapter 5: Link/Phy</u> <u>Interface</u>.
- Filters shall not be used in the cable or backplane. The allowed interconnect characteristics are defined in Section 6.8, "Compliance Channel - DDR and QDR," on page 203
- Receivers **shall** incorporate equalization since the allowed de-emphasis will not be sufficient to guarantee an open eye under all circumstances



Figure 30 Waveform with De-emphasis for Backplane and Cable

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6.4.3 DIFFERENTIAL OUTPUT CHARACTERISTICS

Symbol	Parameter	Maximum	Minimum	Units	Notes
V _{CM}	Output Common Mode Voltage (backplane connections)	1.2	0.30	V	(Vhigh+Vlow)/2 The common mode is unde- fined if DC blocking capaci- tors are used.
Vdiff (serdes)	Differential output Voltage At Transmit SerDes pins (Informative)	1.6	1.0	V	Differential unsigned wave- form amplitude into 100 ohm differential load. Note 13,14,15.
Vdiffc	Differential output At cable connector pin (Normative)	1.6	0.89	V	Differential unsigned wave- form amplitude into 100 ohm differential load. Note 13,14,15
Vdiffb	Differential output At Backplane connector pin (Normative)	1.6	0.80	V	Differential unsigned wave- form amplitude into 100 ohm differential load Note 13,14,15
Vdisable	Disabled Mode output (Note 5)	1.6	0	V	The output in disabled or qui- escent state may be zero volts differential.
Vstandby	Standby Mode output (Note 5)	1.6	0	V	
t _{DRF}	Driver Transition Time		30	ps	at 20-80% at the connector pins into 100 ohm load
I _{ACCM}	AC Common Mode current (Note 3, 6) (RMS Voltage)	5		uA	Determined by EMI restric- tions and shielding effective- ness. 30 MHz to 6.25 GHz
V _{ACCM}	AC Common Mode Voltage (Note 3, 6, 7)	25		mV	RMS
S _{DD}	Differential Output return loss (Note 1)		10	dB	differential mode Note 11.
S _{SE}	Single Ended Output Return Loss (Note 1)		8	dB	Single ended, either output, current -15 to 15 ma, both pins driven. Note 11
Z _{SEDC}	Single Ended Output ImpedanceLow Fre- quency Note 10, Note 12	10,000	30	Ω	Single ended, either output, current -15 to 15 ma, both pins driven Note 11

Table 17 Driver Characteristics for 2.5 Gb/s

Symbol	Parameter	Maximum	Minimum	Units	Notes
S _{DC}	Common Mode to Differen- tial Reflection	-20		dB	Reflected common mode that appears as differential mode. Note 11
I _{DShort}	Short Circuit Current	100	-100	mA	To any voltage between 1.6 and ground, power on or off.
S _{DBtB}	Skew	500		ps	Between any two physical lanes within a single transmit- ter.
J _D	Deterministic Jitter (Note 2, 8)	.17		UI	Without pre-emphasis
J _T	Total Jitter (Note 8)	.35		UI	At +/- 7s (10 ⁻¹² BER)
J _{D2}	Deterministic Jitter (Note 8, Note 9)	0.09		UI	Without pre-emphasis Port Type 2
J_{T2}	Total Jitter (Note 8, Note 9)	0.24		UI	At +/- 7σ Port Type 2
UI _D	Unit Interval	400	400	ps	Plus/Minus 100 ppm mea- sured over a minimum of 10,000 Uls.

Table 17 Driver Characteristics for 2.5 Gb/s

1. At the InfiniBand connector pins from 100 MHz to 1.875 GHz.

2. A transmitter which implements pre emphasis shall meet the receiver mask with the minimum and maximum allowable interconnect configuration.

3. The AC common mode voltage is limited in order to control radiated EMI. Some causes of AC common mode are skew between the true and complement outputs of the differential driver, mismatched levels between the true and complement outputs of the differential driver, and power supply or ground noise such as that caused by switching activity being conducted through the driver.

4. The output level is increased above the minimum required by the specified backplane attenuation to allow for cable attenuation as well as provide headroom for noise. Amplitude is measured for the first bit in a run if a Backplane port, for all bits of a Cable Port. 5. Section 5:, "Link/Phy Interface," on page 43 defines states in which the transmitter is quiescent. In these states driving node is inactive and there are no transitions on the link. Driver outputs shall be static in these states.

6. Common mode current is measured on an IB cable assembly using a detector bandwidth of 120 kHz below 1 GHz and 1MHz above 1 GHz. All physical lanes shall be transmitting the idle pseudo-random character sequence.

7. Since cable shield effectiveness is in excess of 40 dB and common mode impedance is approximately 50 ohms, driver common mode voltage of 25 mV is specified 8. Jitter is measured as defined in IBTA CIWG Test Specification.

9. Port Type 2 - Obsolete

10. DC to 100 MHz

11. Driver impedances selected to adequately absorb reflections and other noise Return Loss measured with respect to 100 ohms, 100 MHz to 3.75 GHz

12. In the absence of DC blocking capacitors. Undefined if DC blocking capacitors present.

13. Refer to IEEE Std.181-2003 for definitions and procedures around un-signed

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waveform amplitude measurements. (amplitude unsigned.)
14.Waveform amplitude measurements shall be conducted only on consecutive transition
bits, over a 2UI Epoch (IEEE Std. 181-2003) unit interval, to a minimum population of 10E4
UI's. This test should apply to any unsigned consecutive transition bit in the test pattern.
15: Top and Base level calculations should be determined based on the histogram mean technique as described in IEEE Std. 181--2003 (Determining State Levels from the Histogram).

Symbol	Parameter	Maximum	Minimum	Units	Notes
V _{CM}	Common Mode Voltage (Backplane connections) Note 12	1.2	0.75	V	(Vhigh+Vlow)/2 The common mode is unde- fined if DC blocking capaci- tors are used.
Vdiff	Differential output (Note 4) (serdes pins, informative)	1.6	0.8	V	Differential unsigned wave- form amplitude into 100 ohm differential load Note 13,14,15
Vdiffc	Differential output (Note 4) (TP6, normative)	1.6	0.65	V	Differential unsigned wave- form amplitude into 100 ohm differential load Note 13,14,15
Vdiff	Differential output (Note 4) (TP1, normative)	1.6	0.60	V	Differential unsigned wave- form amplitude into 100 ohm differential load Note 13,14,15
Vdisable	Disabled Mode output (Note 5)	1.6	0	V	The output in disabled or qui- escent state may be zero volts differential. DC value
Vstandby	Standby Mode output (Note 5)	1.6	0	V	DC value
t _{DRF}	Driver Transition Time		30	ps	At 20-80% at the package pins into 100 ohm load
I _{ACCM}	AC Common Mode current (Note 3, Note 6) (RMS Voltage)	5		uA	Determined by EMI restric- tions and shielding effective- ness. 30 MHz to 6.25 GHz
V _{ACCM}	AC Common Mode Voltage (Note 3, 6, 7)	25		mV	RMS
S _{DD}	Differential Output Return Loss (Note 1)		10	dB	Differential mode Note 11.

Table 18 Driver Characteristics for 5.0 Gb/s

Symbol	Parameter	Maximum	Minimum	Units	Notes
S _{CC}	Single Ended Return Loss (Note 1)		8	dB	Single ended, either output, current -15 to 15 ma, both pins driven. Note 11
Z _{SEDC}	Single Ended Output ImpedanceLow Fre- quency (Note 10, Note 12)	10,000	30	Ω	Single ended, either output, current -15 to 15 ma, both pins driven Note 11
S _{DC}	Common Mode to Differen- tial Reflection	-20		dB	Reflected common mode that appears as differential mode. Note 11
I _{DShort}	Short Circuit Current	100	-100	mA	To any voltage between 1.6 and ground, power on or off.
S _{DBtB}	Skew	500		ps	between any two physical lanes within a single transmit- ter.
J _{D1}	Deterministic Jitter (Note 2, Note 8)	0.15		UI	Without pre-emphasis
J _{T1}	Total Jitter (Note 8)	0.30		UI	At +/- 7σ
UI _D	Unit Interval	200	200	ps	Plus/Minus 100 ppm mea- sured over a minimum of 10,000 UIs.

Table 18 Driver Characteristics for 5.0 Gb/s

1. At the InfiniBand connector pins from 100 MHz to 3.75 GHz.

2. A transmitter which implements pre emphasis **shall** meet the receiver mask with the minimum and maximum allowable interconnect configuration.

3. The AC common mode voltage is limited in order to control radiated EMI. Some causes of AC common mode are skew between the true and complement outputs of the differential driver, mismatched levels between the true and complement outputs of the

differential driver, mismatched levels between the true and complement outputs of the differential driver, and power supply or ground noise such as that caused by switching activity being conducted through the driver.

4. The output level is increased above the minimum required by the specified backplane attenuation to allow for cable attenuation as well as provide headroom for noise. Amplitude is measured for the first bit in a run.

5. <u>Section 5:, "Link/Phy Interface," on page 43</u> defines states in which the transmitter is quiescent. In these states driving node is inactive and there are no transitions on the link. Driver outputs shall be static in these states.

6. Common mode current is measured on an IB cable assembly using a detector bandwidth of 120 kHz below 1 GHz and 1MHz above 1 GHz. All physical lanes shall be transmitting the idle pseudo-random character sequence.

7. Since cable shield effectiveness is in excess of 40 dB and common mode impedance is approximately 50 ohms, driver common mode voltage of 25 mV is specified

8. Jitter is measured as defined in IBTA CIWG Test Specification.

9. N/A - obsolete.

10. DC to 100 MHz

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11. Driver impedances selected to adequately absorb reflections and other noise Return loss with respect to 100 ohms 100 MHz to $6.25~{\rm GHz}$

12. In the absence of DC blocking capacitors. Undefined if DC blocking capacitors present.
 13. Refer to IEEE Std.181-2003 for definitions and procedures around un-signed waveform amplitude measurements. (amplitude unsigned.)

14.Waveform amplitude measurements shall be conducted only on consecutive transition bits, over a 2UI Epoch (IEEE Std. 181-2003) unit interval, to a minimum population of 10E4 UI's. This test should apply to any unsigned consecutive transition bit in the test pattern. 15: Top and Base level calculations should be determined based on the histogram mean technique as described in IEEE Std. 181--2003 (Determining State Levels from the Histogram).

Symbol	Parameter	Maximum	Minimum	Units	Notes
V _{CM}	Common Mode Voltage Backplane connection Note 12	1.2	0.75	V	(Vhigh+Vlow)/2 The common mode is unde- fined if DC blocking capaci- tors are used.
V _{diff}	Differential output (Note 4) (Serdes pins, informative)	1.6	0.6	V	Differential unsigned wave- form amplitude into 100 ohm differential load Note 13,14,15
V _{diffc}	Differential output (Note 4) (TP6, normative)	1.6	0.50	V	Differential unsigned wave- form amplitude into 100 ohm differential load Note 13,14,15
V _{diffb}	Differential output (Note 4) (TP1, normative)	1.6	0.45	V	Differential unsigned wave- form amplitude into 100 ohm differential load Note 13,14,15
V _{disable}	Disabled Mode output (Note 5)	1.6	0	V	The output in disabled or qui- escent state may be zero volts differential.DC
V _{standby}	Standby Mode output (Note 5)	1.6	0	V	DC
t _{DRF}	Driver Transition Time		30	ps	at 20-80% at the connector pins into 100 ohm load
I _{ACCM}	AC Common Mode current (Note 3, Note 6) (RMS Voltage)	5		uA	Determined by EMI restric- tions and shielding effective- ness. 30 MHz to 6.25 GHz
V _{ACCM}	AC Common Mode Voltage (Note 3, Note 6, Note 7)	25		mV	RMS

Table 19 Driver Characteristics for 10 Gb/s

Symbol	Parameter	Maximum	Minimum	Units	Notes
S _{DD}	Differential Output Return Loss (Note 1)	8		dB	Differential mode Note 11.
S _{CC}	Single Ended Output Return Loss (Note 1)	8		dB	Single ended, either output, current -15 to 15 ma, both outputs driven. Note 11
Z _{SEDC}	Single Ended Output ImpedanceLow Fre- quency (Note 10, Note 12)	10,000	30	Ω	Single ended, either output, current -15 to 15 ma, both pins driven Note 11
S _{DC}	Common Mode to Differen- tial Reflection	-20		dB	Reflected common mode that appears as differential mode. Note 11
I _{DShort}	Short Circuit Current	100	-100	mA	To any voltage between 1.6 and ground, power on or off.
S _{DBtB}	Skew	500		ps	between any two physical lanes within a single transmit- ter.
J _{D1}	Deterministic Jitter (Note 2, Note 8)	.15		UI	Without pre-emphasis
J _{T1}	Total Jitter (Note 8)	.30		UI	At +/- 7σ
UI _D	Unit Interval	100	100	ps	Plus/Minus 100 ppm mea- sured over 10,000 UI.

Table 19 Driver Characteristics for 10 Gb/s

1. At the InfiniBand connector pins from 100 MHz to 3.75 GHz.

2. A transmitter which implements pre emphasis shall meet the receiver mask with the minimum and maximum allowable interconnect configuration.

3. The AC common mode voltage is limited in order to control radiated EMI. Some causes of AC common mode are skew between the true and complement outputs of the differential driver, mismatched levels between the true and complement outputs of the differential driver, and power supply or ground noise such as that caused by switching

activity being conducted through the driver. 4. Amplitude is measured for the first bit in a run if a Backplane port, for all bits of a Cable Port.

5. <u>Section 5:, "Link/Phy Interface," on page 43</u> defines states in which the transmitter is quiescent. In these states driving node is inactive and there are no transitions on the link. Driver outputs shall be static in these states.

6. Common mode current is measured on an IB cable assembly using a detector bandwidth of 120 kHz below 1 GHz and 1MHz above 1 GHz. All physical lanes shall be transmitting the idle pseudo-random character sequence.

7. Since cable shield effectiveness is in excess of 40 dB and common mode impedance is approximately 50 ohms, driver common mode voltage of 25 mV is specified
8. Jitter is measured as defined in IBTA CIWG Test Specification.

	 9. N/A - obsolete 10. DC to 100 MHz 11. Driver impedances selected to adequately absorb reflections and other noise. Return Loss with respect to 100 ohms 100 MHz to 12.5 GHz. 12. In the absence of DC blocking capacitors. Undefined if DC blocking capacitors present. 13. Refer to IEEE Std.181-2003 for definitions and procedures around un-signed waveform amplitude measurements. (amplitude unsigned.) 14.Waveform amplitude measurements shall be conducted only on consecutive transition bits, over a 2UI Epoch (IEEE Std. 181-2003) unit interval, to a minimum population of 10E4 UI's. This test should apply to any unsigned consecutive transition bit in the test pattern. 15: Top and Base level calculations should be determined based on the histogram mean technique as described in IEEE Std. 181-2003 (Determining State Levels from the Histogram).
6.4.4 CABLE DRIVING	
	C6-10: This compliance statement is obsolete and has been removed.
6.5 DIFFERENTIAL RECEIVE	C6-11: This compliance statement is obsolete and has been replaced by <u>C6-11.2.1:</u> .
	C6-11.2.1: All input ports shall comply with the parameters and notes of Table 20 Receiver Characteristics for 2.5 Gb/s while operating at SDR. Parameters apply to the pin type as noted. The parameters are defined in terms of values at ASIC pins. They may be measured at accessible test points, with the values adjusted appropriately as defined in <u>Section 6.7.</u> <u>"Compliance Points." on page 201</u> . A BER of 10 ⁻¹² shall be achieved when connected to the worst case transmitter through any compliant channel.
	o6-11.2.1: All input ports claiming InfiniBand Rel. 1.2 Enhanced Signaling compliance shall comply with the parameters and notes of <u>Table 21 Receiver Characteristics for 5.0 Gb/s</u> while operating at DDR. A BER of 10 ⁻¹² shall be achieved when connected to the worst case transmitter

o6-11.2.2: All input ports claiming InfiniBand Rel. 1.2 Enhanced Signaling compliance **shall** comply with the parameters and notes of <u>Table 22 Receiver Characteristics for 10 Gb/s</u> while operating at QDR. A BER of 10^{-12} shall be achieved when connected to the worst case transmitter through any compliant channel.

through any compliant channel.

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6.5.1 DIFFERENTIAL INPUT CHARACTERISTICS

Symbol	Parameter	Maximum	Minimum	Units	Conditions or Remarks
BER	Bit Error Ratio	10 -12			With minimum input
J _{DR}	Deterministic Jitter at Receiver	.47		UI	Port Type 1
J _{TR}	Total Jitter at Receiver	.65		UI	at 10 ⁻¹² BER
Z _{RTerm}	Termination	62.5	40	Ω	To V _{tt} (differential impedance is double) See <u>Figure 32</u> .
V _{tt}	Termination Voltage Note 3, Note 6	1.0	0.5	V	See Figure 32
S _{DC}	Mode Conversion return loss		30	dB	The plus and minus rails of the signal are each terminated to V _{tt} and must be matched to avoid common mode to differential con version. Note 4. Measured at TP1, TP6.
Z _{Vtt}	Vtt Impedance	30	0	Ω	Note 4.
Z _{Vtt}	Vtt Impedance Note 6	10,000	0	Ω	Note 5 Use of large values can reduce excess power caused by Vcm conflicts between driver and receiver.
L _{DR}	Differential Return Loss		10	dB	Note 4
L _{CMR}	Common Mode Return Loss		6	dB	Note 4
V _{RSense}	Input Sensitivity		175	mV	Minimum differential unsigned waveform amplitude. Note 1, 7, 8 See <u>Figure 31 on page 193</u>
V _{RSD}	Signal Threshold		85	mV	Minimum differential unsigned waveform amplitude. Note 2. See <u>Figure 31 on page 193</u>
Vrmax	Maximum Input Voltage	1.6		V	Maximum differential unsigned waveform amplitude.
V _{RCM}	Common Mode Voltage Note 6	1.25	0.25	V	(Vhigh+Vlow)/2 Note 3.
I _{ROff}	Off Current	50	-50	mA	Max. current into a pin with power off. Max voltage 1.6

Table 20 Receiver Characteristics for 2.5 Gb/s

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	Para	neter	Maximum	Minimum	Units	Conditions or Remarks
V _{RHP}	Hot Plug Voltage (Voltage applied on)	with power off or	1.6	-0.5	V	Applied without damage to any IB connector signal pin.
t _{REye}	Eye width			140	ps	Note 9 See <u>Figure 31 on page 193</u> .
S _{RBtB}	Total Skew		24		ns	Across receive physical lanes on a port. (see <u>Section 5.6.7.4,</u> <u>"RxCMD = EnDeSkew," on</u> <u>page 153</u> Item 2)
		 Signals having VRSense may Unless DC module pins. Over a freq Frequency In the abser Refer to IEF measurement Waveform a bits, over a 2L This test shou Top and Bat technique as of Histogram) 	ing an un-signed an un-signed be ignored. blocking capac uency range of from DC to 100 nce of DC block E Std.181-200 procedures. mplitude meas II Epoch (IEEE Id apply to any se level calcula described in IEI	ed differential differential am itors are prese 100 MHz to 1 0 MHz. king capacitors 03 (Amplitude, urement's sha Std. 181-2003 unsigned con ation should be EE Std. 1812	amplitude g ant betwee .875 GHz . Undefin Waveford Il be conc 3), over a secutive t e determi 2003 (Det	e less than VRSD shall be ignored. reater than VRSD and less than en the termination and the InfiniBan 2. ded if DC blocking capacitors preser m, Unsigned) for definitions and ducted only on consecutive transitio minimum population of 10E3 Ul's. transition bit in the test pattern. ned based on the histogram mean ermining State Levels from the

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Symbol	Parameter	Maximum	Minimum	Units	Conditions or Remarks
BER	Bit Error Ratio	10 ⁻¹²			Driven by compliant transmitter through compliance channel
S _{DD}	Differential return loss		8	dB	Reference to 100 ohms
S _{CC}	Common Mode Return Loss		6	dB	reference to 30 ohms. Note 4
V _{tt}	Termination Voltage	1.2	1.0	V	See <u>Figure 32</u> Note 3, Note 6 May need to change
S _{DC}	Mode Conversion at input	-20		dB	The plus and minus rails of the signal are each terminated to V _{tt} and must be matched to avoid common mode to differential con- version. Note 4 Measured at IB connector pins.
Z _{Vtt}	Vtt Impedance	6	0	Ω	Note 5, Note 6 Use of larger values can reduce excess power caused by Vcm conflicts between driver and receiver.
V _{RSense}	Input Sensitivity (informative, at serdes input)		80	mV	Minimum differential unsigned waveform amplitude. Note 1,7,8 See Figure 31 on page 193
V _{CSense}	Input Sensitivity at cable connec- tor (informative)		90	mV	Minimum differential unsigned waveform amplitude. Note 1,7,8,10 See Figure 31 on page 193
V _{BSense}	Input Sensitivity at Backplane connector (informative)		95	mV	Minimum differential unsigned waveform amplitude. Note 1,7,8,10 See Figure 31 on page 193
Vrmax	Maximum Input Voltage	1.6		V	Maximum differential unsigned waveform amplitude.

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V _{RCM}	Common Mode Voltage Note 6	0.70	1.2	V	(Vhigh+Vlow)/2 Note 3
I _{ROff}	Off Current	50	-50	mA	Max. current into a pin with power off. Max 1.6 V
V _{RHP}	Hot Plug Voltage (Voltage applied with power off or on)	1.6	-0.5	V	Applied without damage to any IB connector signal pin.
t _{REye}	Eye width	????		ps	Note 9 See <u>Figure 31 on page 193</u> .
S _{RBtB}	Total Skew	12		ns	Across receive physical lanes on a port. (see <u>Section 5.6.7.4,</u> <u>"RxCMD = EnDeSkew," on</u> <u>page 153</u> Item 2)

1. Signals meeting the InfiniBand input specification shall be received with a maximum bit error rate of 1*10⁻¹².

2. Signals amplitude informative only. DDR signal amplitude determined by transmit and channel

3. Unless DC blocking capacitors are present between the termination and the InfiniBand module pins.

4. Over a frequency range of 100 MHz to 3.75 GHz.

5. Frequency from DC to 100 MHz.

6. In the absence of DC blocking capacitors. Undefined if DC blocking capacitors present.7. Refer to IEEE Std.181-2003 (Amplitude, Waveform, Unsigned) for definitions and measurement procedures.

8.Waveform amplitude measurement's shall be conducted only on consecutive transition bits, over a 2UI Epoch (IEEE Std. 181-2003), over a minimum population of 1000 UI's. This test should apply to any unsigned consecutive transition bit in the test pattern.

9: Top and Base level calculation should be determined based on the histogram mean technique as described in IEEE Std. 181--2003 (Determining State Levels from the Histogram mean technique)

10. Does not supersede Compliant channel requirement

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Symbol	Parameter	Maximum	Minimum	Units	Conditions or Remarks
BER	Bit Error Ratio	10 -12			Driven by compliant transmitter through compliance channel
V _{tt}	Termination Voltage Note 3, Note 6	1.2	0.9	V	See Figure 32
S _{DD}	Differential Return Loss		8	dB	Note 4
S _{CC}	Common Mode Return Loss		6	dB	Note 4
S _{CD}	Mode Conversion, Common mode to differential	-20		dB	The plus and minus rails of the signal are each terminated to V _{tt} and must be matched to avoid common mode to differential con version. Note 4 Measured at IB connector pins.
Z _{Vtt}	Vtt Impedance Note 6	10,000	0	Ω	Note 5 Use of large values can reduce excess power caused by Vcm conflicts between driver and receiver.
V _{RSense}	Input Sensitivity (informative, at serdes pins)		60	mV	Minimum differential unsigned waveform amplitude. Note 1,7,8 See <u>Figure 31 on page 193</u>
V _{CSense}	Input Sensitivity at cable connec- tor.		70	mV	Minimum differential unsigned waveform amplitude. Note 1,7,8,10 See <u>Figure 31 on page 193</u>
V _{BSense}	Input Sensitivity at Backplane connector		60	mV	Minimum differential unsigned waveform amplitude. Note 1,7,8,10 See <u>Figure 31 on page 193</u>
Vrmax	Maximum Input Voltage	1.6		V	Maximum differential unsigned waveform amplitude.

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Symbol	Parameter	Maximum	Minimum	Units	Conditions or Remarks
V _{RCM}	Common Mode Voltage Note 6	1.25	.8	V	(Vhigh+Vlow)/2 Note 3.
I _{ROff}	Off Current	50	-50	mA	Max. current into a pin with power off.
V _{RHP}	Hot Plug Voltage (Voltage applied with power off or on)	1.6	-0.5	V	Applied without damage to any IB connector signal pin.
t _{REye}	Eye width	????		ps	Note 9 See <u>Figure 31 on page 193</u> .
S _{RBtB}	Total Skew	6		ns	Across receive physical lanes on a port. (see <u>Section 5.6.7.4.</u> <u>"RxCMD = EnDeSkew," on</u> <u>page 153</u> Item 2)

Table 22 Receiver Characteristics for 10 Gb/s

1. Signals meeting the InfiniBand input specification shall be received with a maximum bit error rate of 1*10⁻¹².

2. Signals VRSD for information only. Input signal determined by Transmitter and compliance channel.

3. Unless DC blocking capacitors are present between the termination and the InfiniBand module pins.

4. Over a frequency range of 100 MHz to 7.5 GHz.

5. Frequency from DC to 100 MHz.

6. In the absence of DC blocking capacitors. Undefined if DC blocking capacitors present.
7. Refer to IEEE Std.181-2003 (Amplitude, Waveform, Unsigned) for definitions and measurement procedures.

8.Waveform amplitude measurement's shall be conducted only on consecutive transition bits, over a 2UI Epoch (IEEE Std. 181-2003), over a minimum population of 1000 UI's. This test should apply to any unsigned consecutive transition bit in the test pattern.
9: Top and Base level calculation should be determined based on the histogram mean

technique as described in IEEE Std. 181--2003 (Determining State Levels from the Histogram)

10. Does not supersede Compliant channel requirement.

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6.5.2 TERMINATION		
	Figure 32 shows the concept of termination and signal tial and common mode (odd and even mode) terminated dampen noise and reflections in both modes.	definition. Differen tion is important to
Input Signal Tru	e Zrterm	
	Zvtt Vtt	
Input Signal Co	Zrterm Gnd	

Figure 32 Termination and Signaling

6.5.3 BEACON SIGNALING

C6-12: This compliance statement is obsolete and has been replaced by <u>C6-13.2.1:</u>.

C6-13: This compliance statement is obsolete and has been replaced by <u>C6-13.2.2:</u>.

C6-13.2.1: The beaconing sequence is described in detail in <u>Section 5:.</u> <u>"Link/Phy Interface," on page 79</u>. Devices which power down in X_{Sleep} state **shall** detect the beaconing sequence while operating on Auxiliary power. All devices **shall** detect the beaconing sequence. The beaconing sequence is transmitted at SDR only.

C6-13.2.2: The beacon detection shall meet the following requirements: The beaconing detector **shall** detect a minimum unsigned waveform amplitude of 175 mV p-p as a valid signal present. Unsigned waveform amplitudes less than 85 mV p-p **shall** be considered absent. Signals with transitions only at less than 10 MHz **shall** be considered absent. The beaconing sequence is transmitted at the in band signaling rate of 2.5 Gbits/second with an active period of 2 ms and a quiescent period of 100 ms (See Section 5.6.4.2, "Polling States," on page 127).

Note: Beaconing occurs at 2.5 Gb/s. All links begin the initialization process at 2.5 Gb/s. Continued link connection is verified by periodic transmission and reception of the "Link Heartbeat" ordered-set.

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6.5.4 SIGNALING CAUTIONS

C6-14: This compliance statement is obsolete and has been replaced by <u>C6-14.2.1:</u>.

C6-14.2.1: Note that there are many circumstances in InfiniBand in which no differential voltage will be applied at the IB receiver. Examples include sleeping links, disconnected cables, and partially used ports resulting from width negotiation. Therefore means **shall** be provided to disable or de-gate the data coming from such a receiver to assure that false error signals are not generated. This gating **shall** be maintained across speed changes as appropriate. Note that the heartbeat will be absent in a disconnected link.

6.5.5 REPEATER

C6-15: This compliance statement is obsolete and has been replaced by <u>C6-15.2.1</u>.

C6-15.2.1: A repeater which retimes by recovering the clock and filtering it is allowed. The transmit port of any SDR retimer **shall** meet the specifications of <u>Table 17 on page 185</u>. The receive port of any SDR retimer **shall** meet the specifications of <u>Table 20 on page 192</u>. A repeater need be neither protocol aware nor capable of any error detection. Outputs corresponding to quiescent inputs **shall** be quiescent. Repeaters shall be capable of handling SDR signaling in addition to any other signaling rate with which compliance is claimed. Non SDR repeaters may need to be protocol aware to a limited degree in order to participate in the speed negotiation and equalization or have capabilities to handle SDR data with DDR or QDR clocking.

6.6 LOSS MODEL FOR 2.5 GB/S SIGNALING

Note that <u>Section 6.6, "Loss Model for 2.5 Gb/s signaling," on page 199</u> applies only to SDR 2.5 Gbit/s signaling.

6.6.1 BACKGROUND AND REASONING

Allowable interconnect is specified in terms of attenuation at various package boundaries and at two or more frequencies. This bounds the acceptable configurations but does not guarantee operation. Both the driver and the interconnect are responsible for producing the specified signal at the receiver pins.

6.6.2 Loss Values

C6-16: This compliance statement is obsolete and has been replaced by <u>C6-16.2.1:</u>.

C6-16.2.1: <u>Table 23</u> defines the maximum values of the loss assumed in IB interconnect topologies. The following sections define each of the

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parameters. IB components shall limit loss at each package level to provide the eye openings and amplitudes at the Compliance Test Points as shown in Table 24 2.5 Gb/s Signal Test Points on page 202, when operating at 2.5 Gb/s (SDR).

Loss Parameter	Symbol	dB @ 2.5Gb/s, 1.25 GHz	dB at 625 MHz
Total Loss	L _T	15 dB	8 dB
Adapter Board ¹	L _A	2.5 dB	1.8 dB
Cable Assembly ²	L _C	See <u>Chapter 7: Copper</u> <u>Cable</u>	
I/O Plate	L _S	1 dB	0.6 dB
Active Backplane	L _{BA}	9.5 dB	6.5 dB
Passive Backplane	L _{BP}	7 dB	5 dB
Crosstalk	L _{XT}	3dB	N/A

Table 23 SDR Loss Parameter Maximum Values

¹ includes a loss based on 1 pf via at the connector. Implementations must account for larger vias, if used.

² Cable attenuation is measured from the connecting vias on the IB board. Allowable values are defined in Chapter 7: Copper Cable.

3. Loss at 625 MHz specified for predictable equalization. Attenuation is assumed to be

6.6.2.1 TOTAL LOSS (LT)

26 Total loss is measured between the pins of communicating IC packages or between the receiving IC and the passive equalizer at the transmitter. 27

6.6.2.2 ADAPTER BOARD LOSS (LA)

The maximum loss from the IC package to the board connector is 2.5 db at 1250 MHz, including the connector.

6.6.2.3 CABLE ASSEMBLY LOSS (LC)

The maximum loss in a cable assembly, including the connector loss, is 10 db (value given here for reference only) as defined in Section 7:, "Copper Cable," on page 212.

6.6.2.4 I/O PLATE LOSS (LS)

38 The maximum loss from the IC package to the I/O plate connector is 1 dB not including the connector. 39 InfiniBandTM Architecture Release 1.2 **High Speed Electrical Signaling - 2.5, 5.0, & 10.0 Gb/s** VOLUME 2 - PHYSICAL SPECIFICATIONS October, 2004 FINAL

6.6.2.5 PLUGGABLE DEVICE LOSS The maximum loss from the IC package to the Pluggable Device Con-2 nector is 1 dB. 3 4 6.6.2.6 CROSSTALK 5 80 mV referenced to the receiver of the loss budget is reserved for worst 6 case crosstalk and other noise sources. Crosstalk is specified for the 7 Backplane Connector in InfiniBand Architecture Specification, Table 108. "Connector electrical performance requirements," on page 433, and for 8 the cable connectors in InfiniBand Architecture Specification, Table 31, 9 "Cable connector electrical performance requirements," on page 214. 10 11 **6.7 COMPLIANCE POINTS** 12 Since the ASIC or Serdes pins are not accessible, other points within the 13 IB defined topologies are defined and the signal levels listed in Table 24, 14 "2.5 Gb/s Signal Test Points," on page 202 below. These signal levels and 15 eve openings are derived from the already defined driver, receiver, and in-16 terconnect characteristics. All values are for an equivalent 100 ohm differential impedance load located at the test point. Correction or de-17 embedding must be performed to derive actual measured data, taking into 18 account the configuration of the test setup. 19 20 21 Connector 22 23 TP2 TP1 24 ASIC 25 26 TP3 TP4 27 28 29 Board Backplane 30 31 Figure 33 Board/Backplane test points 32 33 34 35 36 37 38 39 40 41 42

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Table 24 2.5 Gb/s Signal Test Points

Test Point	Description	Unsigned Waveform Amplitude Notes 1,2	Eye Width
TP1	Transmitted signal at board side of back- plane connector	.8	250 ps
TP2	Transmitted signal at backplane side of backplane connector	.75	240 ps
TP3	Received signal at board side of connector	.316	150 ps
TP4	Received signal at backplane side of con- nector	.335	160 ps
TP5	Transmitted signal at board side of cable connector	.89	250 ps
TP6	Transmitted signal at cable side of cable connector	.82	240 ps
TP7	Received signal at board side of cable con- nector	.282	150 ps
TP8	Received signal at cable side of cable con- nector	.30	160 ps
TP9	Transmitted signal at board side of plugga- ble interface socket	.89	296 ps
TP10	Received signal at board side of pluggable interface socket	.282	126 ps

1. Refer to IEEE Std.181-2003 (Amplitude, Waveform, Unsigned) for definitions and

procedures around un-signed waveform amplitude measurements. 2. Waveform amplitude measurements shall be conducted only on consecutive transition bits, over a 2UI Epoch (IEEE Std. 181-2003) unit interval, over a minimum population of 10E4 UI's.

C6-16.1.1: This compliance statement is obsolete and has been replaced by <u>C6-16.2.2:</u>.

C6-16.1.2: This compliance statement is obsolete and has been replaced by <u>C6-16.2.3:</u>.

C6-16.1.3: This compliance statement is obsolete and has been replaced by <u>C6-16.2.4:</u>.

C6-16.2.2: SDR Backplane Connections shall comply with the amplitude and eye opening at TP1 and TP3. TP2 and TP4 are for reference.

C6-16.2.3: SDR Cable Connection shall comply with the amplitude and eye opening at TP5 and TP7. TP6 and TP8 are for reference.

C6-16.2.4: 1x Pluggable and 4x PluggableDevice Ports shall comply with the amplitude and eye opening at TP9 and TP10. Measurement may require de-embedding.

6.8 COMPLIANCE CHANNEL - DDR AND QDR

The signal characteristics seen by an InfiniBand DDR or QDR receiver are defined by the combination of the Transmitter characteristics as defined in the tables and any Compliant Channel as defined in this section. It is intended that the channel will be capable of being equalized by the receiver using equalizers such as a 5-tap DFE.

6.8.1 DDR (5.0 GBIT/SEC) COMPLIANT CHANNEL

A Compliant Channel is defined in terms of response to an isolated bit having an amplitude of 1.0 volt, measured at 1.0 UI intervals. <u>Table 25</u> <u>Compliant Channel Impulse response on page 204</u> defines the values. For test purposes, bits of alternating polarity should be used, separated by adequate time.

o6-16.2.1: Any receiver claiming InfiniBand Rel. 1.2 Enhanced Signaling compliance **shall** achieve a BER of 10^{-12} when connected to an InfiniBand compliant Transmitter through any Compliant Channel when operating at 5.0 Gb/s (DDR).

6.8.2 QDR (10.0 GBIT/SEC) COMPLIANT CHANNEL

A Compliant Channel is defined in terms of response to an isolated bit having an amplitude of 1 volt, measured at 1.0 UI intervals as listed in

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<u>Table 25 Compliant Channel Impulse response on page 204</u>. For test purposes, bits of alternating polarity should be used, separated by adequate time.

o6-16.2.1: Any receiver claiming InfiniBand Rel. 1.2 Enhanced Signaling compliance **shall** achieve a BER of 10⁻¹² when connected to an Infini-Band compliant Transmitter through any Compliant Channel when operating at 10.0 Gb/s (QDR).

	-	• •
Interval	DDR Amplitude	QDR Amplitude
-5	.01	.01
-4	.01	.01
-3	.01	.01
-2	.01	.01
-1	.03	.03
0	.180	.180
1	.06	.06
2	.04	.04
3	.03	.02
4	.01	.01
5	.01	.01

Table 25 Compliant Channel Impulse response

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6.8.3 EXAMPLE COMPLIANT CHANNEL DEFINITION



6.8.4 COMPLIANT CHANNEL S-PARAMETERS

Parameters are for maximum loss at Bit rate/2, and must be scaled for shorter configurations having less loss at Bitrate/2.

Frequency	SDD11	SDD21 (min)	SDD21 (max)	SDC11	SDC21
100 MHz	-10	0	-1	-20	-20
200 MHz	-10	-2	-1	-20	-20
625 MHz	-10	-7	-4	-20	-20
1250 MHz	-10	-10	-8	-18	-18
1875 MHz	-10	-12.5	-11	-15	-15
2500 MHz	-10	-15	-15	-10 dB	-10 dB

Table 26 S Parameters DDR (dB)

Table 27 S parameters QDR (dB)

Frequency	SDD11	SDD21 (min)	SDD21 (max)	SDC11	SDC21
100 MHz	-10		0	-20 dB	-20 dB
200 MHz	-10	-2	-1	-20	-20
625 MHz	-10	-3	-2	-20	-20
1250 MHz	-10	-5	-4	-20	-20

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Table 27 S parameters QDR (dB)						
Frequency	SDD11	SDD21 (min)	SDD21 (max)	SDC11	SDC21	
1875 MHz	-10	-7	-6	-18	-18	
2500 MHz	-10	-10	-8	-15	-15	
3750 MHz	-10	-12.5	-11	-12	-12	
5000 MHz	-10	-15 dB	-15	-10 dB	-10dB	

6.9 BIT TO BIT SKEW

6.9.1 SKEW VALUES

C6-17: <u>Table 28</u> defines the allowable bit to bit skew across the physical lanes. All IB ports shall limit skew to the values in Table 28 Bit to Bit Skew **Parameter Maximum Values**

Table 28 Bit to Bit Skew Parameter Maximum Values

Skew Parameter	Symbol	Value
Total Skew ^a	S _{RBtB}	60 UI
Driving Transceiver ^b	S _{DBtB}	500 ps
Backplane	S _{BPBtB}	500 ps
Adapter Board	S _{ABtB}	500 ps
Cable Assembly ^c	S _{CBtB}	See <u>Chapter 7:</u> and <u>Chapter 8:</u>
Transceiver to I/O Plate	S _{SBtB}	500 ps
Retiming Repeater (2 max per link) ^d	S _{RTR}	10 UI each, 20 UI total See <u>Section 5.10,</u> <u>"Retiming Repeaters,"</u> <u>on page 125</u>
Defined in <u>Table 20 Rece</u> 22 and included for referen Defined in <u>Table 17 Drive</u>	iver Characte nce. er Characteris	eristics for 2.5 Gb/s on pag stics for 2.5 Gb/s on page

c. Defined in Chapter 7: Copper Cable.

d. Retiming repeaters may independently insert or delete skip symbols on a per lane basis. Repeaters which do not utilize skips are not counted in this limit.

6.9.2 SKEW DEFINITION

Skew at any point is measured using the zero crossings of the differential voltage of the commas present in the training sequences TS1 and TS2 or in the Skip ordered-set as defined in Section 5.3.2, "Control Ordered-

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<u>sets." on page 98</u>. Each of these sequences transmits a rank of commas on all physical lanes simultaneously.

6.10 ELECTRICAL TOPOLOGIES

This section outlines the electrical topologies accommodated within the InfiniBand specification.

Integrated Circuits (IC) that are depicted represent elements that generate and accept a specified InfiniBand interface. These ICs may be any one of the following types of functions:

- Host Channel Adapter (HCA)
- Target Channel Adapter (TCA)
- Switch
- Repeater (non-addressable retime and redrive component)
- Electrical/Optical Translation function
- Pluggable Device

6.10.1 ON-BOARD

This configuration is used for interconnection of IC on a common PCB.



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5 6

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6.10.2 SLOT ON ACTIVE BACKPLANE

2 This is the typical chipset bridge or switch chip on a backplane that interfaces to an adapter board plugged into the backplane. This topology is 3 typical of PCI configurations. 4



Figure 37 Slot on Active Backplane Topology

6.10.3 SLOT TO SLOT VIA BACKPLANE

21 This topology allows for one pluggable board (for example, a switch) to interface to another pluggable board (for example, a TCA) through a pas-22 sive backplane. 23



6.10.4 COPPER INTERCONNECTS

These interfaces would be used for driving remote TCA or HCA through 39 copper cables either from I/O Plate to I/O Plate, in the case of a switch to 40 a switch or adapter, or from a backplane mounted switch to another backplane mounted switch. A cable will be one of 1x, 4x, 8x or 12x. A typical

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	application of this topology might be a stand-alone necting to another such box or a processor.	storage box con-



Backplanes (or "System Boards") may be connected together using cable.



Figure 40 System Board to System Board via Cable Topology

6.10.5 OPTICAL FIBER

This topology may be used for driving remote IB ports at distances of up to several hundred meters (or several km using the long haul fiber and laser transmitters) through optical interfaces. Each end of the link may be mounted on pluggable boards with each housing optical transceiver components as shown in Figure 41 or be directly mounted on a system board as shown in Figure 42. This release of the InfiniBand specification specifies 1x and 4x short and long haul links, and 1x, 4x, 8x and 12x short haul

optical links, at several speeds. Backplanes may be connected together using optical links. The transceivers depicted translate the InfinibandTM copper interface into an optical interface to drive the optical componentry.

1



face into an InfiniBand Pluggable Device interface to drive the interconnect componentry.



Figure 43 Pluggable Device Topology

6.11 Physical Layer Test and Characterization Facilities

Test, characterization, and compliance verification of an IB port requires additional states, modes, or accessible signals that are not required for functional operation. These facilities, as specified in the Link/Phy section of this annex, are recommended but not required for legacy ports. These facilities are required for devices claiming compliance with Rel. 1.2 Enhanced Signaling.

The test and characterization modes are specified in the Link/Phy section of this annex, <u>Section 5.12</u>, "Physical Layer Compliance Testing." on page 169.

o6-17.2.1: Any device claiming InfiniBand Rel. 1.2 Enhanced Signaling compliance at the slot interface, or copper cable interface **shall** comply with the requirements of <u>Section 6.11 on page 211</u> regarding physical layer test and characterization facilities.

CHAPTER 7: COPPER CABLE

7.1 INTRODUCTION

This chapter defines InfiniBand cables and the connectors used to attach InfiniBand cables to InfiniBand modules. InfiniBand cable connectors **shall** incorporate features shown in the appropriate sections below that specify the connector to board interfaces.

It is the responsibility of the cable and connector designers or suppliers to perform the indicated tests and supply the data to potential customer companies to indicate compliance. It is recommended that the appropriate test groups specified in EIA-364.1000.01 be used for qualification testing, using the following conditions:

- 50 mating cycles preconditioning
- Un-mated exposure, option 2 mixed flowing gas exposure
- Five year product life
- Field operating temperature range up to 60 degrees C.

7.2 CABLE AND BOARD CONNECTORS - COMMON REQUIREMENTS

The requirements stated in this section apply to all connectors used to attach InfiniBand cables to InfiniBand modules. The following individual sections that define the specific connectors to be used for a given link width may also define additional requirements for that specific connector.

Use of the keying definitions included herein is optional; however, utilization of these definitions is highly recommended to prevent plugging of InfiniBand cables into ports using incompatible interfaces such as Fibre Channel.

7.2.1 PHYSICAL AND MECHANICAL PERFORMANCE REQUIREMENTS

C7-1: Connectors to be used on and for connection to InfiniBand modules **shall** meet or exceed the physical and mechanical performance requirements listed in <u>Table 29</u>.

It is also recommended that connector interfaces meet the parameters defined in <u>Table 30</u>. Unless otherwise noted, successful completion of a given test is indicated by an acceptable Low Level Contact Resistance measurement as indicated in EIA-364.1000.01 or other equivalent test sequence.

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2 3 4

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Note that all drawing dimensions in the following sections are in millimeters (mm).

Table 29 Cable connector physical requirements

	Parameter		Minimum	Maximum	Units	Conditions/Comments
N	Durability		250		mating cycles	Without physical damage or exceeding low level contact resistance when mated; no more than 1% of contacts with exposed base metal
Fi	Insertion force	1x		30	Ν	
		4x		56		
		12x		73		
Fw	Withdrawal force	1x		30	Ν	
		4x		49		
		12x		59		
F _r	Retention force		75		Ν	Load pull, per EIA 364-38A
F _{ls}	Side load capability	,	75		N	No damage to cable or board, no opens detected with LLCR test; force applied to the cable in a plane parallel to the I/O plate at a distance of 90 mm, in the direction of the smaller dimension of the receptacle
F _{II}	Longitudinal load c	apability	100		N	No damage to cable or board, no opens detected with LLCR test; force applied to the cable in a plane parallel to the I/O plate at a distance of 90 mm, in the direction of the larger dimension of the receptacle
F _{rc}	Housing contact re force	tention	5		Ν	
t _{pm}	Contact finish – opt	tion 1	0.76 Au over 1.27 Nickel		μm	
t _{pm}	Contact finish – opt	tion 2	0.51 PdNi with Au flash over 1.27 Nickel		μm	Min. 75% Pd in PdNi alloy

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- 41

 D_{wc}

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13 14

	Table 30 Recomm	nended cable co	onnector p	hysical	requirements
Symbol	Parameter	Minimum	Maximum	Units	Conditions/Comment
F _n	Contact normal force	100		cN	per contact beam
S _{hcc}	Contact Hertz stress	170		kpsi	per contact beam

1.0

7.2.2 ELECTRICAL PERFORMANCE REQUIREMENTS

Contact wipe

C7-2: Connectors to be used on and for connection to InfiniBand modules shall meet or exceed the electrical performance requirements for port type 1, listed in Table 31.

mm

Table 31 Cable connector electrical performance requirements

Symbol	Parameter	Minimum	Maximum	Units	Conditions/Comment	
LLCR	Low level contact resis- tance - initial		80	mΩ	through testing per EIA 364-23	
ALLCR	Low level contact resis- tance - change		20	mΩ	through testing per EIA 364-23, as a result of any test group step	
I _{max}	Current rating	0.5		A	per EIA-364-70 or IEC 512-5-1 Test 5a, at 30° C. temperature rise above ambient	
Z _{dco} (peak)	Differential Impedance (peak)	90	110	Ω	Mated cable and board connector, average value measured over the propagation delay	
Z _{dco} (nom)	Differential Impedance (nominal)	95	105	Ω	The connector at 100 ps rise time (at the connector) per EIA 364-108. Includes connector, cable to connector interface, and board termination pads and vias but not equalizer.	
L _{co}	Insertion loss		1.0	dB	Mated cable assembly and board connector, at frequencies up to 1.25 GHz, per EIA 364-101	
S _{cop}	Within pair skew		5	ps	per EIA 364-103; by design, measurement not required	
J _{co}	Jitter		10	ps	per EIA 364-107 with Fibre Channel CJTPAT stimulus until 10000 hits in max. 20 mV high jit- ter box or equivalent, with equipment and fix- ture contribution de-embedded; by design, measurement not required.	
NEXT _c	Near end crosstalk		4	%	Mated cable and board connector, measured differentially with all adjacent neighbor pairs driven at 100 ps transition time, per EIA 364-90 and <u>Section 6.6.2.6</u> . A lower value will result in additional design margin. See Note 2.	

The signal eye pattern at the cable output must conform to the electrical requirements as listed in <u>Table 31</u> and shown in <u>Figure 60</u> in all cases.

Notes

1. All rise or transition times referenced in this chapter of the specification are assumed to be measured from the 20% to 80% levels of the waveform base state to top state amplitudes.

2. Crosstalk is calculated by dividing the larger of the amplitudes of the unsigned positive or negative differential crosstalk noise waveforms by the unsigned amplitude of the differential aggressor waveform, the result being multiplied by 100 to obtain percent. In the case of measurement by superposition, the noise voltage is the sum of the maximum noise amplitude values induced by the individual aggressor pair sources.

7.2.3 ENVIRONMENTAL PERFORMANCE REQUIREMENTS

C7-3: Connectors to be used on and for connection to InfiniBand modules **shall** meet or exceed the environmental performance requirements of EIA-364.1000.01, including exposure to Mixed Flowing Gas consistent with the required product life as defined in <u>Section 7.1</u>.

Unless otherwise noted, successful completion of a given test is indicated by an acceptable Low Level Contact Resistance measurement upon completion of the test, as defined above.

7.2.4 PORT LABELING

It is recommended that I/O ports be labeled to avoid confusion between InfiniBand ports and connections and those used for other incompatible interfaces. The recommended labeling is defined in <u>Section 9.6</u>.

7.3 1x INTERFACE BOARD CONNECTOR

This section defines the connector for the 1x cable interface on InfiniBand boards. The 1x interface is the narrowest InfiniBand link, providing for simultaneous transmit and receive of one bit of differential data.

7.3.1 DESCRIPTION

The connector used on InfiniBand boards for 1x cable ports is similar to that used for Fibre Channel. The receptacle is a surface-mounted design with seven contacts; four of the pins are signal contacts, and three con-

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tacts are connected to signal ground. The connector is shielded to minimize EMI radiation. A suitable receptacle, referred to as HSSDC2 1 InfiniBand, is available from Tyco Electronics and others, and is shown in Figure 44. Detailed drawings of mating interface dimensions are shown in Figure 45. 5

C7-4: All 1x InfiniBand cable plugs **shall** be intermateable with this connector.






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or signal assignment	2
Signal	3 4
ignal Ground	5
lBtxlp(0)	6
IBtxIn(0)	7
lignal Ground	9
BtxOn(0)	10
	11
Fignal Ground	12
	13
hassis Ground	14
B_Sh_Ret on the module.	16
	17
to Chassis Ground in the	18
	19
e cable's inner shield(s)	20
bund shall be provided to in-	21
ment.	23
s not likely to meet the elec-	24
	25
	26
((27
tom-side (opposite the latch	28
	29
	31
	32
cable interface on InfiniBand	33
ineous transmit and receive	34
	35
	36
cable interface on InfiniBand	37
s separated by Ground con-	39
The connector is surface-	40
able receptacle, referred to	41
1010, 13 available 110111 FujilSU	42
Proprietary and Confidential	

Table 32 1x cable board connecto

Pin Number Signal		
1	Signal Ground	
2	IBtxIp(0)	
3	IBtxIn(0)	
4	Signal Ground	
5	IBtxOn(0)	
6	IBtxOp(0)	
7	Signal Ground	
Housing	Chassis Ground	

C7-6: Signal Ground shall be connected to I

C7-7: Signal Ground shall not be connected connector.

C7-7.1.1: A continuous ground path from the through the connector to the board signal gro sure low jitter, low crosstalk and EMI contain

A cable constructed with only a bulk shield is trical requirements of Section 6.3.4.

7.3.4 KEYING

The 1x board connector accommodates a bot side) key with width of 1.0 mm, which is center nector body, as shown in Figure 45.

7.4 4X INTERFACE BOARD CONNECTOR

This section defines the connector for the 4x of boards. The 4x interface provides for simulta of four bits of differential data.

7.4.1 DESCRIPTION

This section defines the connector for the 4x of boards. The connector uses pairs of contacts tacts to reduce near end crosstalk (NEXT). T mounted, and all signal pins are used. A suita as an eight pair MICRO GIGACN^{TM 1} recepta

2

Components Ltd. and others, and is shown in <u>Figure 47</u>. Detailed drawings of mating interface dimensions are shown in <u>Figure 48</u>.

C7-8: All 4x InfiniBand cable plugs **shall** be intermateable with this con-





Copper Cable

7.4.2 FOOTPRINT AND CONTACT PATTERN



Figure 49 4x cable board connector footprint, top view

7.4.3 PIN ASSIGNMENT

C7-9: The pin assignment listed in <u>Table 33</u> **shall** be used for the board connector for InfiniBand 4x cables.

The character 'x' in the signal symbol is the port number, as defined in <u>Section 4.1, "Signal Naming Conventions," on page 69</u>.

Table 33 4x board connector signal assignment

Pin Number	Signal
G1-G9	Signal Ground
S1	IBtxIp(0)
S2	IBtxIn(0)
S3	IBtxIp(1)

Pin Number	Signal
S4	lBtxIn(1)
S5	IBtxIp(2)
S6	IBtxIn(2)
S7	IBtxIp(3)
S8	IBtxIn(3)
S9	IBtxOn(3)
S10	IBtxOp(3)
S11	IBtxOn(2)
S12	IBtxOp(2)
S13	IBtxOn(1)
S14	IBtxOp(1)
S15	IBtxOn(0)
S16	IBtxOp(0)
Housing	Chassis Ground

Table 33 4x board connector signal assignment

C7-10: Signal Ground shall be connected to IB_Sh_Ret on the module.

C7-11: Signal Ground **shall not** be connected to Chassis Ground in the connector. See <u>Section 9.5.4</u>.

C7-11.1.1: A continuous ground path from the cable's inner shield(s) through the connector to the board signal ground **shall** be provided to insure low jitter, low crosstalk and EMI containment.

A cable constructed with only a bulk shield is not likely to meet the electrical requirements of <u>Section 6.3.4</u>.

7.4.4 KEYING

It is recommended that the 4x board and copper cable connectors as used for InfiniBand use keys in positions 4 and 5, shown in <u>Figure 52</u> as viewed from the outside of the chassis. This is to prevent misplugging with other interfaces that might have chosen to use the same physical connector.



Figure 50 4x board and cable connector keying

7.5 12x AND 8x INTERFACE BOARD CONNECTOR

This section defines the connector for the 12x and 8x cable interface on InfiniBand boards. The 12x interface is the widest InfiniBand link, providing for simultaneous transmit and receive of twelve bits of encoded differential data.

7.5.1 DESCRIPTION

This connector uses pairs of contacts separated by Ground contacts to reduce near end crosstalk (NEXT). The connector is a surface-mounted design similar to that of the 4x connector, and all signal pins are used. A suitable receptacle, referred to as a 24 pair MICRO GIGACN receptacle, is available from Fujitsu Components Ltd. and others, and is shown in Figure 51. Detailed drawings of mating interface dimensions are shown in Figure 48.

The 8x cable interface uses the same board connector as the 12x interface described in <u>Section 7.5 on page 225</u>, but with a subset of the pins used.

C7-12: All 12x InfiniBand cable plugs **shall** be intermateable with this connector.

C7-12.2.1: All 8x InfiniBand cable plugs **shall** be intermateable with this connector.



7.5.2 FOOTPRINT AND CONTACT PATTERN

The board footprint shown in Figure 52 should be used for the 12x cable board connector shown in Figure 51. Connector pin numbers are indicated for information. The connector is surface-mounted, so there are no contacts on the secondary side of the board.



Figure 52 12x cable board connector footprint, top view

7.5.3 PIN ASSIGNMENT FOR 12X OPERATION

C7-13: The pin assignment listed in <u>Table 34</u> **shall** be used for the board connector for InfiniBand 12x cables.

The character 'x' in the signal symbol is the port number, as defined in <u>Section 4.1, "Signal Naming Conventions," on page 69</u>.

Pin Number	Signal	
G1-G25	Signal Ground	
S1	IBtxlp(0)	
S2	IBtxIn(0)	
S3	IBtxlp(1)	
S4	lBtxIn(1)	
S5	IBtxlp(2)	
S6	IBtxIn(2)	

Table 34 12x board connector signal assignment

Table 34 12x board connector signal assignment

Pin Number	Signal	2
S7	IBtxIp(3)	3
S8	IBtxIn(3)	5
S9	IBtxIp(4)	6
S10	IBtxIn(4)	7
S11	IBtxIp(5)	8
S12	IBtxIn(5)	9 10
S13	IBtxlp(6)	11
S14	IBtxIn(6)	12
S15	IBtxIp(7)	13
	IBtxIn(7)	14
S17	IBtxIn(8)	16
S18	IBtxIn(8)	17
S10	IBtxIn(0)	18
\$13 \$20	IBtxlp(0)	19
520		20
521		22
S22	IBtxIn(10)	23
S23	IBtxIp(11)	24
S24	IBtxIn(11)	25
S25	IBtxOn(11)	20
S26	IBtxOp(11)	28
S27	IBtxOn(10)	29
S28	IBtxOp(10)	30
S29	lBtxOn(9)	31
S30	IBtxOp(9)	33
S31	IBtxOn(8)	34
S32	IBtxOp(8)	35
S33	IBtxOn(7)	36
S34	IBtxOp(7)	38
S35	IBtxOn(6)	39
S36	IBtxOp(6)	40
	,	41

Pin Number	Signal	
S37	lBtxOn(5)	
S38	IBtxOp(5)	
S39	IBtxOn(4)	
S40	IBtxOp(4)	
S41	IBtxOn(3)	
S42	IBtxOp(3)	
S43	IBtxOn(2)	
S44	IBtxOp(2)	
S45	lBtxOn(1)	
S46	IBtxOp(1)	
S47	lBtxOn(0)	
S48	IBtxOp(0)	
Housing	Chassis Ground	

Table 34 12x board connector signal assignment

C7-14: Signal Ground shall be connected to IB_Sh_Ret on the module.

C7-15: Signal Ground **shall not** be connected to Chassis Ground in the connector.

C7-15.1.1: A continuous ground path from the cable's inner shield(s) through the connector to the board signal ground **shall** be provided to insure low jitter, low crosstalk and EMI containment.

A cable constructed with only a bulk shield is not likely to meet the electrical requirements of <u>Section 6.3.4</u>.

7.5.4 PIN ASSIGNMENT FOR 8X OPERATION

o7-15.2.1: The pin assignment listed in <u>Table 34</u> **shall** be used for the board connector for InfiniBand 8x cables.

The character 'x' in the signal symbol is the port number, as defined in <u>Section 4.1, "Signal Naming Conventions," on page 69</u>.

Table 35 8x board connector signal assignment

Pin Number	Signal
G1-G25	Signal Ground
S1	IBtxIp(0)
S2	IBtxIn(0)
S3	IBtxIp(1)
S4	IBtxIn(1)
S5	IBtxIp(2)
S6	IBtxIn(2)
S7	IBtxIp(3)
S8	IBtxIn(3)
S9	IBtxIp(4)
S10	IBtxIn(4)
S11	IBtxIp(5)
S12	lBtxIn(5)
S13	IBtxIp(6)
S14	IBtxIn(6)
S15	IBtxIp(7)
S16	lBtxIn(7)
S17	reserved
S18	reserved
S19	reserved
S20	reserved
S21	reserved
S22	reserved
S23	reserved
S24	reserved
S25	reserved
S26	reserved
S27	reserved
S28	reserved

Table 35 8>	(board	connector	signal	assignment
-------------	---------	-----------	--------	------------

Pin Number	Signal
S29	reserved
S30	reserved
S31	reserved
\$32	reserved
S33	IBtxOn(7)
S34	IBtxOp(7)
S35	IBtxOn(6)
S36	IBtxOp(6)
S37	IBtxOn(5)
S38	IBtxOp(5)
S39	IBtxOn(4)
S40	IBtxOp(4)
S41	IBtxOn(3)
S42	IBtxOp(3)
S43	IBtxOn(2)
S44	IBtxOp(2)
S45	IBtxOn(1)
S46	IBtxOp(1)
S47	IBtxOn(0)
S48	IBtxOp(0)
Housing	Chassis Ground

7.5.5 KEYING

It is recommended that the 12x board and copper cable connectors as used for InfiniBand use keys in positions 4 and 5, shown in Figure 53 as viewed from the outside of the chassis. This is to prevent misplugging with other interfaces that might have chosen to use the same physical connector.

It is recommended that the 8x board and copper cable connectors as used for InfiniBand use the same keying as that for a 12x cable.

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7.6 PLUGGABLE INTERFACE CONNECTORS

Unlike the 1x, 4x, 8x, and 12x connectors described in the preceding sections, a pluggable interface port is designed to be used with either copper or optical cables. Due to the need to account for the jitter introduced in the assembly between the board and the cable, a new port type, referred to as port type 2, is defined for these devices. The unique electrical requirements for port type 2 are listed in <u>Section 6.4</u>. In the case of the copper pluggable devices, the transceiver may be part of the cable assembly that is mated with the port connector on the board. Only those cable types listed in <u>Table 36</u> **shall** be supported.

The active devices contain circuitry to compensate for the jitter introduced27in the cable assembly. The active optical device external interface is de-28fined in Section 8.10.The passive copper device is permanently attached29to the cable, so the port type 2 interface to the board is the only separable30interface.31

C7-15.1.2: Passive copper pluggable cables **shall** meet the requirements listed in <u>Section 6.4</u>.

Pluggable device type	Board port type	External port type	Cable connector	38
Active copper	2	1	1x Copper (HSSDC2)	40

Table 36 1x Pluggable interface supported device types

		••	
Pluggable device type	Board port type	External port type	Cable connector
Active optical	2	See Section 8.10	See Section 8.10
Passive copper (captive)	2	None (see text)	None (see text)

Table 36 1x Pluggable interface supported device types

7.6.1 1X PLUGGABLE INTERFACE

7.6.1.1 DESCRIPTION

The interface connector used on InfiniBand boards for 1x pluggable copper and optical ports is the same one defined for Small Form Factor Pluggables, as specified in SFF-8074 for Fibre Channel applications. The receptacle is a surface-mounted design with twenty contacts; eleven of the pins are signal contacts, two are power contacts, and seven contacts are connected to signal Ground. A separate metal cage is utilized on the board to minimize EMI radiation. The connector and cage are shown in Figure 54. The example shown in the figure is for a device in which the cable is separable from the transceiver, as in the case of the active copper device.

Note

Not all devices that will physically fit in the pluggable interface port are supported by this specification. See <u>Table 36</u> for the supported pluggable device types.



C7-15.1.3: Connectors to be used for pluggable ports on InfiniBand modules **shall** meet or exceed the physical and mechanical performance requirements listed in <u>Table 37</u>, which are common to those in SFF-8074.

Symbol	Parameter	Minimum	Maximum	Units	Conditions/Comments
Fi	Insertion force	0	40	N	
Fw	Withdrawal force	0	11.5	N	
F _{rx}	Transceiver retention force	90	170	N	no damage to transceiver below 90 N
Frcl	Cage retention (latch strength)	180		N	no damage to latch below 180 N
F_{ck}	Cage kickout spring force	11.5	22	N	
N _{hc}	Durability, host connector and cage	100		cycles	

Table 37 Pluggable interface physical requirements

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Table 37 Pluggable interface physical requirements

Symbol	Parameter	Minimum	Maximum	Units	Conditions/Comments	
N _x	Durability, transceiver	50		cycles		2

7.6.1.3 ELECTRICAL REQUIREMENTS

C7-15.1.4: The pluggable interface **shall** meet the additional electrical performance requirements listed in <u>Section 6.4</u> for port type 2, as specified at the board contacts of the host connector.

7.6.1.4 FOOTPRINT AND CONTACT PATTERN

The board footprint and contact pattern for the pluggable interface is shown in <u>Figure 55</u>. The I/O plate panel cutout is shown in <u>Figure 56</u>.





7.6.1.5 PIN ASSIGNMENTS

C7-15.1.5: The pin assignment shown in <u>Table 38</u> **shall** be used for the 1x pluggable interface.

The reader is referred to SFF-8074 for the detailed descriptions of the pin functions.

Pin number	Signal	Description
1	VeeT	Transmit Ground
2	TxFault	Transmit Fault indication
3	TxDisable	Transmitter Disable (active high)
4	MOD-DEF(2)	Module Definition 2, 2-wire serial interface
5	MOD-DEF(1)	Module Definition 1, 2-wire serial interface

Pin number	Signal	Description	
6	MOD-DEF(0)	Module Definition 0, internally Grounded in module	
7	Rate Select	Selects receiver bandwidth; low or open = reduced, high = full	
8	LOS	Loss of Signal (active high)	
9	VeeR	Receive Ground	
10	VeeR	Receive Ground	
11	VeeR	Receive Ground	
12	IBtxIn(0)	- Received data	
13	IBtxIp(0)	+ Received data	
14	VeeR	Receive Ground	
15	VccR	Receiver power, 3.3 V ±5%	
16	VccT	Transmitter power, 3.3 V ±5%	
17	VeeT	Transmit Ground	
18	IBtxOp(0)	+ Transmit data	
19	IBtxOn(0)	- Transmit data	
20	VeeT	Transmit Ground	

Table 38 Pluggable interface pin assignment

7.6.2 4X PLUGGABLE INTERFACE

This section specifies the 4x Single Data Rate (SDR) (2.5 GT/s) pluggable interface. The 4x Pluggable Interface is designed to allow a copper cable or optical transceiver to be attached to an InfiniBand HCA, TCA or Switch. The 4x Pluggable Interface supports Active Copper, Passive Copper, and Optical (4x-SX and 4x-LX) type devices.

7.6.2.1 DESCRIPTION

The 4x Pluggable is based in part on the XPAK MSA. The mechanical specifications are identical to XPAK, while the High Speed electrical and optical interface specifications are based on the InfiniBand specifications listed in the *InfiniBand Architecture Specification*, <u>Volume 2</u>, <u>Chapters 6</u> and 8.

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7.6.2.2 PHYSICAL REQUIREMENTS

The physical dimensions of the 4x Pluggable transceiver are shown in <u>Figure 57</u> for reference. The reader is referred to the official XPAK MSA documentation for specific dimensions and function.

C7-15.2.1: 4X pluggable interface **shall** meet or exceed the physical, electrical and mechanical performance specifications of the official XPAK MSA documentation.



Figure 57 XPAK transceiver physical outline

Copper Cable

1 2

7.6.2.3 FOOTPRINT AND CONTACT PATTERN





7.6.2.4 PIN ASSIGNMENTS

C7-15.2.2: The pin assignment shown in <u>Table 39</u> **shall** be used for the for the 4x Pluggable interface.

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Name

Pin

No

GND

REF CLK-

REF CLK+

TX LANE3-

TX LANE3+

TX LANE2-

TX LANE2+

TX LANE1-

TX LANE1+

TX LANE0-

TX LANE0+

RX LANE3-

RX LANE3+

RX LANE2-

RX LANE2+

RX LANE1-

RX LANE1+

RX LANE0-

RX LANE0+

SRCCLK-

SRCCLK+

70

69 68

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64 63

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Name

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erface	2
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P2	25
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Table 39 Pin Assignment for 4x Pluggable Interface

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33

34

35

Pin

No

GND

GND

GND

5.0V

3.3V

3.3V

APS

APS

LASI

RESET

VEND SPECIFIC

TX ON/OFF

MGMT I/F

PRTAD3

PRTAD2

PRTAD1

PRTAD0

APS SET

APS

APS

3.3V

3.3V

5.0V

GND

GND

GND

MODE XAUI/SFI4

RX LOCK ER#

APS SENSE

MGMT CLK

MGMT Mode

TX LOCK ER#

MOD DETECT

VEND SPECIFIC

VEND SPECIFIC

7.6.2.5 REGISTER SET

The register map for InfiniBand is identical to XPAK 2.31 and XENPAK 3.0, with the following exceptions:

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	• The XPAK register OUI, in register 32818 (de decimal) is 0x000ACB (hexadecimal) (this is which is 0x0008BE).	ecimal) 0x8032 (hexa- different from XENPAK
	• The XPAK register package type mask, in reg 0x8012 (hexadecimal) is 00000100 (binary), decimal) (this is different from XENPAK which	gister 32768 (decimal), 4 (decimal), 0x04 (hexa- h is 0x01)
	In addition, the following extensions to the XENF set is defined for InfiniBand TM 4x pluggable device XPAK MSA form factor.	AK MSA NVM register ces that conform to the

Table 40 InfiniBand register additions for 4x Pluggable

Field	Dec	Hex	NVRA M Byte	Size	Name	Description	Register value, hex	Interpretation
Basic	32787	8013	12	1	Connector	Optical con- nector	40	MPO/MTP
Basic	32791	8017	16	1	Protocol	Protocol type	20	IB 1x
Basic	32791	8017	16	1	Protocol	Protocol type	40	IB 4x
Basic	32801	8021	26	1	Standards Compliance Code	IB Optical Dis- tance/10GFC Code Byte 3	10	IB LX
Basic	32801	8021	26	1	Standards Compliance Code	IB Optical Dis- tance/10GFC Code Byte 3	20	IB SX
Basic	32801	8021	26	1	Standards Compliance Code	IB Copper type/10GFC Code Byte 3	40	IB active cop- per
Basic	32801	8021	26	1	Standards Compliance Code	IB Copper type/10GFC Code Byte 3	80	IB passive copper

7.6.2.6 HIGH SPEED SIGNALING

7.6.2.6.1 GENERAL REQUIREMENTS

C7-15.2.3: The high-speed signaling interface to the 4x Pluggable **shall** comply with the requirements listed in the *InfiniBand Architecture Specification*, <u>Volume 2</u>, <u>Chapter 6</u>:

7.6.2.6.2 ELECTRICAL SPECIFICATIONS

The electrical interface, including pinout, power supplies and management functionality, is specified by XENPAK MSA v3.0 with the exceptions listed below. The pinout for SFI4-P2 implementation is identical to XE-NPAK MSA v3.0, and is shown for reference only.

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7.6.2.6.3 DIFFERENTIAL DRIVER OUT	PUTS	4
	C7-15.2.4: All SDR output ports for the 4x Pluggable interface shall comply with the parameters and notes of <u>Table 17 Driver Characteristics</u> for 2.5 Gb/s. Parameters apply to the pin type as noted. The parameters are defined in terms of values at ASIC pins. They may be measured at accessible test points, with the values adjusted appropriately as defined in <u>Section 6.7, "Compliance Points," on page 201</u> .	2 3 4 5 6
7.6.2.6.4 DIFFERENTIAL RECEIVER IN	IPUTS	8
	C7-15.2.5: All SDR input ports for the 4x Pluggable interface shall comply with the parameters and notes of <u>Table 20 Receiver Characteristics for 2.5</u> <u>Gb/s</u> . Parameters apply to the pin type as noted. The parameters are defined in terms of values at ASIC pins. They may be measured at accessible test points, with the values adjusted appropriately as defined in <u>Section 6.7</u> , "Compliance Points," on page 201.	9 10 11 12 13
7.6.2.6.5 LOSS MODEL		15
	C7-15.2.6: The maximum loss from the IC package to the Pluggable Device Connector is 1 dB.	16 17
7.6.2.6.6 COMPLIANCE POINTS		18
	C7-15.2.7: 1x Pluggable Device Ports shall comply with the amplitude and eye opening at TP9 and TP10 as described in <u>Table 24 2.5 Gb/s Signal</u> <u>Test Points</u> . Measurement may require de-embedding.	19 20 21 22
7.6.3 4X OPTICAL PLUGGABLE	Devices	23
	C7-15.2.8: All 4x SDR Optical Pluggable devices shall comply with requirements in its respective 4x optical distance classification (SX or LX) in the <i>InfiniBand Architecture Specification</i> , <u>Volume 2</u> , <u>Chapter 8: Fiber Attachment - 2.5 Gb/s</u> , 5.0 Gb/s, & 10 Gb/s.	24 25 26 27
		28
7.7 CABLES	This section defines the characteristics of InfiniBand cables. It is the intent of this specification to allow for and encourage innovation in the market. Therefore, the emphasis is on interoperability and minimum requirements needed to insure functionality without restricting the means of implemen- tation. Specific bulk wire conductor size, insulation materials, etc. are ex- plicitly not specified herein, allowing suppliers to determine the optimum design for a given application.	29 30 31 32 33 34 35 36 37 38
(.1.1 PHYSICAL REQUIREMENT		39
	It is recommended that cable assemblies to be used for InfiniBand prod- ucts have a minimum bend radius of no more than 100 mm (4 inches), as shown in <u>Figure 59</u> . The bend radius is the radius to which the cable can	40 41 42



The sections of this specification that deal with the specific link widths may have additional requirements that **shall** also be met for that specific interface.

Notes

1. Although the cable differential impedance specification listed in <u>Table 41</u> covers a relatively wide range, the board connector and wiring are specified at 100 Ohms nominal. The use of cables with impedance significantly different from 100 Ohms (due to higher wire impedance or equalizer circuitry, or both) will result in losses due to reflections at the impedance mismatches. These losses may be significant unless there is sufficient attenuation in the cable to reduce them to an acceptable level.

2. It is left to the cable designer to evaluate the trade-off between reflection loss and length in the cable design to insure reliable operation. Cables less than some minimum length may not operate reliably outside the range of 90-110 Ohms differential impedance, due to insufficient attenuation of these signal reflections. The signal eye pattern at the cable output must conform to the electrical requirements as listed in <u>Table 41</u> and shown in <u>Figure 60</u> in all cases.

Symbol	Parameter	Minimum	Maximum	Units	Conditions/Comments
Z _{dca} (nom)	Differential Imped- ance, nominal value	95	155	Ω	per EIA 364-108, measured over the length of each signal pair, from the unequalized end (if equalizer is used)
Z _{dca} (peak)	Differential Imped- ance, deviation from nominal value		5	Ω	measured over the length of each signal pair
L _{ca}	Insertion loss		10	dB	mated cable assembly and board connector, at frequencies up to 1.25 GHz, per EIA 364-101
S _{cal}	Pair to pair skew		500	ps	see Table 28 Bit to Bit Skew Parameter Maximum Values
J _{ca}	Jitter		0.25	U	per EIA 364-107 and IEEE 191-2003, with 1 V dif- ferential Fibre Channel CJTPAT stimulus until 10000 hits in max. 20 mV high jitter box or equiv- alent, with equipment and fixture contribution de- embedded; worst case pair, with three adjacent pairs on one side of that pair (if they exist) to be driven at the same end of the cable as the mea- surement is performed, by an asynchronous source with 1.5 V unsigned differential amplitude and transition time of 100 ps or less at the board pins. The far end of each adjacent pair should be terminated in 50 Ohms to Ground. A PRBS gen- erator or other source may be used for driving the adjacent pairs, at a minimum of 1.3 Gb/s. See Figure 60.
V _{Cout}	Eye height (voltage)	196		mV	minimum unsigned differential amplitude for 1 V differential Fibre Channel CJTPAT stimulus until 10000 hits in max. 20 mV high jitter box or equivalent, measured at board connector pins under the same conditions as J_{ca} (see above).See Figure 60. For information, 316 mV if measured without crosstalk.
T _{Reye}	Eye width (time)	0.75		UI	minimum time opening for 1 V differential Fibre Channel CJTPAT stimulus until 10000 hits in max. 20 mV high jitter box or equivalent, measured at board connector pins under the same conditions as J_{ca} (see above). See <u>Figure 60</u> .

The signal eye pattern at the cable output must conform to the electrical requirements as listed in <u>Table 41</u> and shown in <u>Figure 60</u> in all cases.



Figure 60 Eye Opening at receiving board connector pins (differential)

Note

It is recommended that within pair skew be no more than 120 ps total for any given pair in a cable assembly. Within pair skew may cause excessive jitter or induce sufficient shield current to exceed EMI radiation limits. It is expected that shield currents over 1 μ A may be sufficient to cause radiation problems.

Within pair skew is a parameter that is easily measured at the cable assembly level, and is often useful if the eye parameters (opening and jitter) do not meet specification. The eye parameters are the critical test for functionality, hence within pair skew is primarily included here as guidance for diagnostic purposes.

7.7.3 EQUALIZATION

Equalization in the cable, either fabricated as part of the bulk wire or in the form of discrete components in the cable assembly (e. g., on a printed circuit board inside the cable connector backshell), is permitted. However, the cable assembly **shall** be required to meet the electrical requirements defined in <u>Table 41</u> and <u>Figure 60</u>.

Note

Signal reflections can occur when using equalized cable assemblies, due to the presence of equalizer components which add in series with the cable characteristic impedance and may nearly double the apparent impedance seen by the signal. Normally these reflections are harmless due to cable attenuation and the use of source and/or receiver matching. Implementers should be aware of the potential for reflections if less than ideal impedance matches exist at the various interfaces in the path. The signal eye pattern at the cable output must conform to the electrical requirements as listed in <u>Table 41</u> and in <u>Figure 60</u> in all cases.

7.7.4 CABLE SHIELD CONNECTIONS

7.7.4.1 INNER (SIGNAL PAIR OR QUAD) SHIELD

C7-17: The **IB_Sh_Ret** signals **shall** be connected to the cable inner shield(s) in the cable connector.

C7-18: A continuous ground path from the cable's inner shield(s) through the connector to the board signal ground **shall** be provided to insure low jitter, low crosstalk and EMI containment.

Note

The primary purpose of these connections is to provide for isolation of the differential signals from each other. These shields also help to insure that the desired impedance of the link is maintained.

A cable connector or receptacle constructed with only a bulk shield is not likely to meet the electrical requirements of <u>Section 6.3.4</u>.

7.7.4.2 OUTER (BULK) SHIELD

C7-19: The cable bulk shield (shield used over the outside of the collection of conductors) used in InfiniBand cables **shall** be directly connected to chassis ground at both ends.

This specification does not permit AC coupling of the bulk shield.

7.7.5 ACTIVE CABLES

This release of this specification describes Active Cables in <u>Section 7.8</u>, <u>40</u> <u>"Active Cables," on page 264</u>.

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7.7.6 PORT LABELING

It is recommended that I/O cables be labeled to avoid confusion between InfiniBand ports and connections and those used for other incompatible interfaces. The recommended labeling is defined in <u>Section 9.6</u>.

7.7.7 1X INTERFACE CABLE

7.7.7.1 CABLE CONNECTOR DESCRIPTION

The cable plug to be used on InfiniBand 1x cables is a derivative of the plug used for the Fibre Channel standard. The design uses seven in-line contacts, and the backshell incorporates a top side latch.

C7-19.1.1: A metal backshell or other means which fully shields the connector **shall** be bonded to the cable bulk shield through a continuous 360 degree contact to minimize EMI (Electromagnetic Interference).

Two pairs of signals are used, one each for transmit and receive. The signal pairs are isolated by the use of a signal Ground pin between them to minimize near end crosstalk (NEXT). A suitable plug, referred to as HSSDC2 InfiniBand, is available from Tyco Electronics and others, and is shown in Figure 61. Detailed drawings of mating interface dimensions are shown in Figure 48.

C7-20: 1x Board receptacles used on InfiniBand modules **shall** be intermateable with this connector.



7.7.7.2 PIN ASSIGNMENT

Note

Cable signal nets **shall** be connected from each *transmit* signal pair on the source port to the appropriate *receive* signal pair. For example, a cable from port y to port z **shall** be wired to connect IBtyOp(0) (positive output signal from port y, bit 0), to IBtzIp(0) (positive input to port z, bit 0) and IBtyOn(0) to IBtzIn(0), as shown in <u>Table 42</u>.

Table 42 1x cable connector signal assignment Plug 1 Plug 2 Pin number Pin number Signal Signal 1 Signal Ground 7 Signal Ground 2 IBtxlp(0) 6 IBtxOp(0) 3 IBtxIn(0) 5 IBtxOn(0) 4 Signal Ground 4 Signal Ground 5 3 IBtxOn(0) IBtxIn(0) 2 6 IBtxOp(0) IBtxlp(0) 7 1 Signal Ground Signal Ground Housing Chassis Ground Housing Chassis Ground

C7-22: Signal Ground **shall not** be connected to Chassis Ground in the cable or cable connector.

7.7.7.3 KEYING

The 1x cable plug includes a slot to accept a 1.0 mm bottom-side (opposite the latch side) key corresponding to the key in the receptacle, which is centered horizontally in the connector body.

7.7.8 4x CABLE

7.7.8.1 CABLE CONNECTOR DESCRIPTION

The cable plug to be used on InfiniBand 4x cables uses pairs of contacts interspersed with Ground contacts for crosstalk reduction. Eight pairs of signals are used, four each for transmit and receive. A suitable plug, referred to as an eight pair MICRO GIGACN plug, is available from Fujitsu 42

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Components Component, Ltd. and others, and is shown in <u>Figure 62</u>. Detailed drawings of mating interface dimensions are shown in <u>Figure 48</u>.

C7-23: 4x Board receptacles used on InfiniBand modules **shall** be intermateable with this connector.

C7-23.1.1: A metal backshell or other means which fully shields the connector **shall** be bonded to the cable bulk shield through a continuous 360 degree contact to minimize EMI (Electromagnetic Interference).

Side latches are used in conjunction with receptacle features for retention, and are released by pulling on the "lanyard" handle shown in the drawing.




There are no unused pins in the cable plug.

Note

Cable signal nets shall be connected from each transmit signal pair on the source port to the appropriate receive signal pair on the desired destination port. For example, a cable from port y to port z should be wired to connect IBtyOp(0) (positive output signal from port y, bit 0), to IBtzIp(0) (positive input to port z, bit 0) and IBtyOn(0) to IBtzIn(0), as shown in Table 43.

Table 43 4x cable connector signal assignment					
Pl	ug 1	Pl	ug 2		
Pin number	Signal	Pin number	Signal		
G1-G9	Signal Ground	G1-G9	Signal Ground		
S1	IBtxIp(0)	S16	IBtxOp(0)		
S2	IBtxIn(0)	S15	IBtxOn(0)		
S3	IBtxIp(1)	S14	IBtxOp(1)		
S4	IBtxIn(1)	S13	IBtxOn(1)		
S5	IBtxIp(2)	S12	IBtxOp(2)		
S6	IBtxIn(2)	S11	IBtxOn(2)		
S7	IBtxIp(3)	S10	IBtxOp(3)		
S8	IBtxIn(3)	S9	IBtxOn(3)		
S9	IBtxOn(3)	S8	IBtxIn(3)		
S10	IBtxOp(3)	S7	IBtxIp(3)		
S11	IBtxOn(2)	S6	IBtxIn(2)		
S12	IBtxOp(2)	S5	IBtxIp(2)		
S13	IBtxOn(1)	S4	lBtxIn(1)		
S14	IBtxOp(1)	S3	IBtxIp(1)		
S15	IBtxOn(0)	S2	lBtxIn(0)		
S16	IBtxOp(0)	S1	lBtxlp(0)		
Housing	Chassis Ground	Housing	Chassis Ground		

C7-25: Signal Ground shall not be connected to Chassis Ground in the cable or cable connector.

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7.7.8.3 KEYING

It is recommended that the 4x copper cable connectors as used for Infini-Band use keys in positions 4 and 5, shown in <u>Figure 52</u>.

7.7.9 12x CABLE

7.7.9.1 CONNECTOR DESCRIPTION

This cable plug uses a similar design to that of the 4x cable plug. The plug uses pairs of signal contacts interspersed with Ground contacts for crosstalk reduction. Side latches are used in conjunction with receptacle features for retention, and are released by pulling on the "lanyard" handle shown in the drawing. A suitable plug, referred to as a 24 pair MICRO GI-GACN plug, is available from Fujitsu Components Ltd. and others, and is shown in Figure 64. Detailed drawings of mating interface dimensions are shown in Figure 63.

The cable plug may be designed using a dual bulk wire exit to accommodate the large bulk wire diameter while reducing bend radius. In that case, each of the two bulk cables would contain twelve signal pairs of wire.

C7-26: 12x Board receptacles used on InfiniBand modules **shall** be intermateable with this connector.

C7-26.1.1: A metal backshell or other means which fully shields the connector **shall** be bonded to the cable bulk shield through a continuous 360 degree contact to minimize EMI (Electromagnetic Interference).

Twenty-four pairs of signals are used, twelve each for transmit and receive.



Note

Cable signal nets **shall** be connected from each *transmit* signal pair on the source port to the appropriate *receive* signal pair on the desired destination port. For example, a cable from port y to port z should be wired to connect IBtyOp(0) (positive output signal from port y, bit 0), to IBtzIp(0) (positive input to port z, bit 0) and IBtyOn(0) to IBtzIn(0), as shown in <u>Table 44</u>.

Plug 1		PI	ug 2
Pin number	Signal	Pin number	Signal
G1-G25	Signal Ground	G1-G25	Signal Ground
S1	IBtxIp(0)	S48	IBtxOp(0)
S2	IBtxIn(0)	S47	IBtxOn(0)
S3	IBtxIp(1)	S46	IBtxOp(1)
S4	IBtxIn(1)	S45	IBtxOn(1)
S5	IBtxIp(2)	S44	IBtxOp(2)
S6	IBtxIn(2)	S43	IBtxOn(2)
S7	IBtxIp(3)	S42	IBtxOp(3)
S8	IBtxIn(3)	S41	IBtxOn(3)
S9	IBtxIp(4)	S40	IBtxOp(4)
S10	lBtxIn(4)	S39	IBtxOn(4)
S11	IBtxIp(5)	S38	IBtxOp(5)
S12	lBtxIn(5)	S37	IBtxOn(5)
S13	lBtxlp(6)	S36	IBtxOp(6)
S14	lBtxIn(6)	S35	IBtxOn(6)
S15	IBtxIp(7)	S34	IBtxOp(7)
S16	lBtxIn(7)	S33	IBtxOn(7)
S17	IBtxIp(8)	S32	IBtxOp(8)
S18	IBtxIn(8)	S31	IBtxOn(8)
S19	IBtxIp(9)	S30	IBtxOp(9)

Table 44 12x cable connector signal assignment

Plug 1		PI	ug 2
Pin number	Signal	Pin number	Signal
S20	IBtxIn(9)	S29	IBtxOn(9)
S21	IBtxIp(10)	S28	IBtxOp(10)
S22	IBtxIn(10)	S27	IBtxOn(10)
S23	IBtxlp(11)	S26	IBtxOp(11)
S24	lBtxIn(11)	S25	IBtxOn(11)
S25	IBtxOn(11)	S24	IBtxIn(11)
S26	IBtxOp(11)	S23	IBtxIp(11)
S27	IBtxOn(10)	S22	IBtxIn(10)
S28	IBtxOp(10)	S21	IBtxIp(10)
S29	IBtxOn(9)	S20	IBtxIn(9)
S30	IBtxOp(9)	S19	IBtxIp(9)
S31	IBtxOn(8)	S18	IBtxIn(8)
S32	IBtxOp(8)	S17	IBtxlp(8)
S33	IBtxOn(7)	S16	IBtxIn(7)
S34	IBtxOp(7)	S15	IBtxlp(7)
S35	IBtxOn(6)	S14	IBtxIn(6)
S36	IBtxOp(6)	S13	IBtxIp(6)
S37	IBtxOn(5)	S12	IBtxIn(5)
S38	IBtxOp(5)	S11	IBtxIp(5)
S39	IBtxOn(4)	S10	IBtxIn(4)
S40	IBtxOp(4)	S9	IBtxIp(4)
S41	IBtxOn(3)	S8	IBtxIn(3)
S42	IBtxOp(3)	S7	IBtxIp(3)
S43	IBtxOn(2)	S6	IBtxIn(2)
S44	IBtxOp(2)	S5	IBtxIp(2)
S45	IBtxOn(1)	S4	IBtxIn(1)
S46	IBtxOp(1)	S3	IBtxIp(1)
S47	IBtxOn(0)	S2	IBtxIn(0)
S48	IBtxOp(0)	S1	IBtxIp(0)

Table 44 12x cable connector signal assignment

Copper Cable

Table 44 12x cable connector signal assignment

Plug 1		Plu	g 2
Pin number	Signal	Pin number	Signal
Housing	Chassis Ground	Housing	Chassis Ground

C7-28: Signal Ground **shall not** be connected to Chassis Ground in the cable or cable connector. See <u>Section 9.5.4</u>.

7.7.9.3 KEYING

It is recommended that the 12x copper cable connectors as used for InfiniBand use keys as shown in <u>Figure 53</u>.

7.7.10 12x to 3-4x COPPER CABLES

The 12x to 3-4x Copper Cables are used for connecting to devices which may configurably operate with a single 12x port, or with three separate 4x ports, using the same pins. The 12x to 3-4x copper cable provides an interface to a 12x interface board connector, operating as either a single 12x port or three 4x ports. The opposite side of the cable provides three separate 4x cable connectors.

7.7.10.1 12X INTERFACE BOARD CONNECTOR

This section defines the connector for the 12x cable interface on Infini-Band boards. The 12x interface is the widest InfiniBand link, providing for simultaneous transmit and receive of twelve bits of encoded differential data.

7.7.10.2 PIN ASSIGNMENTS

C7-28.2.1: The pin assignment listed in <u>Table 45</u> **shall** be used for the board connector for InfiniBand 12x to 3-4x cables.

The character 'x' in the signal symbol is the port number, as defined in <u>Chapter 4: Port Signal Definitions</u>.

Table 45 12x board connector signal assignment for 12x to 3-4x cables

Pin Number	Signal (single 12x port)	Signal (three 4x ports)
G1-G25	Signal Ground	Signal Ground
S1	IBtxlp(0)	IBtx.1lp(0)
S2	lBtxln(0)	IBtx.1In(0)
S3	lBtxlp(1)	IBtx.1lp(1)

Pin Number	Signal (single 12x port)	Signal (three 4x ports)
S4	lBtxIn(1)	IBtx.1In(1)
S5	IBtxIp(2)	IBtx.1lp(2)
S6	IBtxIn(2)	IBtx.1In(2)
S7	IBtxIp(3)	IBtx.1lp(3)
S8	IBtxIn(3)	IBtx.1In(3)
S9	IBtxIp(4)	IBtx.2Ip(0)
S10	IBtxIn(4)	IBtx.2In(0)
S11	IBtxIp(5)	IBtx.2lp(1)
S12	IBtxIn(5)	lBtx.2In(1)
S13	IBtxIp(6)	IBtx.2lp(2)
S14	IBtxIn(6)	IBtx.2In(2)
S15	IBtxIp(7)	IBtx.2lp(3)
S16	lBtxIn(7)	IBtx.2In(3)
S17	IBtxIp(8)	IBtx.3lp(0)
S18	IBtxIn(8)	IBtx.3In(0)
S19	IBtxIp(9)	IBtx.3lp(1)
S20	IBtxIn(9)	lBtx.3ln(1)
S21	IBtxIp(10)	IBtx.3lp(2)
S22	IBtxIn(10)	IBtx.3In(2)
S23	IBtxlp(11)	IBtx.3lp(3)
S24	IBtxIn(11)	lBtx.3ln(3)
S25	IBtxOn(11)	IBtx.3On(3)
S26	IBtxOp(11)	IBtx.3Op(3)
S27	IBtxOn(10)	IBtx.3On(2)
S28	IBtxOp(10)	IBtx.3Op(2)
S29	IBtxOn(9)	IBtx.3On(1)
S30	IBtxOp(9)	IBtx.30p(1)
S31	IBtxOn(8)	IBtx.3On(0)
\$32	IBtxOp(8)	IBtx.3Op(0)
S33	IBtxOn(7)	IBtx.2On(3)

Table 45 12x board connector signal assignment for 12x to 3-4x cables

Pin Number	Signal (single 12x port)	Signal (three 4x ports)		
S34	IBtxOp(7)	IBtx.2Op(3)		
S35	IBtxOn(6)	IBtx.2On(2)		
S36	IBtxOp(6)	IBtx.2Op(2)		
S37	IBtxOn(5)	IBtx.2On(1)		
S38	IBtxOp(5)	IBtx.2Op(1)		
S39	IBtxOn(4)	IBtx.2On(0)		
S40	IBtxOp(4)	IBtx.2Op(0)		
S41	IBtxOn(3)	IBtx.1On(3)		
S42	IBtxOp(3)	IBtx.1Op(3)		
S43	IBtxOn(2)	IBtx.1On(2)		
S44	IBtxOp(2)	IBtx.1Op(2)		
S45	IBtxOn(1)	IBtx.1On(1)		
S46	IBtxOp(1)	IBtx.1Op(1)		
S47	IBtxOn(0)	IBtx.1On(0)		
S48	IBtxOp(0)	IBtx.1Op(0)		
Housing	Chassis Ground	Chassis Ground		

Table 45 12x board connector signal assignment for 12x to 3-4x cables

7.7.10.3 12x to 3-4x CABLE

This cable provides a means to connect a 12x board connector configured as three 4x ports to three separate 4x devices.

Notes

1. When using a 12x to 3-4x cable, ports 2 and 3 will not width negotiate since there is no lane 0 on those ports.

2. Port 3 (plug 4) of a 12x to 3-4x active cable plugged into an 8x board receptacle will not function.

Twenty-four pairs of signals are used, twelve each for transmit and receive. Eight pairs are used for each 4x port. **Copper Cable**

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C7-28.2.2: A metal backshell or other means which fully shields the connector **shall** be bonded to the cable bulk shield through a continuous 360 degree contact to minimize EMI (Electromagnetic Interference).

7.7.10.4 12x CABLE CONNECTOR DESCRIPTION

The 12x cable plug uses the same connector as the 12x copper cable described in the *InfiniBand Architecture Specification*, <u>Volume 2</u>, <u>Chapter 7</u>: <u>Copper Cable</u>.

C7-28.2.3: 12x Board receptacles used on InfiniBand modules **shall** be intermateable with the cable connector used on the 12x end of the 12x to 3-4x cable.

The 4x cable plug uses the same connector as the 4x copper cable described in the *InfiniBand Architecture Specification*, <u>Volume 2</u>, <u>Chapter 7:</u> <u>Copper Cable</u>.

C7-28.2.4: 4x Board receptacles used on InfiniBand modules **shall** be intermateable with the cable connector used on the 4x end of the 12x to 3-4x cable.

7.7.10.5 PIN ASSIGNMENT

C7-28.2.5: The pin assignment listed in <u>Table 46</u> **shall** be used for 12x to 3-4x cables.

Note

Cable signal nets **shall** be connected from each *transmit* signal pair on the source port to the appropriate *receive* signal pair on the desired destination port. For example, a cable from port y to port z should be wired to connect IBtyOp(0) (positive output signal from port y, bit 0), to IBtzIp(0) (positive input to port z, bit 0) and IBtyOn(0) to IBtzIn(0), as shown in <u>Table 46</u>.

Table 46 12x to 3-4x cable connector signal assignment

Plug 1		Plug number		
Pin number	Signal		Pin number	Signal
G1-G25	Signal Ground	2	G1-G9	Signal Ground
		3	G1-G9	Signal Ground
		4	G1-G9	Signal Ground

Plug 1		Plug number		
Pin number	Signal		Pin number	Signal
S1	IBtx.1lp(0)	2	S16	IBtx.1Op(0)
S2	IBtx.1In(0)	2	S15	IBtx.1On(0)
S3	IBtx.1lp(1)	2	S14	IBtx.1Op(1)
S4	IBtx.1In(1)	2	S13	IBtx.1On(1)
S5	IBtx.1lp(2)	2	S12	IBtx.1Op(2)
S6	IBtx.1In(2)	2	S11	IBtx.1On(2)
S7	IBtx.1lp(3)	2	S10	IBtx.1Op(3)
S8	IBtx.1In(3)	2	S9	IBtx.1On(3)
S9	IBtx.2lp(0)	3	S16	IBtx.2Op(0)
S10	IBtx.2In(0)	3	S15	IBtx.2On(0)
S11	IBtx.2lp(1)	3	S14	IBtx.2Op(1)
S12	IBtx.2In(1)	3	S13	IBtx.2On(1)
S13	IBtx.2lp(2)	3	S12	IBtx.2Op(2)
S14	IBtx.2In(2)	3	S11	IBtx.2On(2)
S15	IBtx.2lp(3)	3	S10	IBtx.2Op(3)
S16	IBtx.2In(3)	3	S9	IBtx.2On(3)
S17	IBtx.3lp(0)	4	S16	IBtx.3Op(0)
S18	IBtx.3In(0)	4	S15	IBtx.3On(0)
S19	IBtx.3lp(1)	4	S14	IBtx.3Op(1)
S20	IBtx.3In(1)	4	S13	IBtx.3On(1)
S21	IBtx.3lp(2)	4	S12	IBtx.3Op(2)
S22	IBtx.3In(2)	4	S11	IBtx.3On(2)
S23	IBtx.3lp(3)	4	S10	IBtx.3Op(3)
S24	IBtx.3In(3)	4	S9	IBtx.3On(3)
S25	IBtx.3On(3)	4	S8	IBtx.3In(3)
S26	IBtx.3Op(3)	4	S7	IBtx.3lp(3)
S27	IBtx.3On(2)	4	S6	IBtx.3In(2)
S28	IBtx.3Op(2)	4	S5	IBtx.3lp(2)
S29	IBtx.3On(1)	4	S4	IBtx.3In(1)

Table 46 12x to 3-4x cable connector signal assignment

Plug 1		Plug number		
Pin number	Signal		Pin number	Signal
S30	IBtx.3Op(1)	4	S3	IBtx.3lp(1)
S31	IBtx.3On(0)	4	S2	IBtx.3In(0)
S32	IBtx.3Op(0)	4	S1	IBtx.3lp(0)
S33	IBtx.2On(3)	3	S8	IBtx.2In(3)
S34	IBtx.2Op(3)	3	S7	IBtx.2lp(3)
S35	IBtx.2On(2)	3	S6	IBtx.2In(2)
S36	IBtx.2Op(2)	3	S5	IBtx.2lp(2)
S37	IBtx.2On(1)	3	S4	IBtx.2In(1)
S38	IBtx.2Op(1)	3	S3	IBtx.2lp(1)
S39	IBtx.2On(0)	3	S2	IBtx.2In(0)
S40	IBtx.2Op(0)	3	S1	IBtx.2lp(0)
S41	IBtx.1On(3)	2	S8	IBtx.1In(3)
S42	IBtx.1Op(3)	2	S7	IBtx.1lp(3)
S43	IBtx.1On(2)	2	S6	IBtx.1In(2)
S44	IBtx.1Op(2)	2	S5	IBtx.1lp(2)
S45	IBtx.1On(1)	2	S4	IBtx.1In(1)
S46	IBtx.1Op(1)	2	S3	IBtx.1lp(1)
S47	IBtx.1On(0)	2	S2	IBtx.1In(0)
S48	IBtx.1Op(0)	2	S1	IBtx.1lp(0)
Housing	Chassis Ground	2, 3, 4	Housing	Chassis Ground

Table 46 12x to 3-4x cable connector signal assignment

7.8 ACTIVE CABLES

It is desirable to provide for the development of cable assemblies or other devices which plug into cable receptacles which incorporate active circuitry. This would include but isn't limited to cables with built-in repeaters and copper cable substitutes which incorporate optical transceivers.

7.8.1 ACTIVE CABLE INTERFACE, 4X AND 12X WIDTHS

The active cable interface provides for simultaneous transmit and receive of four or twelve bits of encoded differential data with power available on the board connector for fiber or copper transponder devices that are external to the board. It uses the same board connector as the respective

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	copper cable interface, but with a different pin assi ground pins.	gnment for the signal	1
			2
7.8.1.1 4X ACTIVE CABLE INTERI	FACE BOARD CONNECTOR		3
	This section defines the connector for the 4x active finiBand boards.	e cable interface on In-	4 5
			6
	C7-28.2.6: All 4x InfiniBand active cable plugs shall this board connector.	be intermateable with	7 8
			9
7.8.1.1.1 PIN ASSIGNMENTS			10
	C7-28.2.7: The pin assignment listed in <u>Table 47</u> s	hall be used for the	11
	cluding current limitations on the power pins are de	sage requirements in-	12
	Section 7.8.3, "Active Cable Power," on page 280. I	Power return is by way	13
	of the Signal Ground pins.		14
			15
	The 12 V or 3.3 V Sense signal is used to enable t	he respective voltage	16
	on the Vcc power supply pin used to provide powe	r to the active compo-	17
	nents in the cable. Both signals are considered acti	ve if their voltage level	18
	is between 0.9 V and 2.4 V DC.		19
			20
	C7-28.2.8: Both 12 V and 3.3 V Sense signals s	hall not be active si-	21
	multaneously.		22
			23
	The character 'x' in the signal symbol is the port nu	Imber, as defined in	24
	Section 4.1, "Signal Naming Conventions," on pag	<u>e 69</u> .	25
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			27

Tab	le 47	4x active board	connector	signal	assignm	ent
		Pin Number		Signal		

Pin Number	Signal
G1	Sense-12V
G2-G6, G9	Signal Ground
S1	IBtxIp(0)
S2	IBtxIn(0)
S3	IBtxIp(1)
S4	IBtxIn(1)
S5	IBtxIp(2)
S6	IBtxIn(2)
S7	IBtxIp(3)

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Pin Number	Signal
S8	IBtxIn(3)
S9	IBtxOn(3)
S10	IBtxOp(3)
S11	IBtxOn(2)
S12	IBtxOp(2)
G7	Sense-3.3V
S13	IBtxOn(1)
S14	IBtxOp(1)
G8	Vcc
S15	IBtxOn(0)
S16	IBtxOp(0)
Housing	Chassis Ground

Table 47 4x active board connector signal assignment

7.8.1.1.2 KEYING

It is recommended that the 4x active board and copper cable connectors use the same keying as that for a 4x cable as defined in the *InfiniBand Architecture Specification*, <u>Volume 2</u>, <u>Section 7.4</u>, <u>"4x Interface board connector," on page 220</u>.

7.8.1.2 8X ACTIVE CABLE INTERFACE BOARD CONNECTOR

This section defines the connector for the 8x active cable interface on InfiniBand boards. The active cable interface provides for simultaneous transmit and receive of four bits of encoded differential data with power available on the board connector for fiber or copper transponder devices. It uses the same board connector as the 12x copper cable interface, but with a different pin assignment for the signal ground pins.

C7-28.2.9: All 8x InfiniBand active cable plugs **shall** be intermateable with this board connector.

7.8.1.2.1 PIN ASSIGNMENTS

C7-28.2.10: The pin assignment listed in <u>Table 48</u> **shall** be used for the board connector for active InfiniBand 8x cables. Usage requirements including current limitations on the power pins are described in <u>Section 7.8.3, "Active Cable Power," on page 280</u>. Power return is by way of the Signal Ground pins.

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The 12 V or 3.3 V Sense signal is used to enable the respective voltage on the Vcc power supply pin used to provide power to the active components in the cable. Both signals are considered active if their voltage level is between 0.9 V and 2.4 V DC.

C7-28.2.11: Both 12 V and 3.3 V Sense signals **shall not** be active simultaneously.

The character 'x' in the signal symbol is the port number, as defined in <u>Section 4.1, "Signal Naming Conventions," on page 69</u>.

Pin Number	Signal	14
G1	Sense-12V	16
G2, G4-G10, G12-G22, G25	Signal Ground	17
S1	IBtxIp(0)	18
S2	IBtxIn(0)	20
S3	IBtxIp(1)	21
S4	IBtxIn(1)	22
G3	Vcc	23
S5	IBtxIp(2)	24
S6	IBtxIn(2)	26
S7	IBtxIp(3)	27
	IBtxIn(3)	28
S9	IBtxIp(4)	30
S10	IBtxIn(4)	31
S11	IBtxIp(5)	32
S12	IBtxIn(5)	33
S13	IBtxIp(6)	35
	IBtxIn(6)	36
S15	IBtxIp(7)	37
S16	IBtxIn(7)	38
S17	reserved	40
	reserved	41
		42

Table 48 8x active board connector signal assignment

Table 48 8x active board connector signal assignment

Pin Number	Signal	2
G11	Vcc	3
S19	reserved	5
S20	reserved	6
S21	reserved	7
S22	reserved	8
S23	reserved	10
S24	reserved	11
	reserved	12
	reserved	13
\$27	reserved	14
\$28	reserved	16
S20	reserved	17
S20	reserved	18
S30	reserved	19
531	reserved	20
S32	reserved	22
\$33	IBtxOn(7)	23
S34	IBtxOp(7)	24
S35	IBtxOn(6)	25
S36	IBtxOp(6)	20
S37	IBtxOn(5)	28
S38	IBtxOp(5)	29
S39	IBtxOn(4)	30
S40	IBtxOp(4)	31
S41	IBtxOn(3)	33
S42	IBtxOp(3)	34
S43	IBtxOn(2)	35
S44	IBtxOp(2)	36
G23	Sense-3.3V	37
	IBtxOn(1)	39
	IBtxOp(1)	40
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Table 48 8x active board connector signal assignment

Pin Number	Signal
G24	Vcc
S47	lBtxOn(0)
S48	IBtxOp(0)
Housing	Chassis Ground

7.8.1.2.2 KEYING

It is recommended that the 8x active board and copper cable connectors use the same keying as that for a 12x cable as defined in the *InfiniBand Architecture Specification*, <u>Volume 2</u>, <u>Chapter 7: Copper Cable</u>.

7.8.1.3 12x ACTIVE CABLE INTERFACE BOARD CONNECTOR

This section defines the connector for the 12x active cable interface on InfiniBand boards. The active cable interface provides for simultaneous transmit and receive of four bits of encoded differential data with power available on the board connector for fiber or copper transponder devices. It uses the same board connector as the 12x copper cable interface, but with a different pin assignment for the signal ground pins.

C7-28.2.12: All 12x InfiniBand active cable plugs **shall** be intermateable with this board connector.

7.8.1.3.1 PIN ASSIGNMENTS

C7-28.2.13: The pin assignment listed in <u>Table 49</u> **shall** be used for the board connector for InfiniBand 12x active cables. Usage requirements including current limitations on the power pins are described in <u>Section 7.8.3, "Active Cable Power," on page 280</u>. Power return is by way of the Signal Ground pins.

The 12 V or 3.3 V Sense signal is used to enable the respective voltage on the Vcc power supply pin used to provide power to the active components in the cable. Both signals are considered active if their voltage level is between 0.9 V and 2.4 V DC.

C7-28.2.14: Both 12 V and 3.3 V Sense signals **shall not** be active simultaneously.

The character 'x' in the signal symbol is the port number, as defined in <u>Section 4.1, "Signal Naming Conventions," on page 69</u>.

Pin Number	Signal	4
G1	Sense-12V	Ļ
, G4-G10, G12-G22, G25	Signal Ground	- 6
S1	IBtxIp(0)	-
\$2	IBtxIn(0)	
\$3	IBtxIp(1)	- ,
S4	IBtxIn(1)	
G3	Vcc	-
	IBtxlp(2)	
S6	IBtxIn(2)	
S7	IBtxlp(3)	
58	IBtxIn(3)	-
50	IBtxIn(3)	
39	IBtxtp(4)	
510	IBtxin(4)	
S11	lBtxlp(5)	
S12	lBtxIn(5)	
S13	IBtxIp(6)	
S14	lBtxIn(6)	4
S15	IBtxIp(7)	
S16	lBtxIn(7)	
S17	lBtxlp(8)	
S18	IBtxIn(8)	_
G11	Vcc	_
S19	IBtxIp(9)	_
S20	IBtxIn(9)	
	IBtxlp(10)	_
	IBtxIn(10)	-
	IBtyln(11)	_
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Table 49 12

2x active board	tive board connector signal assignment	
Pin Number	Signal	2
S26	IBtxOp(11)	4

Table 49 12

S26	IBtxOp(11)	
S27	IBtxOn(10)	
S28	IBtxOp(10)	
S29	lBtxOn(9)	
S30	IBtxOp(9)	
S31	lBtxOn(8)	
S32	IBtxOp(8)	
S33	lBtxOn(7)	
S34	IBtxOp(7)	
S35	lBtxOn(6)	
S36	IBtxOp(6)	
S37	lBtxOn(5)	
S38	lBtxOp(5)	
S39	lBtxOn(4)	
S40	IBtxOp(4)	
S41	lBtxOn(3)	
S42	IBtxOp(3)	
S43	lBtxOn(2)	
S44	IBtxOp(2)	
G23	Sense-3.3V	
S45	lBtxOn(1)	
S46	IBtxOp(1)	
G24	Vcc	
S47	lBtxOn(0)	
S48	IBtxOp(0)	
Housing	Chassis Ground	

7.8.1.3.2 KEYING

It is recommended that the 12x active board and copper cable connectors use the same keying as that for a 12x cable as defined in the InfiniBand Architecture Specification, Volume 2, Section 7.5.

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7.8.2 ACTIVE CABLES, 4X, 8X, AND 12X WIDTHS

7.8.2.1 4x ACTIVE CABLE

Note

A 4x active cable used with InfiniBand version 1 (unpowered) board connector pinout will not function.

7.8.2.1.1 4X ACTIVE CABLE CONNECTOR DESCRIPTION

This cable plug uses the same connector as the 4x copper cable described in the *InfiniBand Architecture Specification*, <u>Volume 2</u>, <u>Chapter 7:</u> <u>Copper Cable</u>.

C7-28.2.15: 4x board receptacles used on InfiniBand modules **shall** be intermateable with this active cable connector.

C7-28.2.16: A metal backshell or other means which fully shields the connector **shall** be bonded to the cable bulk shield through a continuous 360 degree contact to minimize EMI (Electromagnetic Interference).

Eight pairs of signals are used, four each for transmit and receive.

7.8.2.1.2 4X ACTIVE CABLE PIN ASSIGNMENT

C7-28.2.17: The pin assignment listed in <u>Table 44</u> **shall** be used for active InfiniBand 4x cables.

C7-28.2.18: V_{cc} shall not be wired through the cable to the other end.

The 12 V or 3.3 V Sense signal is used to enable the respective voltage on the Vcc power supply pin used to provide power to the active components in the cable. Both signals are considered active if their voltage level is between 0.9 V and 2.4 V DC.

C7-28.1.1: Both 12 V and 3.3 V Sense signals shall not be active simultaneously.

Note

Cable signal nets **shall** be connected from each *transmit* signal pair on the source port to the appropriate *receive* signal pair on the desired destination port. For example, a cable from port y to port z should be wired to connect IBtyOp(0) (positive output signal from port y, bit 0), to IBtzIp(0) (positive input to port z, bit 0) and IBtyOn(0) to IBtzIn(0), as shown in <u>Table 50</u>.

Table 50	4x active cable connector signal assignment

Plu	g 1	Plu	g 2
Pin number	Signal	Pin number	Signal
G1	Sense-12V	G9	Signal Ground
G4-G6	Signal Ground	G4-G6	Signal Ground
S1	IBtxIp(0)	S16	IBtxOp(0)
S2	IBtxIn(0)	S15	IBtxOn(0)
G2	Signal Ground	G8	Vcc
S3	IBtxIp(1)	S14	IBtxOp(1)
S4	IBtxIn(1)	S13	IBtxOn(1)
G3	Signal Ground	G7	Sense-3.3V
S5	IBtxIp(2)	S12	IBtxOp(2)
S6	IBtxIn(2)	S11	IBtxOn(2)
S7	IBtxIp(3)	S10	IBtxOp(3)
S8	IBtxIn(3)	S9	IBtxOn(3)
S9	IBtxOn(3)	S8	lBtxIn(3)
S10	IBtxOp(3)	S7	IBtxIp(3)
S11	IBtxOn(2)	S6	lBtxIn(2)
S12	IBtxOp(2)	S5	IBtxIp(2)
G7	Sense-3.3V	G3	Signal Ground
S13	IBtxOn(1)	S4	lBtxIn(1)
S14	IBtxOp(1)	S3	IBtxIp(1)
G8	Vcc	G2	Signal Ground
S15	IBtxOn(0)	S2	IBtxIn(0)
S16	IBtxOp(0)	S1	IBtxIp(0)
G9	Signal Ground	G1	Sense-12V
Housing	Chassis Ground	Housing	Chassis Ground

Copper Cable

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7.8.2.2 8X ACTIVE CABLE

Note

A 8x active cable used with InfiniBand version 1 (unpowered) board connector pinout will not function.

7.8.2.2.1 8X ACTIVE CABLE CONNECTOR DESCRIPTION

This cable plug uses the same connector as the 12x copper cable described in the *InfiniBand Architecture Specification*, <u>Volume 2</u>, <u>Chapter 7:</u> <u>Copper Cable</u>.

C7-28.2.19: 8x Board receptacles used on InfiniBand modules **shall** be intermateable with this active cable connector.

C7-28.2.20: A metal backshell or other means which fully shields the connector **shall** be bonded to the cable bulk shield through a continuous 360 degree contact to minimize EMI (Electromagnetic Interference).

Sixteen pairs of signals are used, eight each for transmit and receive.

7.8.2.2.2 8x ACTIVE CABLE PIN ASSIGNMENT

C7-28.2.21: The pin assignment listed in <u>Table 44</u> **shall** be used for active InfiniBand 8x cables.

C7-28.2.22: V_{cc} shall not be wired through the cable to the other end.

The 12 V or 3.3 V Sense signal is used to enable the respective voltage on the Vcc power supply pin used to provide power to the active components in the cable. Both signals are considered active if their voltage level is between 0.9 V and 2.4 V DC.

C7-28.1.2: Both 12 V and 3.3 V Sense signals shall not be active simultaneously.

Note

Cable signal nets **shall** be connected from each *transmit* signal pair on the source port to the appropriate *receive* signal pair on the desired destination port. For example, a cable from port y to port z should be wired to connect IBtyOp(0) (positive output signal from port y, bit 0), to IBtzIp(0) (positive input to port z, bit 0) and IBtyOn(0) to IBtzIn(0), as shown in <u>Table 44</u>.

Table 51 8x active cable connector signal assignment					
Plu	ıg 1	Plug 2			
Pin number	Signal	Pin number	Signal		
G1	Sense-12V	G25	Signal Ground		
G4-10, G12-22	Signal Ground	G4-10, G12-22	Signal Ground		
S1	IBtxIp(0)	S48	IBtxOp(0)		
S2	IBtxIn(0)	S47	IBtxOn(0)		
G2	Signal Ground	G24	Vcc		
S3	IBtxIp(1)	S46	IBtxOp(1)		
S4	IBtxIn(1)	S45	IBtxOn(1)		
G3	Vcc	G23	Sense-3.3V		
S5	IBtxIp(2)	S44	IBtxOp(2)		
S6	IBtxIn(2)	S43	IBtxOn(2)		
S7	IBtxIp(3)	S42	IBtxOp(3)		
S8	IBtxIn(3)	S41	IBtxOn(3)		
S9	IBtxIp(4)	S40	IBtxOp(4)		
S10	IBtxIn(4)	S39	IBtxOn(4)		
S11	IBtxIp(5)	S38	IBtxOp(5)		
S12	IBtxIn(5)	S37	IBtxOn(5)		
S13	IBtxIp(6)	S36	IBtxOp(6)		
S14	IBtxIn(6)	S35	IBtxOn(6)		
S15	IBtxIp(7)	S34	IBtxOp(7)		
S16	IBtxIn(7)	S33	IBtxOn(7)		
S17	reserved	S32	reserved		
S18	reserved	S31	reserved		
S19	reserved	S30	reserved		
S20	reserved	S29	reserved		
G11	Vcc	G16	Signal Ground		
S21	reserved	S28	reserved		
S22	reserved	S27	reserved		

Plug 1		PI	Plug 2	
Pin number	Signal	Pin number	Signal	
S23	reserved	S26	reserved	
S24	reserved	S25	reserved	
S25	reserved	S24	reserved	
S26	reserved	S23	reserved	
S27	reserved	S22	reserved	
S28	reserved	S21	reserved	
S29	reserved	S20	reserved	
S30	reserved	S19	reserved	
G16	Signal Ground	G11	Vcc	
S31	reserved	S18	reserved	
S32	reserved	S17	reserved	
S33	IBtxOn(7)	S16	IBtxIn(7)	
S34	IBtxOp(7)	S15	IBtxIp(7)	
S35	IBtxOn(6)	S14	IBtxIn(6)	
S36	IBtxOp(6)	S13	IBtxIp(6)	
S37	IBtxOn(5)	S12	IBtxIn(5)	
S38	IBtxOp(5)	S11	IBtxIp(5)	
S39	IBtxOn(4)	S10	IBtxIn(4)	
S40	IBtxOp(4)	S9	IBtxIp(4)	
S41	IBtxOn(3)	S8	IBtxIn(3)	
S42	IBtxOp(3)	S7	IBtxlp(3)	
S43	IBtxOn(2)	S6	IBtxIn(2)	
S44	IBtxOp(2)	S5	IBtxlp(2)	
G23	Sense-3.3V	G3	Vcc	
S45	IBtxOn(1)	S4	IBtxIn(1)	
S46	IBtxOp(1)	S3	IBtxIp(1)	
G24	Vcc	G2	Signal Ground	
S47	IBtxOn(0)	S2	IBtxIn(0)	
S48	IBtxOp(0)	S1	IBtxIp(0)	

Table 51 8x active cable connector signal assignment

Table 51 8x active cable connector signal assignment

Plu	ıg 1	Plu	g 2
Pin number	Signal	Pin number	Signal
G25	Signal Ground	G1	Sense-12V
Housing	Chassis Ground	Housing	Chassis Ground

7.8.2.3 12x ACTIVE CABLE

Note

A 12x active cable used with InfiniBand version 1 (unpowered) board connector pinout will not function.

7.8.2.3.1 12x ACTIVE CABLE CONNECTOR DESCRIPTION

This cable plug uses the same connector as the 12x copper cable described in the *InfiniBand Architecture Specification*, <u>Volume 2</u>, <u>Chapter 7</u>: <u>Copper Cable</u>.

C7-28.2.23: 12x board receptacles used on InfiniBand modules **shall** be intermateable with this active cable connector.

C7-28.2.24: A metal backshell or other means which fully shields the connector **shall** be bonded to the cable bulk shield through a continuous 360 degree contact to minimize EMI (Electromagnetic Interference).

Twenty-four pairs of signals are used, twelve each for transmit and receive.

7.8.2.3.2 12x ACTIVE CABLE PIN ASSIGNMENT

C7-28.2.25: The pin assignment listed in <u>Table 52</u> **shall** be used for Infini-Band 12x active cables.

C7-28.2.26: V_{cc} shall not be wired through the cable to the other end.

The 12 V or 3.3 V Sense signal is used to enable the respective voltage on the Vcc power supply pin used to provide power to the active components in the cable. Both signals are considered active if their voltage level is between 0.9 V and 2.4 V DC.

C7-28.1.3: Both 12 V and 3.3 V Sense signals shall not be active simultaneously.

Note

Cable signal nets **shall** be connected from each *transmit* signal pair on the source port to the appropriate *receive* signal pair on the desired destination port. For example, a cable from port y to port z should be wired to connect IBtyOp(0) (positive output signal from port y, bit 0), to IBtzIp(0) (positive input to port z, bit 0) and IBtyOn(0) to IBtzIn(0), as shown in <u>Table 44</u>.

Table 52 12x active cable connector signal assignment

Plu	ıg 1	Plu	g 2
Pin number	Signal	Pin number	Signal
G1	Sense-12V	G25	Signal Ground
G4-10, G12-22	Signal Ground	G4-10, G12-22	Signal Ground
S1	IBtxIp(0)	S48	IBtxOp(0)
S2	IBtxIn(0)	S47	IBtxOn(0)
G2	Signal Ground	G24	Vcc
S3	IBtxlp(1)	S46	IBtxOp(1)
S4	IBtxIn(1)	S45	IBtxOn(1)
G3	Vcc	G23	Sense-3.3V
S5	IBtxIp(2)	S44	IBtxOp(2)
S6	IBtxIn(2)	S43	IBtxOn(2)
S7	IBtxIp(3)	S42	IBtxOp(3)
S8	IBtxIn(3)	S41	IBtxOn(3)
S9	IBtxIp(4)	S40	IBtxOp(4)
S10	IBtxIn(4)	S39	IBtxOn(4)
S11	IBtxIp(5)	S38	IBtxOp(5)
S12	IBtxIn(5)	S37	IBtxOn(5)
S13	IBtxIp(6)	S36	IBtxOp(6)
S14	IBtxIn(6)	S35	IBtxOn(6)
S15	IBtxIp(7)	S34	IBtxOp(7)

Plug 1		Plug 2	
Pin number	Signal	Pin number	Signal
S16	IBtxIn(7)	S33	lBtxOn(7)
S17	IBtxIp(8)	S32	IBtxOp(8)
S18	IBtxIn(8)	S31	IBtxOn(8)
S19	IBtxIp(9)	S30	IBtxOp(9)
S20	IBtxIn(9)	S29	IBtxOn(9)
G11	Vcc	G16	Signal Ground
S21	lBtxlp(10)	S28	IBtxOp(10)
S22	lBtxIn(10)	S27	IBtxOn(10)
S23	IBtxIp(11)	S26	IBtxOp(11)
S24	lBtxIn(11)	S25	IBtxOn(11)
S25	IBtxOn(11)	S24	lBtxIn(11)
S26	IBtxOp(11)	S23	lBtxlp(11)
S27	IBtxOn(10)	S22	lBtxIn(10)
S28	IBtxOp(10)	S21	lBtxlp(10)
S29	IBtxOn(9)	S20	IBtxIn(9)
S30	IBtxOp(9)	S19	IBtxIp(9)
G16	Signal Ground	G11	Vcc
S31	IBtxOn(8)	S18	IBtxIn(8)
S32	IBtxOp(8)	S17	IBtxIp(8)
S33	IBtxOn(7)	S16	IBtxIn(7)
S34	IBtxOp(7)	S15	IBtxIp(7)
S35	IBtxOn(6)	S14	IBtxIn(6)
S36	IBtxOp(6)	S13	IBtxIp(6)
S37	IBtxOn(5)	S12	IBtxIn(5)
S38	IBtxOp(5)	S11	IBtxIp(5)
S39	IBtxOn(4)	S10	IBtxIn(4)
S40	IBtxOp(4)	S9	IBtxIp(4)
S41	IBtxOn(3)	S8	IBtxIn(3)
S42	IBtxOp(3)	S7	IBtxIp(3)

Table 52 12x active cable connector signal assignment

Р	lug 1	Р	lug 2
Pin number	Signal	Pin number	Signal
S43	IBtxOn(2)	S6	IBtxIn(2)
S44	IBtxOp(2)	S5	IBtxIp(2)
G23	Sense-3.3V	G3	Vcc
S45	IBtxOn(1)	S4	IBtxIn(1)
S46	IBtxOp(1)	S3	IBtxIp(1)
G24	Vcc	G2	Signal Ground
S47	IBtxOn(0)	S2	IBtxIn(0)
S48	IBtxOp(0)	S1	IBtxIp(0)
G25	Signal Ground	G1	Sense-12V
Housing	Chassis Ground	Housing	Chassis Ground

Table 52 12x active cable connector signal assignment

7.8.3 ACTIVE CABLE POWER

7.8.3.1 INTRODUCTION

This section defines the power use and control of the power provided for active cables as defined in the section of this specification on active cables. This power is provided to enable the construction of active devices such as repeaters and electro-optical converters which plug into Infini-Band version 2 Cable receptacles.

Since the active cable board connectors are intermateable with legacy InfiniBand cables, the associated power supplies must tolerate having their outputs shorted to ground for an indefinite period. Sense pins are supplied to assist in managing and switching the power supply output.

7.8.3.2 LOCAL DC-DC POWER CONVERTER(S)

The IB active cable will generate the design specific voltages from the supplied active cable voltage. These converters will be located in the Active Cable assembly.

7.8.3.3 POWER

The current and voltage specifications are intended to ensure support of active cable assemblies with power consumption at 12V of up to 4 W for a 4x interface and 10W for a 12x interface, and power consumption at 3.3V of up to 1.56 W for a 4x interface and 5.1W for a 12x interface. They are also intended to assure that current per ACP (Vcc) power pin is limited, to control connector heating.

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7.8.3.4 VOLTAGE

	C7-28.2.27: The Active Cable Power 12V (ACP12) voltage shall be a minimum of 10 volts at maximum current and 14 volts maximum at any current from zero to maximum, measured at the Vcc pins at the cable receptacle.
	C7-28.2.28: The Active Cable Power 3.3V (ACP3) voltage shall be a minimum of 3.13 volts at maximum current and 3.47 volts maximum at any current from zero to maximum, measured at the Vcc pins at the cable receptacle.
7.8.3.5 CURRENT	
	C7-28.2.29: The Active Cable Power 12V (ACP12) interface shall be capable of supplying a minimum of 400 mA at 10V for a 4x interface and 1000 mA at 10V for a 12x interface.
	C7-28.2.30: Each end of an active cable assembly using a 12V nominal power supply shall consume a maximum of 400 mA at 10V for a 4x interface, and 1000 mA at 10V for a 12x interface.
	C7-28.2.31: The Active Cable Power 3.3V (ACP3) shall be capable of supplying a minimum of 500 mA at 3.13V for a 4x interface and 1.5 A at 3.13V for a 12x interface.
	C7-28.2.32: Each end of an active cable assembly using a 3.3V nominal power supply shall consume a maximum of 500 mA at 3.13V for a 4x interface and 1.5 A at 3.13V for a 12x interface. Each end of an active cable assembly using a 3.3V nominal power supply shall consume a maximum of 500 mA per ACP (Vcc) power pin in the receptacle at the maximum voltage of 3.47V for the Active Cable Power 3.3V (ACP3) interface.
	C7-28.2.33: An active cable assembly shall consume a maximum of 500 mA per ACP (Vcc) power pin in the receptacle at the maximum voltages of 14V for Active Cable Power 12V (ACP12) interface and 3.47V for the Active Cable Power 3.3V (ACP3) interface.
	Note that the number of pins varies with the width of the port as defined in the section of this specification on active cables. Note also that, in this version of the specification, 8x links use the 12x interface, and are subject to 12x power specifications.
7.8.3.6 SENSE	
	C7-28.2.34: The active cable assembly shall connect a 5K +/- 5% resistor from SENSE-3.3V or SENSE-12V to ground to enable the active

cable power.

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	C7-28.2.35: The ACP circuitry shall only enable p when the presence of the SENSE resistor is detec nected to ground, or is open (no cable), ACP shall	ower to the receptacle ted. If SENSE is con- be disabled.	 2
7.8.3.7 HOT PLUGGING		4	1
	C7-28.2.36: The active cable power shall detect and provide full current availability within 50 millise	t the sense pin value 5 conds. 6	5
7.8.3.8 SHORT CIRCUIT PROTECT	ION	7	7
	C7-28.2.37: The active cable power supply sha indefinite connection to ground and shall limit short than 50 mA when the equivalent load resistance is	Il protect itself against 9 t circuit current to less 1 less than 1 ohm.)) (11
7.8.3.9 LOAD IMPEDANCE		1	12
	C7-28.2.38: The load shall present a maximum draw of 500 mA in parallel with a maximum capacit farads on any Active Cable Power pin. The load sh drawn to 500 mA from any power pin.	steady state current tance of 500 micro- nall limit the current	3 4 5 6
7.8.3.10 AUXILIARY POWER		1	18
	C7-28.2.39: Active Cable Power shall not be ac is not available.	tive when Bulk Power 1	19 20
78311 BYDASSING		2	21
	C7-28.2.40: All active cable power pins, includin vide a low impedance to ground at frequencies from times the maximum bit rate supported on the port. T provided on both the cable assembly and the reception of the power provided on both the cable assembly and the reception of the power provided on both the cable assembly and the reception of the power provided on both the cable assembly and the reception of the power provided on both the cable assembly and the reception of the power provided on both the power power provided on both the power power power provided on both the power po	g sense pins shall pro- n 100 MHz to 0.75 his bypassing shall be ptacle. 2	22 23 24 25 26 27
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CHAPTER 8: FIBER ATTACHMENT - 2.5 GB/s, 5.0 GB/s, & 10 GB/s

8.1 INTRODUCTION This chapter describes the InfiniBand Fiber Attachment for link operation at 2.5 Gb/s (SDR), 5.0 Gb/s (DDR), and 10Gb/s (QDR). This provides effective link bandwidths ranging from 5.0 Gb/s to 120 Gb/s. The Fiber Attachment is a media-level, point-to-point, duplex fiber optic interconnect. A class of very short reach (VSR) fiber optic interconnect options is defined, and is referred to as -SX. A class of longer reach fiber optic interconnect options is defined, and is referred to as -LX. Specifications are provided for each of the interface widths (1x, 4x, 8x, 12x) at one or more distance classes. Certain optical specifications and fiber connector specifications differ between distance classes, and differ between interface width options within a distance class. Except where noted, the specifications contained herein apply to all distance classes for each of the interface width options. 8.2 SCOPE This chapter defines the following attributes for the 2.5, 5.0 & 10.0 GTransfers/second Fiber Attachment: Optical transmission scheme Optical Transmitter mask compliance Jitter compliance Eye safety Optical link budget and distance **Optical Receptacle and Optical Connector Optical Cable Plant** Bulk and Aux power connections. Link encoding **Pluggable Devices** An InfiniBand Optical Transceiver **may** be permanently attached with other electronic components on a printed circuit board, or may be fabricated as a component that plugs-in through the connector housing. Implementation notes are included at the end of this chapter describing recommended arrangements to interface an InfiniBand Optical Trans-

8.3 FIBER ATTACHMENT TECHNOLOGY OPTIONS

Fiber Optic Attachment technology options allowed in this version of the specification are listed in <u>Table 53</u>, <u>Table 54</u>, <u>Table 55</u>. Detailed specifications for these options are provided in the remainder of this chapter.

Table 53 Fiber Optic Attachment Option for SDR (2.5 Gb/s)

	Very short reach (VSR)	Longer reach
1x Wide		
Designation	IB-1x-SX	IB-1x-LX
Wavelength	850nm	1300nm
Connector	dual-LC	dual-LC
Worst-case operating range	2m - 250m using 50/125µm 500MHz.km fiber 2m - 500m using 50/125µm 2000MHz.km fiber 2m - 125m using 62.5/125µm 200MHz.km fiber	2m-10km with single mode fiber
4x Wide		
Designation	IB-4x-SX	IB-4x-LX
Wavelength	850nm	1300nm
Connector	single MPO	dual-SC
Worst-case operating range	2m - 125m using 50/125μm 500MHz.km fiber 2m - 200m using 50/125μm 2000MHz.km fiber 2m - 75m using 62.5/125μm 200MHz.km fiber	2m-10km with single mode fiber
8x & 12x Wide		
Designation	IB-8x-SX, IB-12x-SX	see Note 1
Wavelength	850nm	
Connector	dual MPO	
Worst-case operating range	2m - 125m using 50/125μm 500MHz.km fiber 2m - 200m using 50/125μm 2000MHz.km fiber 2m - 75m using 62.5/125 μm 200MHz.km fiber	

1: 8x wide LX and 12x wide LX links are not defined in this version of the specification.

	Very short reach (VSR)	Longer reach		
1x Wide				
Designation	IB-1x-DDR-SX	IB-1x-DDR-LX		
Wavelength	850nm	1300nm		
Connector	dual-LC	dual-LC		
Worst-case operating range	2m-125m using 50/125µm	2m-10km with single mode fiber		
	500MHz.km fiber			
	2m-200m using 50/125µm			
	2000MHz.km fiber			
	2m-65m using 62.5/125µm			
	200MHz.km fiber			
Ax Wide				
Designation	IB-4x-DDR-SX	IB-DDR-4x-LX		
Wavelength	850nm	see Note 1		
Connector	single MPO			
Worst-case operating range	2m-75m using 50/125um			
worst case operating range	500MHz km fiber			
	2m-150m using 50/125um			
	2000MHz km fibor			
	211-5011 using 62.5/125µ11			
	200MHz.km fiber			
8x & 12x Wide				
Designation	IB-8x-DDR-SX, IB-12x-DDR-SX	IB-12x-DDR-LX		
Wavelength	850nm	see Note 1		
Connector	dual MPO			
Worst-case operating range	2m-75m using 50/125µm			
	500MHz.km fiber			
	2m-150m using 50/125µm			
	2000MHz.km fiber			
	2m-50m using 62.5/125µm			
	200MHz.km fiber			

Table 54 Fiber Optic Attachment Options for DDR (5.0 Gb/s)

1: 4x, 8x and 12x wide DDR LX links are not defined in this specification.

	•	, , , , , , , , , , , , , , , , , , ,
	Very short reach (VSR)	Longer reach
1x Wide		
Designation	IB-1x-QDR-SX	IB-1x-QDR-LX
Wavelength	850nm	1300nm
Connector	dual-LC	dual-LC
Worst-case operating range	2m-82m using 50/125μm 500MHz.km fiber 2m-300m using 50/125μm 2000MHz.km fiber 2m-33m using 62.5/125μm 200MHz.km fiber	2m-10km with single mode fiber
4x Wide		
Designation	IB-4x-QDR-SX	IB-4x-QDR-LX
Wavelength	see Note 1	see Note 1
Connector		
8x & 12x Wide		
Designation	IB-8x-QDR-SX, IB-12x-QDR-SX	IB-8x-QDR-LX, IB-12x-QDR-LX
Wavelength	see Note 1	see Note 1
Connector		

Table 55 Fiber Optic Attachment Options for QDR (10.0 Gb/s)

1: 4x, 8x, and 12x wide QDR SX and LX links are not defined in this specification.

8.4 FIBER ATTACHMENT OVERVIEW

This section provides an overview of the structure, concepts, and mechanisms of the InfiniBand 1x, 4x, 8x, and 12x fiber optic links operating at SDR, DDR, and QDR speeds.

8.4.1 FIBER OPTIC SYSTEM OVERVIEW

A fiber optic link in general conveys InfiniBand signals between two Infini-Band Boards. A fiber optic link used as an external loopback on a single InfiniBand Board is also possible. A fiber optic link consists of a Fiber Optic Cable connected by means of an Optical Connector at each end to a pair of Optical Transceivers. Each Optical Transceiver typically resides on an InfiniBand Board. The Fiber Optic Cable consists of one or more segments of optical fiber, joined together using Fiber Optic Adapters. The Optical Transceiver consists of the following elements:

1) an Optical Transmitter section which converts intermediate electrical signals to InfiniBand-compliant optical signals,

- an Optical Receiver section which converts InfiniBand-compliant optical signals into intermediate electrical signals,
- 3) an Optical Receptacle (which **shall** be single or dual as specified in subsequent sections) into which the Optical Connector plugs,
- 4) a Signal Conditioner section to convert the vendor-specific intermediate electrical signals into InfiniBand-compliant electrical signals which are specified in <u>Chapter 6: High Speed Electrical Signaling -</u> <u>2.5, 5.0, & 10.0 Gb/s</u>,
- 5) In the case of 4x LX a serializer in the transmitter and a de-serializer in the receiver,
- 6) a power management section.

The InfiniBand-compliant optical signal parameters are specified in <u>Sec-</u> <u>tion 8.5</u>. Optical Receptacles and Connectors are specified in <u>Section 8.6</u>. Fiber Optic cables are specified in <u>Section 8.7</u>. Signal Conditioners are specified in <u>Section 8.8</u>.

The Optical Transceiver implements power management functionality (AUX power, beaconing and remote wake-up) as specified in <u>Chapter 14:</u> <u>OS Power Management</u>. Aux power is specified in <u>Section 8.9</u>.

Architecture Note

The intermediate electrical interface within the Optical Transceiver is intended to be vendor-specific and is not specified in this document, although recommended implementations are outlined in <u>Section 8.8</u>. The concept of intermediate electrical signals is intended to facilitate the use of existing optoelectronic components in an InfiniBand architecture with the addition of only a new electrical interface chipset, referred to as a "Signal Conditioner". The Signal Conditioner will typically contain retiming and control functionality to convert the intermediate electrical signals to/from IB-compliant electrical signals. The Signal Conditioner **may** be physically integrated with the optoelectronic components into a solderable or pluggable physical assembly for attachment to an IB board. The intermediate electrical signals are not intended to be connected through the boundaries of the Optical Transceiver.

Implementations are also envisaged wherein an Optical Transceiver converts directly from IB-compliant optical signals to IB-compliant electrical signals.

8.4.2 1x System Overview - SDR, DDR & QDR

C8-1: All 1x Optical Cables shall comply with the requirements in <u>Section</u> <u>8.4.2</u> for respective distance classifications (SX or LX).


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four central positions of the connector, but if present these optional fibers **shall not** be used for IB signals.

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4x optical cable links for SDR, DDR, and QDR differ only in supported data rate.



fiber per direction, and is therefore similar technically similar to an IB-1x-QDR-LX link, but is not identical. It is, rather, a special case of the long-distance SDR 4x link, with unique data serialization, as described in <u>Section 8.4.3.3 on page 290</u>.

C8-2.1.2: All 4x-LX Fiber Optic Cables shall meet <u>Section 8.4.3.2</u>

A 4x-LX optical link carries a duplex 4x link as shown in Figure 67. IB optical signals are generated in the 4x-LX Optical Transmitter using one



both 10GBase-LR and 4x-LX transmitters accept an 8b/10b encoded byte-striped stream across 4 physical lanes. The 4 lanes for 10Gb/s Ethernet run at 3.125 GBd. To serialize the 4 lanes 10GbE removes the 8b/10b encoding from the bytes on the 4 lanes and then recodes using 64b/66b onto one lane. To keep the optical speed for 4x LX similar to 10GBase-LR, 4x LX optical transceivers will directly serialize the 4 lanes to achieve 10.0 Gbd.

A 4x-LX Optical Transmitter **shall** accept an 8b/10b encoded byte striped stream across the 4 physical lanes as described in <u>Chapter 5: Link/Phy</u><u>Interface</u>. The output of the Optical transmitter **shall** serialize the traffic in the following manner:

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The first byte on the cable shall be byte 0 from lane 0, followed by byte 1 from lane 1, then byte 2 from lane 2, then byte 3 from lane 3, then byte 4 from lane 0,... and so on. Each 10 bit byte shall be serialized in bit order starting with bit 0 and ending with bit 9. Refer to Figure 68 for a diagram detailing the transmitter serialization scheme. Lane 0 Lane 1 Lane 2 Lane 3 Byte 8 Byte 9 Byte 10 Byte 11 Byte 4 Byte 5 Byte 6 Byte 7 Byte 0 Byte 1 Byte 2 Byte 3 Byte 7 Byte 6 Byte 5 Byte 4 Time Byte 3 Byte 2 Byte 1 Byte 0 10Gbaud serial stream to Laser Figure 68 4x LX Transmitter Serialization

A 4x-LX Optical Receiver **shall** accept a 8b/10b encoded byte serialized stream as described above from a 4x-LX Transmitter. The output of the Optical Receiver **shall** be a byte-striped stream across 4 lanes as defined in <u>Chapter 5: Link/Phy Interface</u>. Refer to <u>Figure 69</u> for a diagram detailing de-serialization.



Figure 69 4x LX receiver de-serialization

Architecture Note

The transmitter function to serialize 4 lanes of byte striped traffic is fairly straight forward. The receiver is a little more complicated. One method for correctly de-serializing the symbol-multiplexed stream is to use the comma's to align on bytes. Then use the lane identifier information in TS1s and TS2s to rotate the incoming serial stream to align with the correct physical lane.

8.4.4 8x-SX OVERVIEW - SDR & DDR

C8-2.1.4: All 8x-SX Fiber Optic Cables shall meet Section 8.4.4

A 8x-SX optical link carries a duplex 8x link as shown in Figure 70. Typically the fibers are in a ribbon format. IB optical signals are typically generated in the 8x-SX Optical Transmitter using eight lasers and are typically detected in the 8x-SX Optical Receiver using eight photodetectors. To simplify manufacturing, fibers **may** be present in the four extra positions of the connector, but if present these optional fibers **shall** not be used for IB signals.

Each segment of the 8x SX Fiber Optic Cable **shall** have eight multimode fibers for each direction. The 8x-SX Optical Connector **shall** be a dual MPO connector



8.4.5 12x System Overview - SDR, DDR, & QDR

C8-3: All 12x-SX Fiber Optic Cables shall meet Section 8.4.5.

A 12x-SX optical link carries a duplex 12x link as shown in <u>Figure 71</u>. Typically the fibers are in a ribbon format. IB optical signals are typically generated in the 12x-SX Optical Transmitter using twelve lasers and are typically detected in the 12x-SX Optical Receiver using twelve photodetectors.

Each segment of the 12x SX Fiber Optic Cable **shall** have twelve multimode fibers for each direction. The 12x-SX Optical Connector **shall** be a dual MPO connector.



signals. The Optical Transmitter parameters are specified immediately in-

side the optical fiber adjacent to the Optical Transmitter (TP2 of <u>Figure</u><u>74</u>). The Optical Receiver parameters are specified immediately inside the optical fiber adjacent to the Optical Receiver (TP3 of <u>Figure 74</u>). The corresponding fiber optic cable plant specifications are described in <u>Section 8.7</u>.

C8-4: The BER of each lane **shall not** exceed 10^{-12} under any conditions. The optical specifications in this section support meeting this requirement. In particular the Optical Receiver of each lane is expected to operate at a BER of $\leq 10^{-12}$ over lifetime, temperature, and operating range when driven through a cable plant as specified in <u>Section 8.7</u> by an Optical Transmitter data stream compliant with the eye mask, jitter and optical parameter specifications.

Architecture Note

The maximum and minimum of the allowed range of average transmitter power coupled into the fiber are worst-case values to ensure that the specified minimum optical modulation amplitude can reliably be launched despite power supply variations, manufacturing variances, drift due to temperature variations, and aging effects.

The minimum received optical modulation amplitude and maximum average received power together define the input power range which is expected to achieve the required BER. The values specified take into account power penalties caused by the use of an Optical Transmitter and Fiber Optic Cable with a worst-case combination of spectral characteristics, optical modulation amplitude, maximum average power, and pulse shape characteristics.

The Gigabit Ethernet optical link model method of IEEE 802.3z was used to estimate the link performance. This model presently uses the parameters extinction ratio and average optical power. Transmitter and Receiver Optical Modulation Amplitudes were calculated from these data. DDR and QDR performance were estimated using 10GBE. This version uses OMA directly.

C8-5: This compliance statement is obsolete and has been replaced by <u>C8-6.1.1:</u> and <u>C8-6.2.1:</u>

C8-6: All Optical Ports **shall** meet the signal grounding requirements in <u>Chapter 9: Mechanical Specification</u>.

8.5.1 QUIESCENT CONDITION

C8-6.1.1: All Optical Ports **shall** meet the Quiescent conditions and Optical signal Polarity specified in <u>Section 8.5.1</u>, and <u>Section 8.5.2</u>

If an electrical input to an Optical Transmitter is quiescent, then the optical power of that lane **shall not** be modulated. If there are transitions at the electrical input to the Optical Transmitter, then the optical power **shall** be modulated according to the pattern of the transitions.

All parameters for each lane **shall** be met whether the other lanes are individually active or quiescent.

Implementation Note

<u>Chapter 5: Link/Phy Interface</u> includes a description of a beaconing sequence consisting of bursts of transitions separated by quiescent periods. It is recommended that during the quiescent periods DC current continue to flow through the lasers to bias the lasers at least to threshold and ideally to average optical power level. This will ensure that the optical signals meet specification as quickly as possible when the next beaconing burst starts.

8.5.2 OPTICAL SIGNAL POLARITY

C8-6.1.2: All Optical Ports **shall** meet the Optical Signal Polarity specified in <u>Section 8.5.2</u>.

A logic Zero high-speed signaling level at the electrical input to an Optical Transmitter **shall** generate a low level of optical power on the fiber. A logic One high-speed signaling level at the electrical input to an Optical Transmitter **shall** generate a high level of optical power on the fiber.

8.5.3 OPTICAL TRANSMITTER MASK COMPLIANCE FOR LINKS OPERATING AT 2.5 GB/S & 5.0 GB/S

C8-6.2.1: All 1x SX, 1x LX, 4x SX, and 12x SX Optical Ports **shall** meet the Optical Transmitter Mask specified in <u>Section 8.5.3</u> while operating at SDR speed.

C8-6.2.2: All 1x SX, 1x LX, 4x SX, and 12x SX Optical ports **shall** meet the Optical Transmitter Mask specified in <u>Section 8.5.3</u> while operating at DDR speed. For DDR, the O/E converter 3 dB frequency response **shall** be scaled up by a factor of 2 to 3.75 GHz.

8.5.3.1 EYE MASK SPECIFICATION

The optical transmitter pulse shape characteristics are specified in the form of a compliance mask on the eye diagram of <u>Figure 72</u>. This trans-

mitter compliance mask is used to verify the overall response of the Optical Transmitter for rise time, fall time, pulse overshoot, pulse undershoot, and ringing. Compliance with this optical mask is a very good indicator that deterministic effects are within generally acceptable limits, but it does not guarantee compliance with IB jitter specifications.

For uniform measurements, the Optical Transmitter eye **shall** be measured using an O/E converter with a equivalent fourth-order Bessel-Th-ompson response given by:

$$H_P = \frac{105}{105 + 105y + 45y^2 + 10y^3 + y^4}$$

where

$$y = 2.114p$$
 $p = \frac{j\omega}{\omega_r}$ $\omega_r = 2\pi f_r$ $f_r = 1.875GHz$

The O/E converter filter response is based on that described in ITU-T G.957, which provides a physical implementation. The specified O/E converter is only intended to provide uniform measurement and does not represent the noise response of an IB Optical Receiver. An actual SDR (**2.5 GB/S**) IB Optical Receiver has maximum 3dB bandwidth of 2.8 GHz, as specified in <u>Table 65</u>, <u>Table 68</u>, <u>Table 77</u> and <u>Table 83</u>. The IB Optical Receiver maximum 3dB bandwidth does not apply to DDR (**5.0 GB/S**) Receivers.

The reference O/E converter **shall** have 3 dB frequency response of 1.88 GHz. The equivalent response of the 4th order (or higher) Bessel-Thompson reference O/E converter **shall** meet the values listed in <u>Table 56</u> with tolerance **not** exceeding the values listed in <u>Table 57</u>.

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Table 56	Equivalent Response of Reference O/E Converter	2

f/f ₀	f/f _r	Attenuation (dB)	Distortion (UI)
0.15	0.2	0.1	0
0.3	0.4	0.4	0
0.45	0.6	1.0	0
0.6	0.8	1.9	0.002
0.75	1.0	3.0	0.008
0.9	1.2	4.5	0.025
1.0	1.33	5.7	0.044
1.05	1.4	6.4	0.055
1.2	1.6	8.5	0.10
1.35	1.8	10.9	0.14
1.5	2.0	13.4	0.19
2.0	2.67	21.5	0.30

Table 57 Attenuation Tolerance of Reference O/E Converter

Reference Frequency	Attenuation Tolerance
f/f _r	∆a (dB)
0.1 - 1.00 1.00 2.00	-0.0 + 0.5 +0.5 +3.0
NOTE – Intermediate values of ∆a shall frequency scale.	l be linearly interpolated on a logarithmic

The Optical Transmitter compliance mask used for compliance testing **shall** be as in Figure 72. In this figure the amplitude has been normalized such that an amplitude of 0.0 represents logic ZERO and an amplitude of 1.0 represents logic ONE.



Figure 72 Normalized Optical Transmitter Compliance Mask

8.5.3.2 RISE/FALL TIME MEASUREMENT

Optical rise and fall time specifications are based on unfiltered waveforms. Some lasers have ringing or overshoot, which can reduce the accuracy of 20%-80% rise and fall time measurements. Therefore the 4thorder Bessel-Thompson filter defined in <u>Section 8.5.3.1</u> is a convenient filter for measurement of the rise and fall time. Since the limited response of the 4th-order Bessel-Thompson filter will adversely impact the measured response, the following equation should be used to remove the filter response from the rise and fall times:

$$T_{rise} = \sqrt{\left(T_{riseMeasured}\right)^2 - \left(T_{riseFilter}\right)^2}$$

$$T_{fall} = \sqrt{(T_{fallMeasured})^2 - (T_{fallFilter})^2}$$

The filter 3 dB bandwidth used in the measurement **may** be different than the specified reference filter, but any filter used in the measurement **shall** be a fourth order Bessel-Thompson filter.

8.5.3.3 RMS RISE/FALL TIME

Optical rise time and fall time will not be identical in a typical implementation. Optical link models such as the IEEE 802.3z Gigabit Ethernet optical link model are generally defined using the larger of rise time and fall time. This provides an overly pessimistic analysis. Therefore IB optical specifications are defined using T_{rfRMS} , which is the RMS mean of rise time and fall time as defined below:

$$T_{rfRMS} = \sqrt{\frac{\left(T_{rise}\right)^2 + \left(T_{fall}\right)^2}{2}}$$

8.5.3.4 OPTICAL MODULATION AMPLITUDE

Optical Modulation Amplitude (OMA) is defined as the absolute difference between the optical power of a logic ONE level and the optical power of a logic ZERO level. *OMA* is related to Extinction Ratio (*ER* measured in dB) and Average Optical Power (P_{ave} measured in dBm) by the equation:

$$OMA = 2 \times 10^{P_{ave}/10} \times \frac{(1 - 10^{-ER/10})}{(1 + 10^{-ER/10})}$$

8.5.4 OPTICAL TRANSMITTER MASK COMPLIANCE FOR LINKS OPERATING AT 10.0 GB/S 8.5.4.1 1x QDR OPTICAL TRANSMITTER MASK COMPLIANCE - SX & LX

C8-6.2.3: The 1x SX and 1x LX Optical ports **shall** meet the Optical Transmitter Mask requirements in <u>Section 8.5.4.1</u> while operating at QDR speed (**10.0 GB/s**).

The 1x SX Optical Port shall meet the Optical Transmitter Mask as defined for 10GBASE-SR in **ANSI/IEEE P802.3ae-2002® 10Gb/s Ethernet**. 1x SX QDR **shall** use the same transmit and receive optical interface and budget specifications and measurements, with the following notes and exceptions:

The nominal signaling speed shall be 10.0 GBaud <u>+100ppm</u>

The 1x LX QDR Optical Port shall meet the Optical Transmitter Mask as defined for 10GBASE-LR in **ANSI/IEEE P802.3ae-2002® 10Gb/s Eth-ernet**. 1x LX QDR **shall** use the same transmit and receive optical interface and budget specifications and measurements, with the following notes and exceptions:

• The nominal signaling speed shall be 10.0 GBaud <u>+</u>100ppm

8.5.4.2 4x LX OPTICAL TRANSMITTER MASK COMPLIANCE

C8-6.1.3: All 4x-LX Optical Ports **shall** meet the Optical Transmitter Mask specified in <u>Section 8.5.4.2</u>.

Footnote 73. The 4x LX Optical Port **shall** meet the Optical Transmitter Mask as defined for 10GBASE-LR in **ANSI/IEEE P802.3ae-2002® 10Gb/s Ethernet**. 4x LX **shall** use the same transmit and receive optical interface and budget specifications and measurements, with the following notes and exceptions:

The nominal signaling speed shall be 10.0 GBaud <u>+</u>100ppm

8.5.5 OPTICAL JITTER SPECIFICATION FOR LINKS OPERATING AT 2.5 GB/S AND 5.0 GB/S

C8-7: This compliance statement is obsolete and has been replaced by <u>C8-7.2.1:</u>

8.5.5.1 1x SX, 1x LX, 4x SX, and 12x SX Optical Jitter Specifications for 2.5 GB/s and 5.0 GB/s

C8-7.1.1: This compliance statement is obsolete and has been replaced by <u>C8-7.2.1:</u>

C8-7.1.2: This compliance statement is obsolete and has been replaced by <u>C8-7.2.4:</u>

C8-7.2.1: All 1x-SX,1x-LX, 4x-SX, and 12x-SX Optical Ports shall comply with the Jitter requirements in <u>Section 8.5.5.1</u> for respective Link widths/distances as defined in <u>Table 58</u> while operating at SDR speed.

C8-7.2.2: All 1x-SX,1x-LX, 4x-SX, and 12x-SX Optical Ports shall comply with the Jitter requirements in <u>Section 8.5.5.1</u> for respective Link widths/distances as defined in <u>Table 59</u> while operating at DDR speed.

The IB jitter specification is based on the same methodology as the Fibre Channel - Methodologies for Jitter Specification revision 10.0 and the IEEE 802.3z Gigabit Ethernet standards. Figure 74 shows jitter compliance test points TP1, TP2, TP3 and TP4 for an IB-1x optical link.

TP2 is located immediately inside the output end of a test fiber of 2m length plugged into the Optical Transmitter and wrapped 10 turns around a 25.4mm-diameter mandrel, and it is the test point at which all Optical Transmitter optical parameters are defined. TP3 is located immediately inside the optical fiber adjacent to the Optical Receiver, and is the location at which all Optical Receiver optical parameters are defined. TP1 is located at the vendor-specific intermediate electrical signals within the Optical Transmitter. TP4 is located at the vendor-specific intermediate electrical signals within the Optical Receiver. The physical existence of TP1 and TP4 is optional.

Test points for 4x-SX, 8x-SX and 12x-SX links are defined similarly to those for 1x.

Cables.



The total jitter listed for TP4 in <u>Table 58</u> does not include a sinusoidal jitter (SJ) component.

InfiniBand	Compliance	Determini	stic Jitter	Total Jitter	
Link	Point	UI	ps	UI	ps
1x-SX, 1x-LX	TP1 (input test jitter)	0.10	40	0.25	100
	TP2	0.23	92	0.46	184
	TP3	0.30	120	0.54	216
	TP4	0.40	160	0.70	280
4x-SX, 12x-SX	TP1 (input test jitter)	0.10	40	0.25	100
	TP2	0.25	100	0.48	192
	TP3	0.30	120	0.53	212
	TP4	0.40	160	0.70	280

Table 58 Maximum Jitter of Optical Links for SDR

When operating at DDR speed, IB optical links **shall** not exceed the deterministic and total jitter values listed in <u>Table 59</u> at TP2 and TP3 when the input jitter to the Optical Transceiver is compliant with the IB electrical specification.

InfiniDend Link	Compliance	Deterministic Jitter		Deterministic Jitter		Total Jitter	
InfiniBand Link	Point	UI	ps	UI	ps		
1x-SX, 1x-LX	TP1 (input test jitter)	0.14	28	0.26	52		
	TP2	0.26	52	0.452	90.4		
	TP3	0.265	53	0.58	116.1		
	TP4	0.365	72.6	0.756	151.1		
4x-SX, 8x-SX, 12x-SX	TP1 (input test jitter)	0.10	20	0.25	50		
	TP2	0.22	44	0.443	89		
	TP3	0.22	44.6	0.538	108		
	TP4	0.32	64	0.757	151		

Table 59 Maximum Jitter of Optical Links for DDR

For all link types, the Signal Conditioner or other component connected at TP4 **shall** tolerate total jitter of 0.80 UI for SDR (**2.5 GB/s**) and 0.085 for DDR (**5.0 GB/s**), which includes 0.10 UI of sinusoidal jitter (SJ) over a swept frequency from 1.5 MHz to1250 MHz as defined in Figure 75.



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Architecture Note - Jitter Table 58 and Table 59 specify total jitter (TJ) at BER of 10⁻¹² and specifies deterministic jitter (DJ). Random jitter (RJ) can be calculated from TJ and DJ: RJ = TJ - DJ, where RJ is 14σ for BER of 10^{-12} . DJ's of successive physical components add linearly. RJ's add in quadrature. TJ values can only be added by breaking them down into DJ and RJ components. Jitter values are specified at each test point TP1, TP2, TP3, TP4. To determine the amount of deterministic jitter and random jitter that an Optical Transmitter under test adds from TP1 to TP2, the following analysis applies: DJ(Transmitter) = DJ2 - DJ1 $RJ(Transmitter) = \sqrt{(TJ2 - DJ2)^2 - (TJ1 - DJ1)^2}$ where DJ1 = DJ at TP1 DJ2 = DJ at TP2TJ1 = TJ at TP1TJ2 = TJ at TP2A similar analysis using TP3 and TP4 applies to testing an Optical Receiver.

8.5.6 OPTICAL JITTER SPECIFICATIONS FOR LINKS OPERATING AT 10.0 GB/S

8.5.6.1 1x SX QDR AND 1x LX QDR OPTICAL JITTER SPECIFICATIONS

C8-7.2.3: All 1x-QDR-SX and 1x-QDR-LX Optical Ports shall comply with the Jitter requirements in <u>Section 8.5.6.2</u> while operating at QDR speed.

The 1x SX QDR Optical Port shall meet the Optical Jitter specifications as defined for 10GBASE-SR in **ANSI/IEEE P802.3ae-2002 10Gb/s Ethernet**. 4x SX QDR **shall** use the same transmit and receive optical interface and budget specifications and measurements, with the following notes and exceptions:

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	• The nominal signaling speed shall be 10.0 GBaud ±	100ppm
	The 1x LX QDR and Optical Port shall meet the Optical Jitter s defined for 10GBASE-LR in ANSI/IEEE P802.3ae-2002 10 4x LX QDR shall use the same transmit and receive optic budget specifications and measurements, with the followin ceptions:	specifications as I Gb/s Ethernet . cal interface and ing notes and ex-
	• The nominal signaling speed shall be 10.0 GBaud ±	100ppm
8.5.6.2 4x LX OPTICAL JITTER S	SPECIFICATIONS	
	C8-7.2.4: All 4x-LX Optical Ports shall comply with the Jit in <u>Section 8.5.6.2</u> .	ter requirements
	The 4x LX Optical Port shall meet the Optical Jitter spec fined for 10GBASE-LR in ANSI/IEEE P802.3ae-2002 10 4x LX shall use the same transmit and receive optical in budget specifications and measurements, with the followin ceptions:	ifications as de- I Gb/s Ethernet . Iterface and ing notes and ex-
8.5.7 BIT TO BIT SKEW	The nominal signaling speed shall be 10.0 GBaud <u>+</u>	100ppm
	C8-8: All IB optical ports shall not exceed the Maximum lowed across all physical lanes as defined in <u>Table 60</u> will SDR speed.	New values al- hile operating at
	C8-8.2.1: All InfiniBand optical ports shall not exceed the Skew values allowed across all physical Lanes as define while operating at DDR speed.	ne Maximum ed in <u>Table 61</u>
	C8-8.2.2: All InfiniBand optical ports shall not exceed the Skew values allowed across all physical Lanes as define while operating at QDR speed.	he Maximum ed in <u>Table 62</u>
	Table 60 defines the allowable bit to bit skew across the p optical components. All IB optical ports shall limit skew to values defined in <u>Table 60</u> when operating at SDR speed ports shall limit skew to the maximum values defined in <u>Table 61</u> erating at DDR speed. All IB optical ports shall limit skew values defined in <u>Table 62</u> when operating at QDR speed	hysical lanes for to the maximum d. All IB optical <u>able 61</u> when op- to the maximum d.

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Table 60 Maximum Optical Bit to Bit Skew Values for 2.5 Gb/s 2

Skew Parameter	Maximum Value	
Optical Cable Assembly ^a	3.0ns	
Transmitter ^b	500ps	
Receiver ^c	500ps	
a. An optical cable assembly shall include the optical cable and		

appropriate optical connectors at each end of the cable. b. Between any two physical lanes within a transmitter.

c. Between any two physical lanes within a receiver.

Table 61 Maximum Optical Bit to Bit Skew Values for 5.0 Gb/s

Skew Parameter	Maximum Value
Optical Cable Assembly ^a	1.5ns
Transmitter ^b	250ps
Receiver ^c	250ps

a. An optical cable assembly $\ensuremath{\textbf{shall}}$ include the optical cable and

appropriate optical connectors at each end of the cable.

b. Between any two physical lanes within a transmitter.

c. Between any two physical lanes within a receiver.

Table 62 Maximum Optical Bit to Bit Skew Values for 10.0 Gb/s 23 24 24

Skew Parameter	Maximum Value
Optical Cable Assembly ^a	0.75ns
Transmitter ^b	125ps
Receiver ^c	125ps

a. An optical cable assembly **shall** include the optical cable and appropriate optical connectors at each end of the cable.

b. Between any two physical lanes within a transmitter.

c. Between any two physical lanes within a receiver.

8.5.8 1x SDR LINKS - AT 2.5 GB/S

A 1x-SX link operates in the 850nm wavelength band using multimode (MM) fiber. The optical parameters have been selected so as to allow typical 1x-SX Optical Transceivers to use a GaAs Vertical Cavity Surface Emitting Laser (VCSEL) and a photodetector, trans-impedance pre-amplifier and limiting post-amplifier. Three fiber types are specified for 1x-SX:

- i) 1x-SX/50 link: 500MHz.km 50µm / 125µm MM fiber
- ii) 1x-SX/50 link: 2000MHz.km 50µm / 125µm MM fiber

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A 1x-LX link operates in the 1300nm wavelength band using singlemode (SM) fiber. The optical parameters have been selected to allow a typical 1x-LX Optical Transceiver to use an uncooled InP-based Fabry-Perot (FP) laser, Distributed Feedback (DFB) laser or VCSEL laser, and an In-GaAs photodetector, trans-impedance pre-amplifier and limiting post-amplifier. A trade-off curve is provided in Figure 76 between Center Wavelength and RMS Spectral Width to allow designers to select appropriate laser technology while still ensuring link operation. Only one fiber type is specified for 1x-LX: single-mode non-dispersion shifted.

8.5.8.1 1x EYE SAFETY

C8-9: The optical power coupled into the fiber for 1x-SX and 1x-LX **shall** be limited to a maximum value with Class I laser safety operation in accordance with CDRH and IEC 60825-1 Amendment 2 Radiation Safety of Laser Products: Equipment Classification, Requirements and User Guide.

8.5.8.2 1x-SX OPTICAL PARAMETERS

C8-10: This compliance statement is obsolete and has been replaced by <u>C8-10.2.1:</u>.

C8-10.2.1: All 1x-SX Optical Ports shall comply with the Transmitter and Receiver requirements in <u>Section 8.5.8.2</u>.

<u>Table 63</u> gives the link budgets for 1x-SX fiber optic fiber links running at 2.5 GTransfers/second. Fiber plant specifications are described in <u>Section</u> <u>8.7</u>.

Optical Passive Loss is the loss resulting from connections between Fiber Optic Segments (adapters or splices), and attenuation attributable to the fiber cable plant. Optical System Penalty includes all other link penalties other than Optical Passive Loss.

Parameter	IB-1x	IB-1x-SX/50 IB-		-SX/62	1.1	Nete
	Minimum	Maximum	Minimum	Maximum	Units	Note
Baud Rate		2500		2500	Mb/s	
Rate tolerance		<u>+</u> 100		<u>+</u> 100	ppm	

Table 63 Link Parameters - 1x-SX

InfiniBandSM Trade Association

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Table 63 Link Parameters - 1x-SX (Continued)

Demonster	IB-1x	-SX/50	IB-1x-	-SX/62	11	Nete
Parameter	Minimum	Maximum	Minimum	Maximum	Units	Note
Optical Passive Loss		2.44		2.0	dB	
Optical System Penalty		3.56		4.0	dB	
Total link power budget	6		6		dB	
Worst case operating range		2 - 250 ^a 2-500 ^b		2 - 125	m	С
Fiber mode-field (core) diameter		50		62.5	μm	

a. 1x-SX/50 link: 500MHz.km 50µm / 125µm MM fiber

b. 1x-SX/50 link: 2000MHz.km 50µm / 125µm MM fiber

c. Longer operating distance than the range specified here can be achieved using transmitters, receivers and/or cables meeting specification but performing better than worst-case.

> An Optical Transmitter for a 1x-SX link shall meet the parameters specified in Table 64 at TP2.

If any high-speed electrical input signals are less than the V_{RSD} (Signal 21 Threshold) as defined in Chapter 6: High Speed Electrical Signaling - 2.5, 5.0, & 10.0 Gb/s then the optical modulation amplitude shall not exceed 2.0 μW. 24

Table 64 Optical Transmitter Parameters - 1x-SX

Parameter	Minimum	Maximum	Units	Note
Туре	La	aser		
Center Wavelength	830	860	nm	
RMS spectral width		0.85	nm	
Average launched power		-4.0	dBm	а
Optical Modulation Amplitude (OMA)	0.196		mW	b
RMS mean of 20% - 80% Rise/Fall time		150	ps	С
RIN ₁₂ (OMA)		-117	dB/Hz	

a. Average launched power, max. is the lesser of the eye safety limit or Average receiver power, max.

b. Optical modulation amplitude values are peak-to-peak.

c. Optical rise and fall time specifications are based on unfiltered waveforms. See Section 8.5.3.2.

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An Optical Receiver for a 1x-SX link **shall** meet the parameters specified in <u>Table 65</u> at TP3. Conformance testing for a stressed receiver at TP3 **shall** follow the methods of Annex A of Fibre Channel Physical Interface revision 8.0.

If the average received optical power on any Lane is less than -30 dBm then the corresponding high-speed electrical signaling output **shall** be squelched to less than V_{RSD} (Signal Threshold) as defined in <u>Chapter 6:</u> High Speed Electrical Signaling - 2.5, 5.0, & 10.0 Gb/s. The electrical outputs of every lane with a optical power greater than -20dBm **shall not** be squelched.

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Parameter	Minimum	Maximum	Units	Note
Average received power		-1.5	dBm	
Optical modulation amplitude	0.050		mW	а
Return loss of receiver	12		dB	
Stressed receiver sensitivity (OMA)	0.102		mW	а
Stressed receiver ISI test	2.0		dB	
Stressed receiver DCD component of DJ (at Tx)	40		ps	
Receiver electrical 3 dB upper cutoff frequency		2.8	GHz	
Receiver electrical 10 dB upper cutoff frequency		6.0	GHz	

Table 65 Optical Receiver Parameters - 1x-SX

a. Optical modulation amplitude values are peak-to-peak.

8.5.8.3 1x-LX OPTICAL PARAMETERS

C8-11: This compliance statement is obsolete and has been replaced by <u>C8-11.2.1:</u>.

C8-11.2.1: All 1x-LX Optical Ports shall comply with the Transmitter and Receiver requirements in <u>Section 8.5.8.3</u>.

<u>Table 66</u> gives the link budgets for 1x-LX single-mode fiber optic links running at 2.5GTransfers/second. Fiber plant specifications are described in <u>Section 8.7</u>.

Parameter	Minimum	Maximum	Units	Note
Baud Rate		2500	Mb/s	
Rate tolerance		<u>+</u> 100	ppm	
Optical Passive Loss		6.64	dB	
Optical System Penalty		2.36	dB	
Total link power budget	9.0		dB	
Worst case operating range		2 - 10,000	m	а
Fiber mode-field (core) diameter		9	μm	

Table 66 Link Parameters - 1x-LX

a. Longer operating distance than the range specified here can be achieved using transmitters, receivers and/or cables meeting specification but performing better than worst-case.

An Optical Transmitter for a 1x-LX link **shall** meet the parameters specified in <u>Table 67</u> at TP2.

If any high-speed electrical input signals are less than the V_{RSD} (Signal Threshold) as defined in <u>Chapter 6: High Speed Electrical Signaling - 2.5.</u> <u>5.0, & 10.0 Gb/s</u> then the optical modulation amplitude **shall not** exceed 2.0 μ W.

In addition, the RMS spectral width of a 1x-LX Optical Transmitter **shall** lie on or below the curve shown in <u>Figure 76</u> as a function of Optical Transmitter Center Wavelength. The curve was calculated using the worst-case fiber at a given Optical Transmitter Center Wavelength for all operating conditions. Specifically, the zero-dispersion wavelength of the fiber was chosen to be 1324nm for Optical Transmitter Center Wavelengths below approximately 1312nm, and the zero-dispersion wavelength of the fiber

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was chosen to be 1300nm for Optical Transmitter Center Wavelengths above approximately 1312nm.

Table 67 Optical Transmitter Parameters - 1x-LX					
Parameter	Minimum	Maximum	Units	Note	
Туре	La	iser			
Center Wavelength	1270	1360	nm		
RMS spectral width			nm	а	
Average launched power		-3.0	dBm	b	
Optical Modulation Amplitude (OMA)	0.186		mW	С	
RMS mean of 20% - 80% Rise/Fall time		150	ps	d	
RIN ₁₂ (OMA)		-120	dB/Hz		

Table 67 Optical Transmitter Parameters - 1x-I X

a. See text and Figure 76.

b. Average launched power, max. is the lesser of the eye safety limit or Average receiver power, max.

c. Optical modulation amplitude values are peak-to-peak.

d. Optical rise and fall time specifications are based on unfiltered waveforms. See Section 8.5.3.2.

An Optical Receiver for a 1x-LX link shall meet the parameters specified in Table 68 at TP3.

22 If the average received optical power on any Lane is less than -30 dBm 23 then the corresponding high-speed electrical signaling output shall be squelched to less than V_{RSD} (Signal Threshold) as defined in Chapter 6: 24 High Speed Electrical Signaling - 2.5, 5.0, & 10.0 Gb/s. The electrical out-25 puts of every Lane with a optical power greater than -20dBm shall not be 26 squelched. 27

Table 68 Optical Receiver Parameters - 1x-LX

Parameter	Minimum	Maximum	Units	Note
Average received power		-1.5	dBm	
Optical modulation amplitude	0.0234		mW	а
Return loss of receiver	20		dB	

Parameter	Minimum	Maximum	Units	Note	
Stressed receiver sensitivity (OMA)	0.0365		mW	а	
Stressed receiver ISI test	0.58		dB		
Stressed receiver DCD component of DJ (at TX)	40		ps		
Receiver electrical 3 dB upper cutoff frequency		2.8	GHz		
Receiver electrical 10 dB upper cutoff frequency		6.0	GHz		

Table 68 Optical Receiver Parameters - 1x-LX

a. Optical modulation amplitude values are peak-to-peak.



Figure 76 1x-LX Trade-off between RMS Spectral Width and Center Wavelength

8.5.9 1x DDR LINKS - AT 5.0 GB/S

A 1x-DDR-SX link uses similar transmitter, receiver, and fiber technology as 1x-SX links described in <u>Section 8.5.8</u>, and differ in bit rate, and in the parameters described below. A 1x-DDR-LX link also uses similar technology as 1x-LX links described in <u>Section 8.5.8</u>.

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8.5.9.1 EYE SAFETY C8-11.2.2: The optical power coupled into the fiber for 1x-DDR-SX and 2 1x-DDR-LX shall be limited to a maximum value with Class I laser safety 3 operation in accordance with CDRH and IEC 60825-1 Amendment 2 Ra-4 diation Safety of Laser Products: Equipment Classification, Requirements 5 and User Guide. 6 7 8 8.5.9.2 1x-DDR-SX OPTICAL PARAMETERS 9 **C8-11.2.3:** All 1x-DDR-SX Optical Ports shall comply with the Transmitter 10 and Receiver requirements in <u>Section 8.5.9.2</u>. 11 Table 69 gives the link budgets for 1x-DDR-SX fiber optic fiber links running at 5.0 GTransfers/second. Fiber plant specifications are described in 14 Section 8.7. 15 Optical Passive Loss is the loss resulting from connections between Fiber 16 Optic Segments (adapters or splices), and attenuation attributable to the 17 fiber cable plant. Optical System Penalty includes all other link penalties 18 other than Optical Passive Loss. 19 20

Parameter	IB-1x-SX/50 IB-1x-SX/62	SX/50 IB-1x		IB-1x-SX/50		-SX/62	11	Nete
	Minimum	Maximum	Minimum	Maximum	Units	Note		
Baud Rate		5000		5000	Mb/s			
Rate tolerance		<u>+</u> 100		<u>+</u> 100	ppm			
Optical Passive Loss		1.97		1.76	dB			
Optical System Penalty		3.6		4.4	dB			
Total link power budget	7.93		7.93		dB			
Worst case operating range		2 - 125 ^a 2-200 ^b		2 - 65	m	с		
Fiber mode-field (core) diameter		50		62.5	μm			

Table 69 Link Parameters - 1x-DDR-SX

a. 1x-SX/50 link: 500MHz.km 50mm / 125mm MM fiber

b. 1x-SX/50 link: 2000MHz.km 50mm / 125mm MM fiber

c. Longer operating distance than the range specified here can be achieved using transmitters, receivers and/or cables meeting specification but performing better than worst-case.

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An Optical Transmitter for a 1x-DDR-SX link **shall** meet the parameters specified in <u>Table 70</u> at TP2.

Parameter	Minimum	Maximum	Units	Note
Туре	La	aser		
Center Wavelength	830	860	nm	
RMS spectral width		0.85	nm	
Average launched power		-2.0	dBm	а
Optical Modulation Amplitude (OMA)	0.247		mW	b
RMS mean of 20% - 80% Rise/Fall time		75	ps	С
RIN ₁₂ (OMA)		-123	dB/Hz	

Table 70 Optical Transmitter Parameters - 1x-DDR-SX

a. Average launched power, max. is the lesser of the eye safety limit or Average receiver power, max.

b. Optical modulation amplitude values are peak-to-peak.

c. Optical rise and fall time specifications are based on unfiltered waveforms. See Section 8.5.3.2.

An Optical Receiver for a 1x-DDR-SX link **shall** meet the parameters specified in <u>Table 71</u> at TP3. Conformance testing for a stressed receiver at TP3 **shall** follow the methods of Annex A of Fibre Channel Physical Interface revision 8.0.

Table 71 Optical Receiver Parameters - 1x-DDR-SX

Parameter	Minimum	Maximum	Units	Note
Average received power	0.0		dBm	
Optical modulation amplitude (Informa- tive)		0.040 Informative	mW	а
Return loss of receiver	12		dB	
Stressed receiver sensitivity (OMA)	0.074		mW	a ,b
Stressed receiver ISI test		2.48	dB	
Stressed receiver DCD component of DJ (at Tx)	17.0		ps	

a. Optical modulation amplitude values are peak-to-peak.

b. Stressed receiver entries for Sensitivity and ISI differ for each fiber type. The values here apply to 50u, 500 MHz-km fiber.

8.5.9.3 1x-DDR-LX OPTICAL PARAMETERS

C8-11.2.4: All 1x-DDR-LX Optical Ports **shall** comply with the Transmitter and Receiver requirements in <u>Section 8.5.9.3</u>.

<u>Table 72</u> gives the link budgets for 1x-LX single-mode fiber optic links running at 2.5GTransfers/second. Fiber plant specifications are described in <u>Section 8.7</u>.

Parameter	Minimum	Maximum	Units	Note
Baud Rate		5000	Mb/s	
Rate tolerance		<u>+</u> 100	ppm	
Optical Passive Loss		5.66	dB	
Optical System Penalty		2.4	dB	
Total link power budget	9.8		dB	
Worst case operating range		2 - 10,000	m	а
Fiber mode-field (core) diameter		9	μm	

Table 72 Link Parameters - 1x-DDR-LX

a. Longer operating distance than the range specified here can be achieved using transmitters, receivers and/or cables meeting specification but performing better than worst-case.

An Optical Transmitter for a 1x-DDR-LX link **shall** meet the parameters specified in <u>Table 73</u> at TP2.

In addition, the RMS spectral width of a 1x-DDR-LX Optical Transmitter **shall** lie on or below the curve shown in Figure 77 as a function of Optical Transmitter Center Wavelength and minimum Transmit OMA. The curve was calculated using the worst-case fiber at a given Optical Transmitter Center Wavelength for all operating conditions. Specifically, the zero-dispersion wavelength of the fiber was chosen to be 1324nm for Optical Transmitter Center Wavelengths below approximately 1312nm, and the zero-dispersion wavelength of the fiber was chosen to be 1300nm for Optical Transmitter Center Wavelengths above approximately 1312nm.

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Parameter	Minimum	Maximum	Units	Note
Туре	La	ser		
Center Wavelength	1270	1360	nm	
RMS spectral width		0.47	nm	а
Average launched power		-1.0	dBm	b
Optical Modulation Amplitude (OMA)	0.29		mW	С
RMS mean of 20% - 80% Rise/Fall time		75	ps	d
RIN ₁₂ (OMA)		-123	dB/Hz	

Table 73 Optical Transmitter Parameters - 1x-DDP-IX

a. See text and Figure 77.

b. Average launched power, max. is the lesser of the eye safety limit or Average receiver power, max.

c. Optical modulation amplitude values are peak-to-peak.

d. Optical rise and fall time specifications are based on unfiltered waveforms. See Section 8.5.3.2.

An Optical Receiver for a 1x-DDR-LX link shall meet the parameters specified in Table 74 at TP3.

Table 74 Optical Receiver Parameters - 1x-DDR-LX

Parameter	Minimum	Maximum	Units	Note
Average received power	-1.0		dBm	
Optical modulation amplitude (Informa- tive)		0.029 Informative	mW	а
Return loss of receiver	12		dB	
Stressed receiver sensitivity (OMA)	0.030		mW	а
Stressed receiver ISI test	1.45		dB	
Stressed receiver DCD component of DJ (at TX)	16.3		ps	
Receiver electrical 3 dB upper cutoff frequency		5.3	GHz	b
Receiver electrical 10 dB upper cutoff			GHz	2

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Figure 77 1x-DDR-LX Trade-off between OMA, RMS Spectral Width, and Center Wavelength

8.5.10 4x SDR LINKS - AT 2.5 GB/S

C8-12: This compliance statement is obsolete and has been replaced by <u>C8-12.2.1</u>:.

C8-12.1.1: This compliance statement is obsolete and has been replaced by <u>C8-12.2.2</u>.

C8-12.2.1: All 4x-SX Optical Ports **shall** comply with the Eye Safety, Transmitter, and Receiver requirements in <u>Section 8.5.10.1</u> and <u>Section 8.5.10.2</u>.

C8-12.2.2: All 4x-LX Optical Ports **shall** comply with the Eye Safety, Transmitter, and Receiver requirements in <u>Section 8.5.10.3</u> and <u>Section</u> <u>8.5.10.4</u>

A 4x-SX link operates in the 850nm wavelength band using multimode (MM) fiber. The optical parameters have been selected so as to allow typical 4x-SX Optical Transceivers to use an array of GaAs VCSELs and an array of photodetectors, trans-impedance pre-amplifiers and limiting postamplifiers. Three fiber types are specified for 4x-SX:

- i) 4x-SX/50: 500MHz.km 50µm / 125µm MM fiber
- ii) 4x-SX/50: 2000MHz.km 50µm / 125µm MM fiber
- iii) 4x-SX/62: 200MHz.km 62.5µm / 125µm MM fiber

8.5.10.1 4x-SX EYE SAFETY

The optical power emitted from a 4x-SX port shall be limited to a maximum value for Class 1M laser safety in accordance with IEC/EN 60825-1 Amendment 2 Safety of Laser Products, part 1: Equipment classification, requirements, and user's guide and FDA/CDRH 21 CFR 1040.10

For systems that are required to meet existing IEC Class I laser safety regulations, Open Fiber Control (OFC) or other similar vendor-specific protocols **should** be implemented to meet the CDRH and IEC requirement. Any such implementation **shall** be transparent to all InfiniBand layers.

Recommendation to System Designer

Without any form of open fiber control, the power levels specified for the 4x-SX Optical Transmitter will meet the new relaxed specification for IEC Class 1M.

8.5.10.2 4x-SX OPTICAL PARAMETERS

<u>Table 75</u> gives the link budgets for 4x-SX multimode fiber optic links running at 2.5 GTransfers/second. Fiber plant specifications are described in <u>Section 8.7</u>.

Deremeter	IB-4x	-SX/50	IB-4x	-SX/62	Unito	Nata
Farameter	Minimum	Maximum	Minimum	Maximum	Units	Note
Baud Rate		2500		2500	Mb/s	
Rate tolerance		<u>+</u> 100		<u>+</u> 100	ppm	

Table 75 Link Parameters - 4x-SX

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InfiniBandTM Architecture Release 1.2 Fiber Attachment - 2.5 Gb/s, 5.0 Gb/s, & 10 Gb/s **VOLUME 2 - PHYSICAL SPECIFICATIONS**

Table 75 Link Parameters - 4x-SX (Continued)

Devenueter	IB-4x	-SX/50	IB-4x-	-SX/62	Unite	Nete
Parameter	Minimum	Maximum	Minimum	Maximum	Units	Note
Optical Passive Loss		1.9		1.8	dB	
Optical System Penalty		2.9		3.0	dB	
Total link power budget	4.8		4.8		dB	
Worst case operating range		2 - 125 ^a 2 - 200 ^b		2 - 75	m	С
Fiber mode-field (core) diameter		50		62.5	μm	

a. 4x-SX/50: 500MHz.km 50µm / 125µm MM fiber

b. 4x-SX/50: 2000MHz.km 50µm / 125µm MM fiber

c. Longer operating distance than the range specified here can be achieved using transmitters, receivers and/or cables meeting specification but performing better than worst-case.

> An Optical Transmitter for a 4x-SX link shall meet the parameters specified in Table 76 at TP2.

> If any high-speed electrical input signals are less than the V_{RSD} (Signal Threshold) as defined in Chapter 6: High Speed Electrical Signaling - 2.5, 5.0. & 10.0 Gb/s then the optical modulation amplitude shall not exceed 5.0 μW.

Table 76 Optical Transmitter Parameters - 4x-SX

Parameter	Minimum	Maximum	Units	Note
Туре	La	aser		
Center Wavelength	830	860	nm	
RMS spectral width		0.85	nm	
Average launched power		-2.5	dBm	а
Optical Modulation Amplitude (OMA)	0.150		mW	b
RMS mean of 20% - 80% Rise/Fall time		150	ps	С
RIN ₁₂ (OMA)		-117	dB/Hz	

a. Average launched power per fiber, max. is the lesser of the eye safety limit or Average receiver power, max.

b. Optical modulation amplitude values are peak-to-peak.

39 c. Optical rise and fall time specifications are based on unfiltered waveforms. See Section 8.5.3.2.

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An Optical Receiver for a 4x-SX link **shall** meet the parameters specified in <u>Table 77</u> at TP3.

If the average received optical power on any Lane is less than -26 dBm 3 then the corresponding high-speed electrical signaling output **shall** be 4 squelched to less than V_{RSD} (Signal Threshold) as defined in <u>Chapter 6</u>: 5 <u>High Speed Electrical Signaling - 2.5, 5.0, & 10.0 Gb/s</u>. The electrical outputs of every lane with a optical power greater than -18 dBm **shall not** be 7 squelched. 8

Table 77 Optical Receiver Parameters - 4x-SX					
Parameter	Minimum	Maximum	Units	Note	
Average received power		-1.5	dBm		
Optical modulation amplitude	0.050		mW	а	
Return loss of receiver	12		dB		
Stressed receiver sensitivity (OMA)	0.085		mW	а	
Stressed receiver ISI test	0.90		dB		
Stressed receiver DCD component of DJ (at TX)	60		ps		
Receiver electrical 3 dB upper cutoff frequency		2.8	GHz		
Receiver electrical 10 dB upper cutoff frequency		6.0	GHz		

a. Optical modulation amplitude values are peak-to-peak.

8.5.10.3 4x-LX EYE SAFETY

The 4x LX Optical Port **shall** meet the Eye safety as defined for 10GBASE-LR in **ANSI/IEEE P802.3ae-2002 10Gb/s Ethernet**.

8.5.10.4 4x-LX OPTICAL PARAMETERS

The 4x-LX Optical Port **shall** meet the Optical Parameters as defined for 10GBASE-LR in **ANSI/IEEE P802.3ae-2002 10Gb/s Ethernet**. 4x LX **shall** use the same transmit and receive optical interface and budget specifications and measurements, with the following notes and exceptions:

InfiniBand TM Architecture Release 1.2	Fiber Attachment - 2.5 Gb/s, 5.0 Gb/s, & 10 Gb/s
VOLUME 2 - PHYSICAL SPECIFICATIONS	

 The nominal signaling speed for 4x-LX shall be 10.0 GBaud <u>+</u>100ppm

8.5.11 4x-DDR-SX LINK

C8-12.2.3: All 4x-DDR-SX Optical Ports **shall** comply with the Eye Safety, Transmitter, and Receiver requirements in <u>Section 8.5.11.1</u> and <u>Section 8.5.11.2</u>.

A 4x-DDR-SX link operates in the 850nm wavelength band using multimode (MM) fiber. The optical parameters have been selected so as to allow typical 4x-DDR-SX Optical Transceivers to use an array of GaAs VCSELs and an array of photodetectors, trans-impedance pre-amplifiers and limiting post-amplifiers. Three fiber types are specified for 4x-DDR-SX:

- i) 4x-SX/50: 500MHz.km 50µm / 125µm MM fiber
- ii) 4x-SX/50: 2000MHz.km 50µm / 125µm MM fiber
- iii) 4x-SX/62: 200MHz.km 62.5µm / 125µm MM fiber

8.5.11.1 4x-DDR-SX EYE SAFETY

The optical power emitted from a 4x-DDR-SX port **shall** be limited to a maximum value for Class 1M laser safety in accordance with IEC/EN 60825-1 Amendment 2 Safety of Laser Products, part 1: Equipment classification, requirements, and user's guide and FDA/CDRH 21 CFR 1040.10

For systems that are required to meet existing IEC Class I laser safety regulations, Open Fiber Control (OFC) or other similar vendor-specific protocols **should** be implemented to meet the CDRH and IEC requirement. Any such implementation **shall** be transparent to all InfiniBand layers.

Recommendation to System Designer

Without any form of open fiber control, the power levels specified for the 4x-DDR-SX Optical Transmitter will meet the new relaxed specification for IEC Class 1M.

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8.5.11.2 4x-DDR-SX OPTICAL PARAMETERS

Table 78 gives the link budgets for 4x-DDR-SX multimode fiber optic links running at 5.0 GTransfers/second. Fiber plant specifications are described in Section 8.7.

Table 78 Link Parameters - 4x-DDR-SX

Parameter	IB-4x	-SX/50	IB-4x	-SX/62		
	Minimum	Maximum	Minimum	Maximum	Units	Note
Baud Rate		5000		5000	Mb/s	
Rate tolerance		<u>+</u> 100		<u>+</u> 100	ppm	
Optical Passive Loss		1.78 ^a 2.06 ^b		1.70	dB	
Optical System Penalty		2.5 ^c 2.3 ^d		3.2	dB	
Total link power budget	6.25		6.25		dB	
Worst case operating range		2 - 75 ^e 2 - 150 ^f		2 - 50	m	g
Fiber mode-field (core) diameter		50		62.5	μm	

a. 4x-SX/50: 500MHz.km 50µm / 125µm MM fiber

b. 4x-SX/50: 2000MHz.km 50µm / 125µm MM fiber

c. 4x-SX/50: 500MHz.km 50µm / 125µm MM fiber

d. 4x-SX/50: 2000MHz.km 50µm / 125µm MM fiber

e. 4x-SX/50: 500MHz.km 50µm / 125µm MM fiber

f. 4x-SX/50: 2000MHz.km 50µm / 125µm MM fiber

g. Longer operating distance than the range specified here can be achieved using transmitters, receivers and/or cables meeting specification but performing better than worst-case.

> An Optical Transmitter for a 4x-DDR-SX link shall meet the parameters specified in Table 79 at TP2.

Table 79 Optical Transmitter Parameters - 4x-DDR-SX

Parameter	Minimum	Maximum	Units	Note
Туре	La	ser		
Center Wavelength	830	860	nm	
RMS spectral width		0.85	nm	
Average launched power		-2.0	dBm	а
Table 79 Optical Transmitter Parameters - 4x-DDR-SX

Parameter	Minimum	Maximum	Units	Note
Optical Modulation Amplitude (OMA)	0.224		mW	b
RMS mean of 20% - 80% Rise/Fall time		75	ps	С
RIN ₁₂ (OMA)		-122	dB/Hz	

a. Average launched power per fiber, max. is the lesser of the eye safety limit or Average receiver power, max.

b. Optical modulation amplitude values are peak-to-peak.

c. Optical rise and fall time specifications are based on unfiltered waveforms. See Section 8.5.3.2

An Optical Receiver for a 4x-DDR-SX link **shall** meet the parameters specified in <u>Table 80</u> at TP3.

Table 80 Optical Receiver Parameters - 4x-DDR-SX

Parameter	Minimum	Maximum	Units	Note
Average received power	-1.5		dBm	
Optical modulation amplitude (Informative)		0.053 Informative	mW	а
Return loss of receiver	12		dB	
Stressed receiver sensitivity (OMA)	0.078		mW	b
Stressed receiver ISI test	1.50		dB	
Stressed receiver DCD component of DJ (at TX)	16.3		ps	

a. Optical modulation amplitude values are peak-to-peak.

b. Stressed Rx entries for Sensitivity and ISI differ for each fiber type. The entries shown are for 50u, 500MHzkm fiber

8.5.12 8x-SX LINKS - AT 2.5 GB/S

C8-12.2.4: All 8x SX Optical Ports **shall** meet all the optical specifications for 12x-SX in <u>Section 8.5.13</u> with the exception that 8x SX has only eight receive and transmit lanes.

8.5.13 12x-SX LINKS - AT 2.5 GB/S

C8-13: This compliance statement is obsolete and has been replaced by <u>C8-13.2.1</u>.

C8-13.2.1: All 12x-SX Optical Ports shall comply with the Eye Safety, Transmitter, and Receiver requirements in <u>Section 8.5.13</u>.

A 12x-SX link operates in the 850nm wavelength band using multimode (MM) fiber. The optical parameters have been selected so as to allow typical 12x-SX Optical Transceivers to use an array of GaAs VCSELs and an array of photodetectors, trans-impedance pre-amplifiers and limiting postamplifiers. Two fiber types are specified for 12x-SX:

- i) 12x-SX/50 link: 500MHz.km 50µm / 125µm MM fiber
- ii) 12x-SX/50 link: 2000MHz.km 50µm / 125µm MM fiber
- iii) 12x-SX/62 link: 200MHz.km 62.5µm / 125µm MM fiber

8.5.13.1 12-SX EYE SAFETY

The optical power coupled into the fiber for IB-12x-SX **shall** be limited to a maximum value with Class IIIB laser safety operation in accordance with CDRH and EN 60825-1 Amendment 2 Radiation Safety of Laser Products: Equipment Classification, Requirements and User Guide.

For systems that are required to meet existing IEC Class I laser safety regulations, Open Fiber Control (OFC) or other similar vendor-specific protocols **should** be implemented to meet the CDRH and IEC requirement. Any such implementation **shall** be transparent to all InfiniBand layers.

Recommendation to System Designer

Without any form of open fiber control, the power levels specified for the 12x-SX Optical Transmitter will meet the proposed new relaxed specification for IEC Class 1M, which is currently in the process of ratifications. However, the InfiniBand Trade Association cannot guarantee when or if the new Class 1M power level will be ratified. Vendors **should** consider this when designing InfiniBand systems.

8.5.13.2 12x-SX OPTICAL PARAMETERS

<u>Table 81</u> gives the link budgets for 12x-SX and 8x-SX multimode fiber optic links running at 2.5 GTransfers/second. Fiber plant specifications are described in <u>Section 8.7</u>.

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5	IB-12x	IB-12x-SX/50 IB-		-SX/62		
Parameter	Minimum	Maximum	Minimum	Maximum	Units	Note
Baud Rate		2500		2500	Mb/s	
Rate tolerance		<u>+</u> 100		<u>+</u> 100	ppm	
Optical Passive Loss		1.9		1.8	dB	
Optical System Penalty	2.9			3.0	dB	
Total link power budget	4.8		4.8		dB	
Worst case operating range	125 ^a 200 ^b		75	m	С	
Fiber mode-field (core) diameter		50		62.5	μm	

Table 81 Link Parameters - 12x-SX and 8x-SX

a. 12x-SX/50 link: 500MHz.km 50µm / 125µm MM fiber

b. 12x-SX/50 link: 2000MHz.km 50µm / 125µm MM fiber

c. Longer operating distance than the range specified here can be achieved using transmitters, receivers and/or cables meeting specification but performing better than worst-case.

An Optical Transmitter for a 12x-SX or 8x-SX link **shall** meet the parameters specified in <u>Table 82</u> at TP2.

If any high-speed electrical input signals are less than the V_{RSD} (Signal Threshold) as defined in <u>Chapter 6: High Speed Electrical Signaling - 2.5,</u> <u>5.0, & 10.0 Gb/s</u> then the optical modulation amplitude **shall not** exceed 5.0 μ W.

Table 82 Optical Transmitter Parameters - 12x-SX and 8x-SX

Minimum	Maximum	Units	Note
La	aser		
830	860	nm	
	0.85	nm	
	-4	dBm	а
0.150		mW	b
	150	ps	с
	-117	dB/Hz	
	Minimum La 830 0.150	Minimum Maximum Laser 860 830 860 0.85 -4 0.150 150 -117 -117	Minimum Maximum Units Laser 830 860 nm 0.85 nm -4 dBm 0.150 mW 150 ps -117 dB/Hz

a. Average launched power per fiber, max. is the lesser of the eye safety limit or Average receiver power, max.

b. Optical modulation amplitude values are peak-to-peak.

c. Optical rise and fall time specifications are based on unfiltered waveforms. See Section 8.5.3.2.

An Optical Receiver for a 12x-SX link **shall** meet the parameters specified in <u>Table 83</u> at TP3.

If the average received optical power on any Lane is less than -26 dBm then the corresponding high-speed electrical signaling output **shall** be squelched to less than V_{RSD} (Signal Threshold) as defined in <u>Chapter 6</u>: <u>High Speed Electrical Signaling - 2.5, 5.0, & 10.0 Gb/s</u>. The electrical outputs of every lane with a optical power greater than -18 dBm **shall not** be squelched.

Table 83 Optical Receiver Parameters - 12x-SX

Minimum	Maximum	Units	Note
	-1.5	dBm	
0.050		mW	а
12		dB	
0.085		mW	а
0.90		dB	
60		ps	
	2.8	GHz	
	6.0	GHz	
	Minimum 0.050 12 0.085 0.90 60	Minimum Maximum -1.5 -1.5 0.050 -1.5 12 -1.5 0.085 -0.085 0.90 -0.090 60 2.8 6.0 -0.010	Minimum Maximum Units -1.5 dBm 0.050 mW 12 dB 0.085 mW 0.90 dB 60 ps 2.8 GHz 6.0 GHz

a. Optical modulation amplitude values are peak-to-peak.

8.5.14 8x-DDR-SX AND 12x-DDR-SX LINKS

C8-13.2.2: All 8x-SX-DDR and 12x-SX-DDR Optical Ports shall comply with the Eye Safety, Transmitter, and Receiver requirements in <u>Section</u> 8.5.14

A 8x-DDR-SX and 12x-DDR-SX links operates in the 850nm wavelength band using multimode (MM) fiber. The optical parameters have been selected so as to allow typical 8x-DDR-SX and 12x-DDR-SX Optical Transceivers to use an array of GaAs VCSELs and an array of photodetectors, trans-impedance pre-amplifiers and limiting post-amplifiers. Three fiber types are specified for 8x-DDR-SX and 12x-DDR-SX:

i) 12x-SX/50 link: 500MHz.km 50µm / 125µm MM fiber

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- ii) 12x-SX/50 link: 2000MHz.km 50µm / 125µm MM fiber
- iii) 12x-SX/62 link: 200MHz.km 62.5µm / 125µm MM fiber

8.5.14.1 8X-DDR-SX AND 12X-DDR-SX EYE SAFETY

The optical power coupled into the fiber for 8x-DDR-SX and 12x-DDR-SX **shall** be limited to a maximum value with Class 1M laser safety operation in accordance with CDRH and EN 60825-1 Radiation Safety of Laser Products: Equipment Classification, Requirements and User Guide.

For systems that are required to meet existing IEC Class I laser safety regulations, Open Fiber Control (OFC) or other similar vendor-specific protocols **should** be implemented to meet the CDRH and IEC requirement. Any such implementation **shall** be transparent to all InfiniBand layers.

8.5.14.2 8x-DDR-SX AND 12x-DDR-SX OPTICAL PARAMETERS

<u>Table 84</u> gives the link budgets for 8x-DDR-SX and 12x-DDR-SX multimode fiber optic links running at 5.0 GTransfers/second. Fiber plant specifications are described in <u>Section 8.7</u>.

Descusion	IB-12x	IB-12x-SX/50		IB-12x-SX/62		
Parameter	Minimum	Maximum	Minimum	Maximum	Units	Note
Baud Rate		5000		5000	Mb/s	
Rate tolerance		<u>+</u> 100		<u>+</u> 100	ppm	
Optical Passive Loss		1.78 ^a 2.06 ^b		1.68	dB	
Optical System Penalty		2.6 ^c 2.5 ^d		3.1	dB	
Total link power budget	6.25		6.25		dB	
Worst case operating range		2-75 ^e 2-150 ^f		2-45	m	g
Fiber mode-field (core) diameter		50		62.5	μm	

Table 84 Link Parameters - 8x-DDR-SX and 12x-DDR-SX

d. 12x-SX/50 link: 2000MHz.km 50µm / 125µm MM fiber

e. 12x-SX/50 link: 500MHz.km 50µm / 125µm MM fiber

f. 12x-SX/50 link: 2000MHz.km 50µm / 125µm MM fiber

g. Longer operating distance than the range specified here can be achieved using transmitters, receivers and/or cables meeting specification but performing better than worst-case.

An Optical Transmitter for a 8x-DDR-SX and 12x-DDR-SX link **shall** meet the parameters specified in <u>Table 85</u> at TP2.

Table 85 Optical Transmitter Parameters - 8x-DDR-SX and 12x-DDR-SX

Parameter	Minimum	Maximum	Units	Note
Туре	La	ser		
Center Wavelength	830	860	nm	
RMS spectral width		0.85	nm	
Average launched power		-2.0	dBm	а
Optical modulation amplitude	0.224		mW	b
RMS mean of 20% - 80% Rise/Fall time		75	ps	С
RIN ₁₂ (OMA)		-122	dB/Hz	

a. Average launched power per fiber, max. is the lesser of the eye safety limit or Average receiver power, max.

b. Optical modulation amplitude values are peak-to-peak.

c. Optical rise and fall time specifications are based on unfiltered waveforms. See Section 8.5.3.2.

An Optical Receiver for a 12x-DDR-SX link **shall** meet the parameters specified in <u>Table 83</u> at TP3.

Parameter	Minimum	Maximum	Units	Note
Average received power	-1.5		dBm	
Optical Modulation Amplitude (OMA) (Informative)		0.053 Informative	mW	а
Return loss of receiver	12		dB	
Stressed receiver sensitivity (OMA)	0.078		mW	a ,b
Stressed receiver ISI test	1.50		dB	2
Stressed receiver DCD component of DJ (at TX)	16.3		ps	

a. Optical modulation amplitude values are peak-to-peak.

b. Stressed Rx entries for Sensitivity and ISI differ for each fiber type. The entries shown are for 50u, 500MHzkm fiber

8.5.15 1x QDR LINKS

C8-13.2.3: All 1x-QDR-SX Optical Ports **shall** comply with the Eye Safety, Transmitter, and Receiver requirements in <u>Section 8.5.15.1</u> and <u>Section 8.5.15.2</u>

C8-13.2.4: All 1x-QDR-LX Optical Ports **shall** comply with the Eye Safety, Transmitter, and Receiver requirements in <u>Section 8.5.15.1</u> and <u>Section 8.5.15.3</u>

A 1x-QDR-SX link operates in the 850nm wavelength band using multimode (MM) fiber. The optical parameters have been selected so as to allow typical 1x-SX Optical Transceivers to use a GaAs Vertical Cavity Surface Emitting Laser (VCSEL) and a photodetector, trans-impedance pre-amplifier and limiting post-amplifier. Three fiber types are specified for 1x-QDR-SX:

- i) 1x-SX/50 link: 500MHz.km 50µm / 125µm MM fiber
- ii) 1x-SX/50 link: 2000MHz.km 50µm / 125µm MM fiber
- iii) 1x-SX/62 link: 200MHz.km 62.5µm / 125µm MM fiber

A 1x-QDR-LX link operates in the 1300nm wavelength band using singlemode (SM) fiber. The optical parameters have been selected to allow a typical 1x-LX Optical Transceiver to use an uncooled InP-based Fabry-Perot (FP) laser, Distributed Feedback (DFB) laser or VCSEL laser, and an InGaAs photodetector, trans-impedance pre-amplifier and limiting post-amplifier. A trade-off curve is provided in <u>Figure 65</u> between Center Wavelength and RMS Spectral Width to allow designers to select appropriate laser technology while still ensuring link operation. Only one fiber type is specified for 1x-LX: single-mode non-dispersion shifted.

8.5.15.1 1x QDR EYE SAFETY

C8-13.2.5: The optical power coupled into the fiber for 1x-QDR-SX and 1x-QDR-LX **shall** be limited to a maximum value with Class I laser safety operation in accordance with CDRH and IEC 60825-1 Radiation Safety of Laser Products: Equipment Classification, Requirements and User Guide.

8.5.15.2 1x-QDR-SX OPTICAL PARAMETERS

The 1x QDR SX Optical Port shall meet the Optical Parameters as defined for 10GBASE-SR in **ANSI/IEEE P802.3ae-2002 10Gb/s Ethernet**. 1x QDR SX **shall** use the same transmit and receive optical interface and budget specifications and measurements, with the following notes and exceptions:

 The nominal signaling speed for 1x-QDR-SX shall be 10.0 GBaud <u>+</u>100ppm

8.5.15.3 1x-QDR-LX OPTICAL PARAMETERS

The 1x LX QDR Optical Port shall meet the Optical Parameters as defined for 10GBASE-LR in **ANSI/IEEE P802.3ae-2002 10Gb/s Ethernet**. 1x LX QDR **shall** use the same transmit and receive optical interface and budget specifications and measurements, with the following notes and exceptions:

 The nominal signaling speed for 1x-QDR-LX shall be 10.0 GBaud <u>+</u>100ppm

8.6 OPTICAL RECEPTACLE AND CONNECTOR

The primary function of the optical fiber connector specification is to define mechanical alignment of the optical fibers to the optical port of an Optical Transceiver.

The objective of this section is to specify the optical interface sufficiently to ensure the following:

- a) Intermateability
- b) Mechanical/Optical Performance
- c) Maximum Supplier Flexibility

In this section, only the dimensions necessary to specify the transmitterreceiver center-center distance of the 12x-SX connector are provided. All other dimensions are included by reference to other standards. **C8-14:** All Optical Transceivers **shall** present the Optical Receptacle specified in <u>Optical Receptacle and Connector (Section 8.6)</u> through the system bulkhead. Typically, this bulkhead will be a connector housing.

Optical Receptacles, Optical Connectors, and Fibre Optic Adapters **shall** be as specified in this section.

The InfiniBand connector for 1x, 1x DDR and 1x QDR links **shall** be a duplex LC connector, for 4x SX and 4x SX DDR links **shall** be an MPO connector, for 4x LX links **shall** be a dual-SC connector and for 12x, 8x SX DDR and 12x SX DDR links **shall** be a dual-MPO connector.

8.6.1 1x CONNECTOR - LC

The connectors, adapters and receptacles described here **shall** be fully duplex, creating fully bi-directional optical connection with one mating action. Figure 78 and Figure 79 show outline drawings of the Duplex LC Optical Connector and Duplex LC Fiber Optic Adapter respectively.

The 1x Optical Connector defined by this specification **shall** conform to ANSI/TIA/EIA 604-10 (FOCIS 10), Fiber Optic Connector Intermateability Standard, Type "LC".

Cable supports Crimp sleeves
Dual yoke
Connectors FOCIS 10 designation d=2 r=2
Figure 78 Dual LC Plug

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LC Dual Adapter FOCIS 10 designation n=2 m=2 (shown)

Figure 79 Dual LC Fiber Optic Adapter

8.6.1.1 1x FIBER OPTIC CONNECTOR

C8-15: All 1x Optical Cable Connectors shall comply with connector specifications of <u>Section 8.6.1.1</u>.

The InfiniBand connector for 1x links **shall** be a duplex LC connector.

The 1x Optical Connector on each end of the Fiber Optic Cable **shall** conform to:

- i) ANSI/TIA/EIA 604-10 (FOCIS 10), Fiber Optic Connector Intermateability Standard, Type "LC", and 20
- ii) Fibre Channel Physical Interface standard (FC-PI), revision 21 8.0 22

The implementation of connectors or adapters compliant with the FOCIS 10 standard **shall not** preclude the intermateability of connectors, adapters or receptacles compliant with the FOCIS 10A standard.

8.6.1.2 1x FIBER OPTIC RECEPTACLE

C8-16: All 1x Optical Port Receptacles shall comply with receptacle and fiber orientation specifications of <u>Section 8.6.1.2</u> and <u>Section 8.6.1.3</u>.

The 1x (SX & LX) Optical Transceiver Port **shall** be a Type "LC" receptacle as defined by ANSI/TIA/EIA 604-10 (FOCIS 10), Fiber Optic Connector Intermateability Standard.

It **may** contain resilient sleeves to optically align the connector plug ferrules. The positioning of the ferrule endfaces to optimize optical coupling can be accomplished in a variety of ways not described here.

The implementation of connectors, adapters or receptacles compliant with the FOCIS 10 standard **shall not** preclude the intermateability of connectors, adapters or receptacles compliant with the FOCIS 10A standard.

8.6.1.3 1x FIBER OPTIC RECEPTACLE ORIENTATION	
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1x-SX and 1x-LX FIber Optic Transceivers **shall** follow the Transmit/Receive convention detailed in Figure 80. If the Optical Connector is orientated such that the keying features on the LC housings are at the top, then looking into the Fiber Optic Receptacle the fiber on the left **shall** be used for optical transmit and the fiber on the right **shall** be used for optical receive.



Figure 80 1x-SX and 1x-LX Optical Receptacle orientation looking into the Optical Transceiver

8.6.1.4 1x COLOR

C8-17: The 1x-SX multimode Optical Connector, Adapter and Receptacle, or a visible portion of these, **shall** be beige in color.

C8-18: The 1x-LX singlemode Optical Connector, Adapter and Receptacle, or a visible portion of these, **shall** be blue in color.

8.6.2 4x-SX CONNECTOR - SINGLE MPO

The connectors, adapters and receptacles described here **shall** be fully duplex, creating fully bi-directional optical connection with one mating action.

8.6.2.1 4x-SX FIBER OPTICAL CONNECTOR

C8-19: All 4x SX Optical Cable Connectors shall comply with fiber optical connector specifications of <u>Section 8.6.2.1</u>.

The 4x-SX Optical Connector on each end of the Fiber Optic Cable **shall** consist of a female MPO plug. The female MPO plug **shall** conform to IEC 1754-7-4, Push/Pull MPO Female Plug Connector Interface, and **shall** contain a female MT ferrule.

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A female MT ferrule is similar to a male MT ferrule, except that the female ferrule does not have alignment pins. Instead, alignment holes are provided, which accept the alignment pins of the corresponding male MT ferrule. In this manner, precision alignment is achieved between the ferrule in an Optical Receptacle and the ferrule in an Optical Connector.

Figure 81 shows an outline drawing of a typical MPO connector with pushpull coupling mechanism. The MPO housing surrounds a rectangular male MT ferrule. The male MT ferrule has positions for 12 fibers. The male MT ferrule is typically 6.4 mm by 2.5 mm and contains two precision alignment pins of 0.7 mm diameter.

8.6.2.2 4x-SX FIBER OPTICAL RECEPTACLE

C8-20: All 4x SX Optical Port Receptacles shall comply with receptacle and fiber optical orientation specifications of <u>Section 8.6.2.2</u> and <u>Section 8.6.2.3</u>

The 4x-SX Optical Transceiver Port **shall** have a 4x-SX Optical Receptacle which **shall** be a male MPO receptacle. The male MPO receptacle **shall** have two fixed pins conforming to IEC 1754-7-5, and **shall** conform to IEC 1754-7-3, Push/Pull MPO Adapter Interface standard.

Note: In the U.S.A., the MPO connector is also known as the MTP connector.

8.6.2.3 4X-SX FIBER OPTIC RECEPTACLE ORIENTATION

27 4x-SX Optical Transceivers shall follow the Transmit/Receive convention detailed in Figure 82. If the Optical Connector is orientated such that the 28 keying feature on the MPO housing is at the top, then looking into the 29 Fiber Optic Receptacle fibers are numbered left-to-right as 0-through-11. 30 The 4 fiber positions on the left (fibers 0, 1, 2, 3) shall be used for optical 31 transmit and the 4 fiber positions on the right (fibers 8, 9, 10, 11) shall be 32 used for optical receive. Fibers 0, 1, 2, 3 shall carry transmit Lanes 0, 1, 33 2, 3 respectively. Fibers 8, 9, 10, 11 shall carry receive Lanes 3, 2, 1, 0 respectively. 34

The central four fibers (fibers 4, 5, 6, 7) **may** be physically present. If one or more of the central four fibers is present, then it **shall not** be used to carry IB signals.

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The connectors, adapters and receptacles described here **shall** be fully duplex, creating fully bi-directional optical connection with one mating action.

8.6.3.1 4x LX FIBER OPTIC CONNECTOR

C8-20.1.1: All 1x Optical Cable Connectors shall comply with connector specifications of <u>Section 8.6.3.1</u>.

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Receive Lane Number

 Fiber number
 0 1 2 3 4 5 6 7 8 91011

 Used (o) or not (x)
 0 0 0 0 x x x x 0 0 0 0

Figure 82 4x-SX Optical Receptacle orientation looking into the Transceiver

The InfiniBand connector for 4x LX links **shall** be a duplex SC connector.

The 4x LX Optical Connector on each end of the Fiber Optic Cable **shall** conform to the requirements of IEC 61754-4.

Only the Floating Duplex style Connector Plug **shall** be used. Rigid SC Duplex connector **shall not** be used.

8.6.3.2 4x LX FIBER OPTIC RECEPTACLE

C8-20.1.2: All 1x Optical Port Receptacles shall comply with receptacle and fiber orientation specifications of <u>Section 8.6.3.2</u> and <u>Section 8.6.3.3</u>.

The 4x LX Optical Transceiver Port **shall** be a Type "SC" receptacle as defined by IEC 61754-4-5.

8.6.3.3 4x LX FIBER OPTIC RECEPTACLE ORIENTATION

4x LX Fiber Optic Transceivers shall follow the Transmit/Receive convention detailed in Figure 83. If the Optical Connector is orientated such that3031313231333134323532363237323832393330323132323333333434343435343634

8.6.4 8x-SX OPTICAL RECEPTACLE AND CONNECTOR

C8-20.2.1: All 8x SX Optical Cable Connectors and 8x Optical Port Receptacles shall comply with the 12x-SX connector and receptacle specifications in <u>Section 8.6.4</u> and <u>Section 8.6.5</u> with the exception of the following exception for Fiber Optic Receptacle Orientation:



Figure 83 4x-LX Optical Receptacle orientation

8x-SX Optical Transceivers **shall** follow the transmit/receive convention detailed in Figure 84. If the Optical Connector is orientated such that the keying features on the MPO housings are at the top, then looking into the Optical Receptacle the fibers are numbered left-to-right as 0-through-11 for the left-hand section and 0-through-11 for the right hand section. The 8 fiber positions on the left **shall** be used for optical transmit and the 8 fiber positions on the right **shall** be used for optical receive. On the left, fibers 0, 1, 2, 3, 4, 5, 6, 7 **shall** carry transmit Lanes 0, 1, 2, 3, 4, 5, 6, 7 respectively. On the right, fibers 4, 5, 6, 7, 8, 9, 10, 11 **shall** carry receive Lanes 7, 6, 5, 4, 3, 2, 1, 0 respectively. On the left fibers 8, 9, 10, 11 **may** be present but **shall not** be used to carry IB signals. On the right fibers 0, 1, 2, 3 **may** be present but **shall not** be used to carry IB signals.

InfiniBand TM Architecture Rel Volume 2 - Physical Specific	October, 2004 FINAL		
		Receiver on Right	1 2 3 4 5 6 7
Transmit Lane number Fiber number Used (o) or not (x)	0 1 2 3 4 5 6 7 8 91011 0 1 2 3 4 5 6 7 8 91011 0 0 0 0 0 0 0 0 0 x x x x	1110 9 8 7 6 5 4 3 2 1 0' 0 1 2 3 4 5 6 7 8 91011 x x x x x 0 0 0 0 0 0 0	8 9 Receive Lane Number 1 Fiber number Used (o) or not (x)
Figure 84	4 8x-SX Optical Receptacle	e orientation looking into th	1 1 1 1 1 1
8.6.5 12x-SX CONNEC	TOR - DUAL MPO		1
	The connectors, addupter, creating full	apters and receptacles descr y bi-directional optical conne	ibed here shall be fully 1 ction. 2
8.6.5.1 12x-SX FIBER O	PTIC CONNECTOR		2
	C8-21: All 12x-SX specifications of <u>Se</u>	Optical Cable Connectors sha <u>ction 8.6.5.1</u> .	all comply with connector 2 2 2
	The 12x-SX Optical consist of a double IEC 1754-7-4, Push shall contain a fema	Connector on each end of the female MPO plug. Each fema I/Pull MPO Female Plug Con ale MT ferrule.	e Fiber Optic Cable shall 2 ale plug shall conform to 2 nector Interface, and 2 2
8.6.5.2 12x-SX FIBER O	PTIC RECEPTACLE		3
	C8-22: This complian <u>C8-22.2.1:</u>	ance statement is obsolete ar	nd has been replaced by 3 3
	C8-22.2.1: All 12x-Stacle and fiber optic Section 8.6.2.3	SX Optical Port Receptacles a al orientation specifications of	shall comply with recep- of <u>Section 8.6.5.2</u> and 3
	The 12x-SX Optical tacle which shall co MPO receptacle sh fixed pins conformir 3, Push/Pull MPO A	Transceiver Port shall have onsist of a double male MPO all be as described in <u>Section</u> of to IEC 1754-7-5, and shal adapter Interface standard.	a 12x-SX Optical Recep- receptacle. Each male <u>n 8.6.2</u> , shall have two I conform to IEC 1754-7- 4

A 12x Optical Transceiver **may** consist of physically separate Transmit and Receive Modules or a single physical Transceiver.

If a 12x solution is based on separate transmit and receive modules, then these modules **shall** support a centerline to centerline receptacle spacing of 20.0 mm +/-0.5 mm as defined in Figure 85.

If a 12x solution is based on a single transceiver module, then these modules **shall** support a centerline to centerline receptacle spacing of 16.0 mm \pm 0.1mm as defined in Figure 85.





Implementation Note

To simplify cable management, in typical installations a duplex Fiber Optic Cable will be mated to a 12x-SX Optical Transceiver in a single mating action. This reduces the probability of mis-configuration. A plastic clip would serve to join two individual MPO housings together to form a double-MPO connector. Alternatively, a common housing could be moulded to house two sets of MPO actuation mechanisms plus two MT ferrules that float independently. In all cases, the two MT ferrules would float independently of each other to some extent.

The Optical Transceiver within the IB module could be constructed either as one transceiver component. Alternatively it could be constructed as separate Optical Transmitter and Optical Receiver components mounted to the board independently, but mutually aligned to within the total travel of the two MT ferrules.

8.6.5.3 12X-SX FIBER OPTIC RECEPTACLE ORIENTATION

12x-SX Optical Transceivers **shall** follow the transmit/receive convention detailed in <u>Figure 86</u>. If the Optical Connector is orientated such that the

keying features on the MPO housings are at the top, then looking into the Optical Receptacle the fibers are numbered left-to-right as 0-through-11 for the left-hand section and 0-through-11 for the right hand section. The 12 fiber positions on the left **shall** be used for optical transmit and the 12 fiber positions on the right shall be used for optical receive. On the left, fibers 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 shall carry transmit Lanes 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 respectively. On the right, fibers 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 shall carry receive Lanes 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0 respectively.



Fiber Optic Cables for links in the -SX class shall use either 50/125 μ m optical fiber or 62.5/125 µm multimode optical fiber compliant respectively with the "MMF 50/125 um" or "MMF 62.5/125 µm" specification in this section.

	Fiber Optic Cables for links in the -LX class shall use non-dispersion- shifted single mode fiber compliant with the "SMF" specification in this section.	1 2
	SMF shall conform to TIA/EIA-492CAAA-98 "Dispersion-Unshifted Single-Mode Optical Fibers".	3 4 5
	MMF 500 MHz.km 50/125 μ m shall conform to TIA/EIA-492AAAB-98 "Detail Specification for 50- μ m Core Diameter/125- μ m Cladding Diameter Class Ia Graded-Index Multimode Optical Fibers" or IEC 60793-2 Type A1a.	6 7 8 9 10
	MMF 2000 MHz.km 50/125 μm shall conform to TIA/EIA-492AAAC. TIA/EIA-492AAAC is presently in ballot.	11 12
	MMF 62.5/125 μ m shall conform to TIA/EIA-492AAAA-A-97 "Detail Specification for 62.5- μ m Core Diameter/125- μ m Cladding Diameter Class Ia Graded-Index Multimode Optical Fibers" or IEC 60793-2 Type A1b.	13 14 15 16 17 18
	Recommendation to Optical System Designer	19 20
	For new -SX installations, MMF 50/125 μ m fiber should be used because of the increased range of 1x-SX/50 links compared to 1x-SX/62 links.	21 22 23
	4x-SX, 8x-SX and 12x-SX Fiber Optic Cables may use ribbonized fibers.	24 25
	SMF, MMF 50/125 μ m and MMF 62.5/125 μ m fibers shall also conform to the respective columns of <u>Table 87</u> .	26 27 28
8.7.2 MODAL BANDWIDTH		29 30
	The Modal Bandwidth for the 500 MHz.km and 200 MHz.km cables with Overfilled Launch specified in <u>Table 87</u> is the worst case modal band- width, measured according to the methods of TIA2.2.1 working specifica- tion TIA/EIA/455-204-FOTP204 Measurement method for Multimode Fiber Bandwidth. The 2000MHz.km cable is measured using TIA/EIA- 492AAAC. Worst case modal bandwidth is defined as the lowest band- width that can occur in a fiber under reasonable launch conditions.	31 32 33 34 35 36 37
	In practice, worst case modal bandwidth is used to account for differences in multimode fiber bandwidth that can occur under restricted launch con- ditions relative to bandwidth observed using an overfilled launch condi- tion. The Optical System Penalty limits presented in <u>Section 8.5.8</u> , <u>Section 8.5.10</u> and <u>Section 8.5.13</u> represent conservative calculations	38 39 40 41 42

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based on an overfilled launch model. In practice, better link performance is typically expected.

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	SMF (9 μm)	MMF 50/125 μm	MMF 62.5/125 μm	Units
Nominal Fiber Specification Wavelength	1310	850	850	nm
Fiber Cable Attenuation (Max)	0.5	3.5	3.5	dB/km
Modal Bandwidth with Overfilled Launch (Min)	not applicable	500 ^a and 2000 ^b	200	MHz.km
Zero Dispersion Wavelength λ_0	$1300 \le \lambda_0 \le 1320$	$1295 \le \lambda_0 \le 1320$	$1320 \le \lambda_0 \le 1365$	nm
		0.11 for	0.11 for	
				ps/nm² . kı
		1500 3 M ₀ 3 1520 and	1520 3 K ₀ 3 1540 and	
Zero Dispersion Slope So (Max)	0.093			
		$001(\lambda_0 - 1190)$ for $95 \le \lambda_0 \le 1300$	$001(1458 - \lambda_0)$ for $48 \le \lambda_0 \le 1365$	
a. Overfilled launch bandwidth per l b. Effective modal bandwidth for fib	IEC 60793-1-41 or TIA er meeting TIA /EIA-49 BER OPTIC CABLE	/EIA 455-204. 92AAAC		
HCALL ASSIVE E000 OF TH				

Optical Passive Loss **shall** be not exceed than the values specified in <u>Table 63</u>, <u>Table 66</u>, <u>Table 75</u> and <u>Table 81</u> for 1x-SX, 1x-LX, 4x-SX and 12x-SX links respectively. Optical Passive Loss **shall not** exceed the values specified in <u>Table 69</u>, <u>Table 72</u>, <u>Table 78</u>, <u>Table 84</u>, and <u>Table 84</u> for 1x-DDR SX, 1x-DDR LX, 4x-DDR SX, 8x-DDR-SX and 12x-DDR-SX links respectively. The loss of the fiber plant **shall** be verified by the methods of OFSTP-14A. The Optical Passive Loss of a Fiber Optic Cable is the sum of attenuation losses due to the fiber, Fiber Optic Adapters and splices.

Connection Insertion Loss for 4x-LX **shall not** exceed the values specified for 10GBASE-L optical cables in **ANSI/IEEE P802.3ae-2002 10Gb/s Ethernet**. The loss of the fiber plant **shall** be verified by the methods defined in **ANSI/IEEE P802.3ae-2002 10Gb/s Ethernet**. The Connection Insertion Loss for 4x-LX of a Fiber Optic Cable is the sum of attenuation losses due to the fiber, Fiber Optic Adapters and splices.

A Fiber Optic Cable **may** contain one or more Fiber Optic Adapters and/or splices, provided that the total Optical Passive Loss conforms to the optical budget of this specification. In calculating worst case operating range values for <u>Table 63</u>, <u>Table 66</u>, <u>Table 69</u>, <u>Table 72</u>, <u>Table 75</u>, <u>Table 78</u> and <u>Table 81</u>, a total loss budget of 1.5dB was assigned to Fiber Optic Adapters and splices. For 4x-LX, 10G Ethernet assumed a budget of 2.0dB for Fiber Optic Adapters and splices.

8.7.4 FIBER OPTIC ADAPTERS AND SPLICES

8.7.4.1 1x (SX & LX) FIBER OPTIC ADAPTERS AND SPLICES

C8-25: All 1x (SX & LX) Optical Cable adaptors and splices **shall** comply with <u>Section 8.7.4.1</u>

If the 1x Fiber Optic Cable consists of more than one Fiber Optic Segment, then the Fiber Optic Adapter used to join the Fiber Optic Segments **shall** conform to ANSI/TIA/EIA 604-10 (FOCIS 10), Fiber Optic Connector Intermateability Standard, Type "LC".

Fiber Optic Adapters and splices for 1x-SX (multimode) links **shall** have a return loss of 20dB minimum as measured by the methods of FOTP-107 or equivalent. Fiber Optic Adapters and splices for 1x-LX (single-mode) links **shall** have a return loss of 26dB minimum as measured by the methods of FOTP-107 or equivalent.

8.7.4.2 4x-SX FIBER OPTIC ADAPTERS AND SPLICES

If the 4x -SX Fiber Optic Cable consists of more than one Fiber Optic Segment, then Optical Adapters are used to join the Fiber Optic Segments. These Optical Adapters are not detailed in this specification. **C8-26:** Fiber Optic Adapters and splices for 4x-SX links **shall** have a return loss of 20dB minimum as measured by the methods of FOTP-107 or equivalent.

8.7.4.3 4X-LX FIBER OPTIC ADAPTERS AND SPLICES

If the 4x -LX Fiber Optic Cable consists of more than one Fiber Optic Segment, then Optical Adapters are used to join the Fiber Optic Segments. These Optical Adapters are not detailed in this specification.

C8-26.1.1: Fiber Optic Adapters and splices for 4x-LX links **shall** have a return loss of 26dB minimum as measured by the methods of FOTP-107 or equivalent.

8.7.4.4 12x-SX FIBER OPTIC ADAPTERS AND SPLICES

If the 12x -SX Fiber Optic Cable consists of more than one Fiber Optic Segment, then Optical Adapters are used to join the Fiber Optic Segments. These Optical Adapters are not detailed in this specification.

C8-27: Fiber Optic Adapters and splices for 12-SX links **shall** have a return loss of 20dB minimum as measured by the methods of FOTP-107 or equivalent.

8.8 SIGNAL CONDITIONER IN OPTICAL TRANSCEIVER

C8-28: All Optical Ports shall comply with the Signal Conditioner requirements in <u>Section 8.8</u>

C8-28.2.1: All 8x SX Signal conditioners **shall** meet all the signal conditioner specifications for 12x-SX in <u>Section 8.8</u> with the exception that 8x SX has only eight receive and transmit lanes.

8.8.1 MOTIVATION FOR SIGNAL CONDITIONER

At this time, optical functionality is relatively expensive compared to electronic functionality. The overall system cost is generally minimized by using optical components (lasers, Fiber Optic Cables and photoreceivers) that are as low performance as can be tolerated, while including relatively sophisticated signal conditioning and control functionality in the electrical domain in the Optical Transmitter and Optical Receiver. Hence, optical links in general, including those specified for InfiniBand, are generally designed to operate at higher jitter than the electrical interconnects found on printed circuit boards

The optical jitter specification of <u>Section 8.5.5</u> is relaxed from the jitter specification for high-speed electrical signaling specified in <u>Chapter 6:</u> <u>High Speed Electrical Signaling - 2.5, 5.0, & 10.0 Gb/s</u>. However, the electrical inputs (Optical Transmitter side) and electrical outputs (Optical Receiver side) of an Optical Transceiver **shall** meet the high-speed signaling specification of <u>Chapter 6: High Speed Electrical Signaling - 2.5, 5.0, & 10.0 Gb/s</u>.

These high speed electrical signaling jitter limits should be compared to the optical jitter specification of <u>Table 58</u> for the different links widths and distance classes.

If an Optical Transceiver does not perform signal conditioning and an IB Electrical Transceiver driver output is connected directly through a short board trace to the intermediate electrical interface TP1 in an Optical Transceiver, then the recommended input jitter specification will be exceeded at TP1. The use of appropriate pre-emphasis can reduce deterministic jitter (DJ), making it more likely that the system will meet the mandatory jitter compliance at TP2 and TP33.

There is a related problem on the Optical Receiver side, assuming that the jitter at the intermediate electrical interface TP4 meets the recommended typical value. The typical TP4 jitter exceeds the specified input jitter tolerance of an IB Electrical Transceiver. Hence the system may not work correctly.

8.8.2 SIGNAL CONDITIONER IMPLEMENTATION

This section describes possible implementations of the Optical Transceiver to include the signal conditioning functionality.

Figure 87, Figure 88, Figure 89, Figure 90 and Figure 91 show typical IB Optical Transceiver implementations for 1x, 1x-DDR-SX, 1x-QDR-SX, 4x-SX, 4x-DDR-SX, 4x-LX, 8x-DDR-SX, 12x-SX, and 12x-DDR-SX respectively. In each case an optional Signal Conditioner is shown. This Signal Conditioner **shall** be present in an Optical Transceiver if the optoelectronic components do not directly provide IB-compliant high-speed electrical signals.

The function of the Signal Conditioner is to convert between IB-compliant high-speed electrical signaling and the intermediate electrical interface of the optoelectronic components. The Signal Conditioner **should** be implemented as a repeater, IB-compliant Retiming Repeater, or an adaptive equalizer.

Implementation Note

The system designer may choose to integrate the Signal Conditioner with the optoelectronic components, or may choose to install it separately on the Board.

Retiming functionality generally dissipates considerable power. For thermal considerations it may be advantageous to physically separate the signal conditioner from the optoelectronic components. This is especially true for 4x-SX and 12-SX links. In this case the intermediate electrical interface requires careful design to ensure signal integrity.

Implementation Note

In some implementations it may be expedient for an Optical Transceiver not to present an IB-compliant electrical interface. For instance, the Signal Conditioner functionality could be collapsed within the SerDes block of a Switch chip to reduce system power and cost and to improve functional density. In this case the "Optical Transceiver" no longer presents an IB-compliant high-speed electrical signaling interface. Nonetheless the TP2 and TP3 optical specifications can still be met. Hence the overall IB Module and the optical ports may still be able to claim IB-compliance, since the non-compliant electrical interface is hidden within the IB Module.

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		Optica	al Transc	eiver		Opt	ical Tra	ansceiver		
B-compliant high-speed electrical out- outs		ditioner	Ontoelectronics				Optoelectronics	ioner	*** ** ** ** ** **	IB-compliant high-speed electrical in- puts
B-compliant high-speed electrical in- outs	±++ ±++ ±++ ±++ ±++ ±++ ±++ ±++ ±++ ±++	Signal Con	Ontoelectronics		TP2		Optoelectronics	Signal Condit	*****	IB-compliant high-speed electrical out- puts

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Figure 90 Recommended 8x-SX and 8x-DDR-SX Optical Link Implementation

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8.9 AUX POWER		1
	C8-29: All Optical Ports shall comply with Aux power behavior in <u>Section</u> . <u>8.9</u>	2 3
	C8-29.2.1: All 8x-SX Optical Ports shall meet all the Aux power specifications for 12x-SX in <u>Section 8.9</u> with the exception that 8x SX has only eight receive and transmit lanes.	4 5 6 7
8.9.1 BEHAVIOR IN AUX POWE	r Mode	7 8
	To facilitate compliance with the overall Auxiliary power budget, an Optical Transceiver should not draw more than 150mW in Aux power mode. This limit depends on how much other functionality the IB Module is required to provide in Aux power mode. More than 150mW of Aux power may be available to an Optical Transceiver in certain implementations.	9 10 11 12 13
	The high-speed electrical outputs of an Optical Receiver operating under Aux power shall be squelched to less than V_{RSD} (Signal Threshold) as defined in <u>Chapter 6: High Speed Electrical Signaling - 2.5, 5.0, & 10.0</u> <u>Gb/s</u> .	14 15 16 17
8.9.2 BEACONING AND WAKE-	UP	18
	An Optical Receiver operating only under Aux power shall detect the presence of a beaconing sequence (refer to the appropriate receiver specifications in <u>Section 8.5</u> for the minimum valid optical levels) on the Fiber Optic Cable and trigger the appropriate response. See <u>Chapter 14:</u> <u>OS Power Management</u> and <u>Chapter 5: Link/Phy Interface</u> .	20 21 22 23 24
8.10 OPTICAL PLUGGABLE DE	VICES	25
8.10.1 1X OPTICAL PLUGGABL	E DEVICES	26
	C8-29.1.1: All 1x SX and 1x LX Optical Pluggable Devices shall comply with <u>Section 8.10.1</u>	27 28 29
	Any 1x Optical Pluggable device shall comply with electrical and mechan- ical 1x pluggable requirements in <u>Chapter 6: High Speed Electrical Sig- naling - 2.5, 5.0, & 10.0 Gb/s</u> and <u>Chapter 7: Copper Cable</u> , and the respective 1x optical distance classifications (SX or LX) in <u>Section 8.4.2</u> , <u>Section 8.5</u> , <u>Section 8.6.1</u> , <u>Section 8.7</u> , and <u>Section 8.9</u>	30 31 32 33 34 35 36 37 38 39
		40 41

CHAPTER 9: MECHANICAL SPECIFICATION

9.1 MECHANICAL OVERVIEW

This section describes form factors, chassis slot details, and environmental considerations necessary to implement InfiniBand (IB) systems and board modules.

This specification provides for a 3U chassis implementation with modules oriented vertically as shown in Figure 92, as well as a 6U chassis, and double width modules for both a 3U and 6U chassis. Chassis designs which orient the modules horizontally are also supported.



Figure 92 Standard Module, 3U Chassis Slots

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An InfiniBand mechanical system consists of InfiniBand Modules which are inserted into InfiniBand Slots, where a slot is defined to be a chassis 2 location capable of accepting a single width module. To be explicit, there 3 is no definition for a "double width slot". Wide modules, by definition, occupy two adjacent regular width slots. This specification does not define a 4 particular chassis or backplane design, but it does define all relevant di-5 mensions and interfaces for a single slot, as well as the spacing between 6 adjacent slots. The designer can step-and-repeat this slot definition as re-7 quired to build any size system. 8

9.1.1 DIMENSIONS AND TOLERANCES

C9-1: All dimensions included in this chapter are in millimeters and **shall** have a tolerance of +/- 0.25 mm unless otherwise specified.

Note to Designers

Some assembly tolerances in Figure 97 on page 366, Figure 101 on page 370, Figure 105 on page 374, or Figure 109 on page 378 may require assembly fixturing. Specific examples include dimensions between paddle guard and ejector surfaces.

9.1.2 MODULE DESCRIPTION

Most of the mechanical definition for InfiniBand is centered around the module. The module, shown in <u>Figure 93 on page 358</u>, consists of the following parts:

- a) The module carrier a basic metal structure which provides:
 - A metal plate which aligns and supports the circuit board(s) and provides EMI suppression between adjacent boards
 - Metal guides which mate with the surfaces of the slot for alignment, guidance, thermal management, and additional EMI suppression
 - A connector housing which provides for external connector mounting, four sided EMI sealing, ESD protection, and thermal management
- b) The module ejector(s) & latch(es) a handle and latch which provide:
 - Controlled insertion and ejection of the module for hot add/remove
 35 36 36 37
 - Retention of the module during operation or shipping
- c) The module cover easily removable cover to protect the board 39
 - Provides ESD protection for the board and components
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 - Prevents damage during module handling

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	Protects the user from high temperature	ure components
	 May optionally provide air dams / defl thermal characteristics of the module 	ectors to improve the
	Provides area for additional transvers	e airflow
	d) The board(s) which implement the modul	e's functionality
		6
		7
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	e) An optional area in the module guide are airflow in a predominantly transverse dir	ection.
	Note to Chassis Designers	

The right most slot in a chassis must provide the EMI gasket for the right side of the last module. Thereafter, the modules seal against one another or against the left wall of the chassis.

9.1.3.1 SLOT DESIGNATIONS

Viewed from the external surface of the carrier connector housing, slot numbering convention is from left to right or bottom to top depending upon the orientation of InfiniBand Modules. System designers should label chassis slots in a manner identical to the slot designation reported through the system management structure to facilitate module hot add/remove.

This release of the specification supports more than one port per slot connector. This highlights the need to provide the user a consistent means to identify chassis and modules that support greater that one port per slot connector. The following table, <u>Table 88</u>, outlines this naming convention for chassis slot labeling.

Table 88 Chassis Slot Configurations and Labeling

Label ^a	Descriptions	
CxP0	Primary slot connector with no ports (Power and or Management only)	
CxP1	Primary slot connector with port 1 populated	
CxP2	Primary slot connector with ports 1 and 2 populated	
CxP3	Primary slot connector with ports 1, 2, and 3	
OxP0	Optional slot connector with no ports (Power and or Management only)	
OxP1	Optional slot connector with port 1 populated	
OxP2	Optional slot connector with ports 1 and 2 populated	
OxP3	Optional slot connector with ports 1, 2 and 3 populated	
a. C = Prin position inf <u>backplane</u> Table 101	hary Slot Connector, $O = Optional Slot Connector, x = Slot Number. Portformation can be found in Table 100 Backplane connector board andcontact assignments for three 4x ports - primary side on page 421 andBackplane connector board and backplane contact assignments for three$	
1x ports - r	primary side on page 422.	
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Example slot labeling:

- Chassis Slot 4 with 2 ports on the primary connector would be labeled as "C4P2".
- Tall Slot 6 with optional connector with two ports on the primary connector and one port on the optional connector would be "C6P2-O6P1".

9.1.3.2 MODULE PORT DESIGNATIONS

The addition of support for more than one port per slot / module connector in this version of the specification creates the need to provide a consistent means for user to match module and slot that support these additional ports. The following labeling convention is defined for modules and should be placed clearly on the module cover.

Label ^a	Description
C1P1	Primary backplane connector with port 1 populated
C1P2	Primary backplane connector with ports 1 and 2 populated
C1P3	Primary backplane connector with ports 1, 2 and 3 populated
C2P0	Second primary backplane connector with no port (This is for wide modules that use the second primary port for power or management or both)
C2P1	Second primary backplane connector with port 1 populated
C2P2	Second primary backplane connector with ports 1 and 2 populated
C2P3	Second primary backplane connector with ports 1, 2 and 3 populated
O1P0	Optional backplane connector with no port (This is for Tall modules that use the optional port for power or management or both)
01P1	Optional backplane connector with port 1populated (Tall Modules)
O1P2	Optional backplane connector with ports 1 and 2 populated
O1P3	Optional backplane connector with ports 1, 2 and 3 populated
O2P0	Second optional backplane connector with no ports (Tall Wide Modules)
O2P1	Second optional backplane connector with port 1 populated
O2P2	Second optional backplane connector with ports 1 and 2 populated
0000	Second antional backplane connector with parts 1, 2 and 2 populated

Table 90 Module Port Configurations and Labels

Ports location information can be found in Table 100 Backplane connector board and backplane contact assignments for three 4x ports - primary side on page 421 and Table 101 Backplane connector board and backplane contact assignments for three 1x ports primary side on page 422.

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Example module labeling:

- Standard module with 2 ports labeled as "C1P2"
- 2 Standard Wide Module with 2 port one on each connector = "C1P1-3 C2P1".
- Standard Wide module with 4 port two on each connector = "C1P2-C2P2".
- Tall module with 2 ports on primary connector = "C1P2"
- Tall Wide module with 12 ports 3 on each connector = "C1P3-C2P3-O1P3-O2P3"

o9-1.1.1: Chassis that support greater than one InfiniBand port per backplane connector shall populate the ports in the connector in the defined configurations in Table 88 Chassis Slot Configurations and Labeling on page 360 using the connector pin assignments defined for 4x ports in Table 101 Backplane connector board and backplane contact assignments for three 1x ports - primary side on page 422 or for 1x ports in Table 102 Backplane connector board and backplane contact assignments secondary side on page 423. Each slot shall be clearly labeled with the appropriate label from Table 88 Chassis Slot Configurations and Labeling on page 360.

o9-1.1.2: Modules that support greater than one InfiniBand port on each backplane connector shall populate the ports in the backplane connectors in the defined configurations in Table 89 Module Port Configurations and Labels on page 361 using the connector pin assignments defined for 4x ports in Table 101 Backplane connector board and backplane contact assignments for three 1x ports - primary side on page 422 or for 1x ports in Table 102 Backplane connector board and backplane contact assignments - secondary side on page 423. Each module shall be clearly labeled with the appropriate labels from Table 89 Module Port Configurations and Labels on page 361.

9.1.4 DATUM PLANE DEFINITION

The remaining sections of the mechanical specification, as well as the backplane connector specification, are based on detailed dimensioned drawings which all use a common set of reference Datum planes. These Datum planes are defined in Table 90 which is referenced to a vertical module orientation.

Table 90 Datum Planes

Datum Name	Definition	37 38
A	Horizontal plane, perpendicular to both the board and backplane, which passes through the center of the InfiniBand backplane connector	39 40
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Table 90 Datum Planes					
Datum Name	um Definition				
В	Vertical plane, coincident with the primary (connector) surface of the Infini- Band backplane				
С	Vertical plane, coincident with the primary component surface of the Infini- Band board				
D	Vertical plane, parallel to the backplane and coincident with the inside sur- face of the carrier's connector housing				
E	Vertical plane, parallel to Datum C and offset from Datum C by 7mm; coin- cident with the left side of the carrier plate.				

9.2 MODULE DESCRIPTION

The InfiniBand Module completely encloses the board. It minimally consists of a board, carrier, cover, standard ejector, and latch.



C9-2: Dimensions and tolerances for all modules shall conform to Figure

Figure 95 General Module Assembly Dimensions (Parametric)

Table 91 Par	ametric Dimens	sions for <mark>Figure 95</mark>
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Module Size	Dimension U	Dimension V	Dimension W	Dimension X
Standard	112.00	"U" - 7mm	29.0	"W" - 1mm
Standard Wide	112.00	"U" - 7mm	59.0	"W" - 1mm
Tall	245.35	"U" - 7mm	29.0	"W" - 1mm
Tall Wide	245.35	"U" - 7mm	59.0	"W" - 1mm



9.2.1 STANDARD SIZE MODULE

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9.2.2 TALL SIZE MODULE



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the second board, this entire space is free for venting provided the module still complies with Figure 123 on page 401.

Figure 104 Wide Module Critical Dimensions









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9.2.5 MODULE LEAD-IN



9.2.6 MODULE MATERIALS

C9-8: Module materials (carrier, ejector, latch) shall be galvanically compatible to zinc finishes and any EMI gasket material chosen. All module3940404141

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9.2.7 FILLER MODULES		4
	C9-9: Each unoccupied IB Slot shall contain a fi the EMI shielding of the faraday cage and specifie The filler module shall operate within the minimur established for normal modules (see <u>Table 94 or</u>	ller module to maintain ed airflow characteristics. m and maximum airflows page 399).
	A filler module may consist of, but is not limited t rier without a cover and with the Standard Modul	o, an empty module car- 6 e ejector and latch. 7
9.2.8 MODULE INDICATORS		8
	C9-10: All requirements detailed in <u>Section 9.2.</u> garding module LEDs.	8 shall be followed re-
	Each InfiniBand Module shall have two indicator one yellow. These indicators shall be positioned a modules (vertical module orientation) within the s area shown in <u>Figure 99 on page 368</u> , <u>Figure 103</u> on page 376, or <u>Figure 111 on page 380</u> .	12 13 14 13 14 15 16 12 12 13 14 13 14 14 15 16
	All LEDs shall meet the following wavelength an ments:	17 18 Iuminescence require-
9.2.8.1 WAVELENGTH		20
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	Table 92 Module Indicator Spe	22 ecification 23
	LED Wavelen	24 gth 25
	Green (Blue-Green) 555 - 565	nm 26
	Yellow (Amber) 582 - 592	nm 27
9.2.8.2 LUMINESCENCE		28 29
	Module Indicators shall have a minimum lumine per square meter over an area of at least 1.5 mm	scence of 80 candellas 30 n by 1.5 mm. 31
9.2.9 MODULE COMPONENT HE	IGHT	32
	Component height limitations are governed by the pend on material thicknesses of the board, carried	e module design and de- r and cover. The location 36 36 37 38 39 40 41
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of the primary side of the board in relation to the carrier is defined in <u>Sec-</u> tion 9.2.12 and can also be seen in the figures earlier in this section.

Note to Board Designers

There is decreased secondary side component height in the connector end of the module due to the recess for the ejector

9.2.10 MODULE EJECTOR AND LATCH DETAILS

Figure 113 through Figure 118 on page 390 show ejector and latch details and their relationships to respective modules and the chassis slots. Ejector may be removable, this will allow Ejectors to meet system vendor's requirement.

C9-11: All InfiniBandTM Modules **shall** have Standard ejectors.

Standard ejectors should comply with all dimensions specified in <u>Figure</u> <u>115 on page 387</u>

C9-11.a1: No feature of the Ejector when assembled to the Carrier shall extend beyond datum "E".

C9-11.a2: When Ejector is latched no feature of the Ejector shall extend
over the connector housing to an extent that it will interfere with the mated
connectors for the module it is attached to. For a universal handle (works
with all connectors that fit within the connector allocated area) this dimension shall not extend more than 2.8mm from Datum E over the carrier
connector housing.

C9-11.a3: No feature of the Ejector, when in the latched (closed) position, **shall** protrude more than 35mm in front of the Ejector pivot centerline.

C9-11.a4: Ejector **shall** have no sharp edges. Ejector edges **shall** comply with UL1439 as a minimum condition for safe handling.

C9-11.a5: To prevent the Ejector from being damaged in normal handling outside of the chassis the Ejector "Latch" **shall** require a minimum of 1.4 Newtons (5 ounces) of force to release the Ejector from the "closed" position.

C9-11.a6: When the ejector is latched the Ejector latch mechanism **shall** prevent the Module from being inadvertently released from its slot when a force of 111 Newtons (25 pounds) is applied to the face of the Module in the direction of removal of the Module.

C9-11.a7: The Carrier **shall** include a hard stop feature that prevents the Ejector from extending beyond 95 degrees from the latched position.

C9-12: All Tall form factors (including Tall Wide) modules **shall** have Upper ejectors.

Upper ejectors should comply with all dimensions specified in Figure 116 6 on page 388

C9-13: Each Ejector shall have a latch mechanism.

Latch mechanisms for all All InfiniBandTM Modules should comply with all dimensions specified in <u>Figure 117 on page 389</u>

Figure 118 on page 390 specifically deals with module assembly details and shows how the camming mechanism works during insertion and extraction. The camming motion itself allows a more controlled insertion with decreased potential for backplane connector damage.

Note to Designers

Ejector mechanism must be designed to handle insertion/extraction forces equivalent to two backplane connector's insertion force with a reasonable margin of safety to also include frictional forces from guides and EMI gaskets. The Ejector should be strong enough to withstand a module insertion force of 40 lb.













Mechanical Specification

The cover is used to prevent accidental contact of conductive components or solder leads with adjacent modules. It also prevents human contact with hot components, and provides ESD protection. The cover **may** also be used to control/channel airflow.

The design of the cover is not further specified, but it is recommended that all covers be easily removable, without tools, to aid the module manufacturing process.

Note to Designers

It is anticipated that most covers will be made from plastic with appropriate ESD treatment. If used, metal covers must make reliable electrical contact with the carrier to prevent EMI problems. An example of a module cover design can be found in appendix <u>Section 1.1, "Module</u> <u>Design Examples," on page 729</u>.

9.2.12 BOARD MOUNTING

C9-15: The PCB **shall** be secured to the module carrier. Regardless of the PCB thickness, the board primary side **shall** be located 7 +/- 0.3 mm from the outside of the carrier, datum E (see <u>Figure 98 on page 367</u>, <u>Figure 102 on page 371</u>, <u>Figure 106 on page 375</u>, or <u>Figure 110 on page 379</u> for standard, tall, wide, or tall wide modules respectively).

This dimension will insure the PCB will properly mate with the backplane connector. Recommended board mounting points can be found in <u>Figure 119</u> and <u>Figure 120</u>. These are recommendations **only** to facilitate some standardization of carrier design. These hole sizes, recommended in <u>Figure 119</u> and <u>Figure 120</u> are based on M3.5 size fasteners. The board designer is responsible for providing adequate mounting points to meet the EMI requirements of <u>Section 9.5.4</u>.

C9-16: Datums A and B are defined by the board connector position within the module. All Standard Modules **shall** comply with the dimensions that define these datums as shown in <u>Figure 97 on page 366</u>

C9-17: Datums A, AA, and B are defined by the board connector position within the module. All Tall Modules **shall** comply with the dimensions that define these datums as shown in <u>Figure 101 on page 370</u>

C9-18: Datums A and B are defined by the board connector position within the module. All Wide Modules **shall** comply with the dimensions that define these datums as shown in <u>Figure 105 on page 374</u>

Mechanical Specification

C9-19: Datums A, AA, and B are defined by the board connector position within the module. All Tall Wide Modules **shall** comply with the dimensions that define these datums as shown in Figure 109 on page 378

9.3 INFINIBAND BOARD PHYSICAL DESCRIPTION

9.3.1 BOARD DIMENSIONS

The dimensions included in this section describe the maximum allowable board dimensions within a module. The goal of this specification is to define the interface dimensions loosely to enable internal flexibility for the module designer.

<u>Figure 119</u> illustrates the board dimensions and connector location for a standard height module. <u>Figure 120</u> illustrates the board dimensions and connector locations for a tall height module.



Mechanical Specification

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Shown from Primary Side

- 100,13 -

МАХ

Figure 119 Board Dimensions for Standard Module

TOLERANCE: ±0.13



		2
9.3.2 PADDLE GUARD		3
	A paddle guard is a requirement for every IB board edge connector. The paddle guard helps to separate connector contacts and it adapts different thickness boards to the connector. A detailed description of the paddle	4 5 6
	quard is given in Section 10.3.2 "Paddle Guard" on page 414	7
	guard is given in <u>occulor 10.0.2, if addie Odard, on page 414</u> .	8
		9
3.3.3 BOARD THICKNESS		10
	C9-20: The thickness of InfiniBand printed boards is left to the module de-	11
	signer and shall range from 1.44 to 2.64 mm thick.	12
		13
	Although any thickness of board is allowable within this stated range,	14
	early adopters of InfiniBand TM should design to nominal thickness of ei-	15
	ther 1.6 or 2.4mm to take advantage of pre-tooled paddle guards. Regard-	16
	less of board thickness, the mounting shall comply with the 7mm	17
	face (see Figure 98 on page 367 Figure 102 on page 371 Figure 106 on	18
	page 375, or Figure 110 on page 379).	19
	<u>page or e</u> , or <u>regare recompage or e</u> ,r	20
9.3.4 INFINIBAND BOARD-EDGI		21
CIGH IN INDAND BOARD EDG		22
	Refer to IEC 61076 for detailed specification of the IB connector, board	23
	paddle routing, artwork, paddle guard details, and connector environ-	24
	mental information. For InfiniBand specific details for this connector, refer	20
	to <u>Chapter To. Backplane Connector Specification</u> .	20
		28
9.4 CHASSIS SLOT DESCRIPTION	NC	29
	Most of the mechanical definition for InfiniBand is centered around the	30
	module. InfiniBand does not define an entire "chassis"; it defines a min-	31
	imal set of requirements for a "chassis slot".	32
		33
		34
		35
9.4.1 BACKPLANE REQUIREME	NTS	36
	C9-21: Connector spacing between adjacent InfiniBand Slots shall be 30	37
	+/- 0.10 mm (see <u>Figure 121</u>).	38
		39
	C9-22: Connector spacing between two ports in a tall slot shall be 133.35 +/-0.20 mm (see Figure 121).	40 41 42
		- r 🚄

E

Recommendation to Chassis/Backplane Designers The backplane will likely be in the direct path of airflow for the module. Backplane height should be minimized to maximize module cooling. OPTIONAL BACKPLANE ΔΔ H -30.00±0.10 133.35±0.20 -REQUIRED BACKPLANE -BACKPLANE CONNECTOR

Figure 121 Backplane Connector Spacing
nfiniBand TM Architecture Release 1.2 /OLUME 2 - PHYSICAL SPECIFICATIONS	Mechanical Specification	October, 2004 FINAL
9.4.2 BACKPLANE CONNECTOR		
	Refer to <u>Chapter 10: Backplane Connector Spe</u> tails	ecification for connector de-
9.4.3 CHASSIS SLOT DETAIL		
	C9-23: Chassis slots shall comply with all dim specified in Figure 122.	nensions and tolerances
	BACKPLANE BACKPLAN	IE CONNECTOR
		В

CHASSIS SLOT

T

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13.00

TO CL OF

COMPRESSED EMI GASKET

221.50 ±0.5 TYP

This specification is intended to provide a consistent and repeatable method for ensuring a minimum level of integrity and environmental performance. This section details a standard test process that all chassis,

9.5 DESIGN CONSIDERATIONS

InfiniBand TM Architecture Release 1.2
VOLUME 2 - PHYSICAL SPECIFICATIONS

modules, and back-planes specified in this standard can use to be complient.

It is the system designer's responsibility to evaluate the relationship between the modules, chassis, and the system environment.

9.5.1 COOLING/THERMAL

The design objective is to supply the necessary airflow at the required temperature to insure that component temperatures are met. The chassis will provide sufficient cooling to meet all specifications when cooled by the fan(s) in the system enclosure. Fans are required to provide sufficient airflow to cool the modules under all conditions. Filler modules (or equivalent) will be required to prevent excessive airflow through spaces not occupied by modules.

9.5.2 COOLING REQUIREMENTS

The InfiniBand Module will be used in various ambient environments. To insure that the module meets temperature requirements for these various environments, two thermal profiles have been developed. Allowable inlet temperatures to the module for these thermal profiles are given in <u>Table 93</u>. Type "A" equipment refers to general purpose computing equipment and has been elevated under the assumption that the module receives pre-heated air. Type "B" refers to Network Equipment Building Systems (NEBS), Level 3.

Thermal Profile	Module Inlet Temperature (C)
A	0 - 45
В	0 - 55

Table 93 Operational Inlet Temperature Specification

To insure that components in the InfiniBand Module receive adequate cooling to meet reliability and temperature goals, minimum airflow rates per module have been specified. <u>Table 94</u> lists minimum airflow requirements per module type. It is the system engineer's responsibility to meet the minimum flow rate requirements. To insure adequate airflow it is important to insure that the combined module and system resistance curve intersect the fan curve(s) at a point above the minimum required flow rate

(see Appendix, <u>Section 1.2, "Computational Fluid Dynamics (CFD) Re-</u> sults," on page 736 for details).

Table 94 Minimum Airflow Rates Per Module

Module Type	Minimum Airflow, Type A cubic feet/minute (cfm)	Minimum Airflow, Type B cubic feet/minute (cfm)
Standard	6	9
Wide Standard	12	18
Tall	12	18
Wide Tall	24	36

C9-24: A chassis slot **shall** deliver the appropriate volumetric flow rate as specified in <u>Table 94</u> within the temperature range specified in <u>Table 93 on page 398</u>.

9.5.3 MODULE THERMAL DESIGN

The design of the module vents is critical to insure proper airflow. If the module design has too much resistance, components in the module may not receive adequate cooling air. On the other hand if the resistance of the module is too low, airflow may bypass other modules with higher resistances, reducing cooling airflow to these modules and therefore raising component temperatures. To insure cooling requirements can be met and to reduce the impact of bypass, Figure 123 on page 401 has been constructed giving minimum and maximum allowable resistances per module.

In addition, <u>Table 95 on page 401</u> has been constructed to give estimates of minimum and maximum vent areas per module to meet <u>Figure 123</u>. See Appendix, <u>Section 1.3</u>, <u>"Module Pressure Drop Testing," on page 739</u> for details associated with pressure drop testing of modules.

C9-25: Longitudinal airflow is the presumed norm for most general purpose computing equipment since it suggests the most dense packaging. In the most dense system implementations where a vertical module occupies all but a fraction of a chassis' height, all of the module's cooling air is presumed to pass through the connector housing vents travelling in a longitudinal direction through the module. The increased airflow requirements of systems conforming to <u>Table 94</u>, type B, may not be achievable in a purely longitudinal cooling scenario. Additional chassis height may be required to open up plenums above and/or below the module and to potentially add additional chassis venting in parallel with the connector

Mechanical Specification

housing venting. InfiniBandTM modules are required to have a minimum of open vent area along the top and bottom cover surfaces to facilitate additional airflow that would tend to flow in a more transverse direction. The decision is left to the system designer on whether or not to selectively open corresponding areas in the chassis to take advantage of transverse airflow. Regardless of the intended system implementation (longitudinal vs. transverse), all modules **shall** fall within the minimum and maximum resistance requirements for modules with longitudinal airflow shown in Figure 123 on page 401.

Note that the transverse airflow is the primary method for cooling in some market segments for example the telephone industry. Products targeted at these markets should insure adequate transverse venting to support the environment requirements. See annex A figure-143 for an example of a cover venting.

The curves in Figure 123 represent flow dependent resistance through a module. The pressure axis is constant regardless of module size. The flow rate axis has been differentiated for the Standard, Tall, Wide, and the Tall Wide size.

The connector housing areas specified for connectors may also be used for cooling provided that EMI attenuation is met.

Note to designers

The minimum flowrates described in <u>Table 94</u> were analytically determined to produce similar component temperatures at the respective inlet temperatures (<u>Table 93 on page 398</u>). In other words, a module designed for Type A environments should achieve similar component temperatures in Type B environments given the Type B enclosure provides the specified airflow



Table 95 Estimated Vent Area to Meet Specified ModuleResistances

Module Type	Minimum Open Vent Area (mm ²)	Maximum Open Vent Area (mm ²)
Standard	500	750
Standard Wide	1000	1500
Tall	1000	1500
Tall Wide	2000	3000

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9.5.4 EMI & ESD REQUIREMENTS

The implementation of the connection between Signal ground and Chassis ground is the responsibility of the system integrator. That connection should be made at a point that minimizes Electromagnetic Interference (EMI).

C9-26: Although not recommended, it is permissible to connect signal ground and chassis ground together on an InfiniBandTM module. If such connection(s) must be made, the InfiniBandTM module **shall** be fully EMC tested and qualified with this connection in place, and the module **shall** continue to meet the ESD specifications of sections <u>9.5.4.4.1</u> or <u>9.5.4.4.2</u> of the InfiniBandTM Mechanical specification, as well as all applicable FCC and EC EMC regulatory requirements. Since a logic to frame ground connection has a great potential for causing EMC problems if done improperly, modules making this connection **shall** be EMC tested with all supported I/O cables attached while exercising all I/O interfaces using typical customer data. Note that, in this instance, idle data alone are not sufficient to test the module I/O interfaces, as the InfiniBandTM idle data pattern has been defined to minimize EMI. Typical customer data **shall** be used when verifying EMC compliance.

C9-27: The module **shall** make a near continuous (no gap greater than 4 mm) EMI seal with the chassis and surrounding modules around its perimeter.

This is necessary in order to meet the stringent requirements of <u>Figure</u> <u>124</u>.

C9-28: The module **shall** provide an EMI gasket located per <u>Figure 98 on</u> <u>page 367</u>, <u>Figure 102 on page 371</u>, <u>Figure 106 on page 375</u>, or <u>Figure 110</u> <u>on page 379</u>.

C9-29: The chassis **shall** provide an EMI gasket on the top and bottom surfaces of the slot that mate with the module per <u>Figure 122 on page 397</u>.

C9-30: The gasket material **shall** be used with a nominal compression of up to 50% assuming it is compressed in a nominal gap of 1 mm. The gasket material **shall** be such that sliding contact causes no degradation. The gasket material **shall** have a finish that is galvanically compatible with zinc.

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9.5.4.1 EMI

The IB chassis and modules are of closed construction and are designed to maintain an EMI environment compatible with worldwide regulatory requirements for various classes of equipment. The modules and chassis, with conductive gaskets at the seams form a Faraday cage enclosure. The modules themselves will be an integral part of the chassis EMI containment strategy.

C9-31: Attenuation levels of <u>Figure 124</u> **shall** be met by **all** module carriers regardless of the relative level of internal module emissions.

The intent of Figure 124 is to provide a known level of containment at the carrier connector housing as an integral part of the system EMI enclosure. The curve specifies containment provided by the carrier as tested in a defined carrier attenuation reference chassis and in no way specifies the completed module EMI containment characteristics nor provides any assurance that the module will pass industry standards. Refer to normative appendix Section 1.5, "Carrier Attenuation Test Procedure (Normative)," on page 749 for EMI test procedures and appendix A1.6 Fabrication and Assembly of the EMI Reference Chassis on page 754 for the definition of the carrier attenuation reference chassis.

There is a carrier guide surface provided to allow a continuous contact between module top and bottom and chassis (conductive, resistive, or iso-

lated). This continuous contact along the length of the module is intended to limit interference between modules.



9.5.4.2 IB MODULE AIR VENT DESIGN FOR EMI

In order to meet the specification for shielding effectiveness given in Figure 124, the number, size, and spacing of the vent holes and the thickness of the connector housing must be controlled. To meet this specification, alternative vent designs have been evaluated using Finite Difference Time Domain (FDTD) modeling of an electric field source near the module connector housing. These results indicate that the required shielding effectiveness may be obtained by the designing the holes per Table 96.

Table 96 IB Module Vent Design for EMI Shielding		
Hole Size (LxW, mm)	Conn. Housing Thickness, mm	Hole Spacing, Center-Center, mm
2 x 2	0.5	3

Hole Size (LxW, mm)	Conn. Housing Thickness, mm	Hole Spacing, Center-Center, mm
2 x 2	1	3
4 x 4	2	5
6 x 6	4	7
8 x 8	8	9

Table 96 IB Module Vent Design for EMI Shielding

These vent dimension design points will permit the maximization of the air vent area (assumes no connectors) while still allowing an IB Module to meet the required EMI shielding effectiveness. If more shielding is necessary and less open area is needed for airflow, the diameter and number of holes may be reduced to the level required to provide the minimum open vent area as specified in <u>Table 95 on page 401</u>.

There are three levels of EMI containment that the module vendor must create; the first level is base carrier containment per the curve specified in fig which may be met simply by adhering to the guidelines in this section. The second level is an extension of the carrier mechanical containment which may be needed to compensate for holes created by various connectors. The first and potentially the second levels are required to meet the InfiniBand[™] specification. The third level, which is not addressed by this specification, is additional suppression at the board/component level which may be required for the product to pass agency tests.

9.5.4.3 IB EXTERNAL CONNECTOR EMI REQUIREMENTS

In addition to controlling the vent holes, connector openings in the connector housing must also be controlled. The maximum single opening allowed for an unshielded connector is a 10mm waveguide.

Note to designers

Waveguide thickness for one or more unshielded openings should conform to <u>Table 97</u>. All other unused or unshielded connector openings should be capped or provided with a second internal layer of shielding.

Table 97 Connector Housing Design Requirements forNormally Unshielded Connectors (i.e. Optical, UnshieldedTwisted Pair, etc.)

Connector Hole Size, mm	Number of Holes	Conn. Housing Thickness, mm
10 x 10	1	4
10 x 10	2	10
10 x 10	4	10
10 x 10	8	15

Refer to Appendix, <u>Section 1.4, "Shielding Effectiveness," on page 743</u> for the shielding attenuation provided by the waveguides shown in <u>Table 97</u>.

To avoid the use of waveguides for optical and other usually unshielded connectors, the connector itself must be shielded and its maximum aperture size limited to 4 mm.

9.5.4.3.1 SHIELDED CONNECTORS

D Shell or other shielded external connectors used on InfiniBand Modules must also be grounded through a full 360 degree contact around the interface between the connector and connector housing.

9.5.4.4 ESD

C9-32: All modules **shall** meet the appropriate ESD requirements described in <u>Section 9.5.4.4</u>

The ESD performance of the module **shall** meet the requirements of EN55024 following the procedures specified in IEC 61000-4-2. This standard requires that the InfiniBand Module provides sufficient shielding and grounding to meet ESD discharges of the appropriate category:

9.5.4.4.1 GENERAL PURPOSE COMPUTING EQUIPMENT

Level 2 test of 4 kV contact and 8 kV indirect both polarities

9.5.4.4.2 NETWORK EQUIPMENT BUILDING SYSTEMS (NEBS)

Level 4 test of 8 kV contact and 15 kV indirect both polarities

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Note to Designers

Meeting this requirement may require the use of light pipes or other techniques to recess the LEDs behind the connector housing surface.

9.6 CHASSIS AND CABLE ICONS

InfiniBand has leveraged the use of industry connectors for both copper and optical cables solutions. Because of this it is important to clearly identify InfiniBand cables and chassis connectors to avoid confusion and interoperability issues in multi-system environments. This highlights the need for a cable / connector icon.

9.6.1 ICONS

The following icons have been chosen to identify InfiniBand connectors for both cables and chassis. There is one icon for each cable width identified below. The use of the icon is optional but highly recommended.



Positive Negative	1 2 3 4 5 6 7 8
Figure 127 12x Icon	9
	1
o9-32.1.1: If an icon is associated with an InfiniBand port, it shall be a scaled version of the icon in <u>Figure 125</u> , <u>Figure 126</u> , or <u>Figure 127</u> that represents the interface width of the associated port. The icon shall not be less than 5mm height and 5mm in width.	1 1 1 1 1
The physical placement (top, bottom, side) and means (label, stamping or molding) is left to the implementation.	1
o9-32.1.2: If an InfiniBand icon is used to identify a copper or optical port and color coding is used to further enhance identification, Pantone 399 C (Green) shall be used.	2 2 2 2 2
Recommendation: If the InfiniBand icon is not used for port association and a color scheme is used., it is recommended that Pantone 399 C (Green) be used.	222
o9-32.1.3: If an icon is associated with an InfiniBand copper cable or optical fiber, it shall be a scaled version of the icon in Figure 125, Figure 126, or Figure 127 that represents the interface width of the associated cable or fiber. The size and contrast of the icon shall allow it to be visible from a distance of 0.5m under standard office lighting (500 lux).	2 3 3 3 3 3
Recommendation: If an icon is affixed, stamped or molded on an Infini- Band copper cable, it is recommended that it be placed in the space noted as "Icon Area" in Figure 61: 1x cable plug, Figure 62: 4x cable plug or Figure 64: 12x cable plug for copper cables or Figure 54 on page 234 of chapter 7 for optical pluggables.	3 3 3 3 3

CHAPTER 10: BACKPLANE CONNECTOR SPECIFICATION

10.1 INTRODUCTION

The connectors used to attach InfiniBand boards to InfiniBand backplanes are defined in this section. These connectors are a one-piece design mounted on the backplane, into which the InfiniBand board is inserted. One example of a suitable connector is specified in a draft New Work Proposal to the International Electrotechnical Commission (IEC). The detailed connector specification is included in final draft International Standard specification IEC 61076-4-115.

Two connectors are defined, one type for use with 1x and 4x boards, and a second type for 12x boards. InfiniBandTM boards and backplanes **shall** incorporate features shown in the appropriate sections below that specify the connector to board and connector to backplane interfaces. The 1x/4x and 12x connectors are externally identical, but the backplane footprint for the 1x/4x connector may have a reduced footprint from that used for the 12x connector if desired, due to the smaller number of contacts utilized. The board footprint for the connector contacts is the same in all cases.

The board edge "paddle" which mates with the connector is covered by a "paddle guard," a plastic shroud that fits over the paddle to protect the contacts during insertion and withdrawal of the board from the backplane connector. The paddle guard also serves to initiate closure of the connector housing when the board is inserted.

It is the responsibility of the connector supplier to perform the indicated tests on any backplane connectors to be used for InfiniBand boards and supply the data to potential customer companies to indicate compliance. It is recommended that the appropriate test groups specified in EIA-364.1000.01 for one piece connectors be used for qualification testing, using the following conditions:

- 50 mating cycles preconditioning
- Unmated exposure
- Five year product life
- Field operating temperature range up to 60 degrees C.

10.2 CONNECTOR DESCRIPTION

The InfiniBand backplane connector is a low insertion force connector with two sets of contacts. One set of contacts is used on the primary side of the InfiniBand board for high-speed differential pair signals and their

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corresponding grounds. A second set of contacts is used on the secondary side of the board for low-speed signals, power, and ground. The 12x connector contains 24 pairs of high-speed contacts (48 pins) and 18 low speed/power contacts. The 1x/4x connector contains eight pairs of high-speed contacts and the same number (18) low speed/power contacts.

Closure of the mechanism that engages the high-speed contacts is achieved by an internal mechanism which is actuated by outline features on the paddle guard. It is thus vitally important that the paddle guard outline not deviate from that described in the sections below. Sequencing of low speed/power contacts for hot insertion and withdrawal of boards is accomplished through the use of contact staggering, controlled by openings in the paddle guard, as described in <u>Section 10.3.2</u>.

Figure 128 shows a diagram of the backplane connector mounted on a backplane and an exploded board assembly with paddle guard to be inserted into the connector.



Figure 128 Backplane connector and board paddle (a), paddle guard assembly (b)

The mechanical, electrical, and environmental performance requirements for InfiniBand backplane connectors are defined in <u>Section 10.5</u>, <u>Section 10.6</u>, and <u>Section 10.7</u> respectively.

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10.3 CONNECTOR TO BOARD F	HYSICAL REQUIREMENTS	1
	Note that all drawing dimensions in the following sections are in millime- ters (mm), and are in accordance with ASME Y14.5M-1994. The con- nector drawings contained in this document are intended for reference purposes only. The reader is encouraged to consult IEC specification 61076 and the respective supplier's drawings for detailed design informa- tion.	2 3 4 5 6 7
10.3.1 BOARD CONTACT PATT	ERNS	8
	C10-1: The contact patterns shown in Figure 129 shall be used on the primary side of InfiniBand boards for high speed contacts to the backplane connector.	9 10 11
	C10-2: The contact pattern shown in Figure 130 shall be used on the secondary side of InfiniBand boards for low speed and power contacts.	12 13 14
	C10-3: The board paddle design shown in <u>Figure 131</u> shall be used on InfiniBand boards to insure interoperability.	15 16
	As mentioned in the previous sections, the sequencing of signals for hot insertion and withdrawal is controlled by the openings in the paddle guard, which are defined in the following section.	17 18 19 20
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Figure 130 Board contact pattern - secondary side of board



Figure 131 Board paddle outline - primary side of board

10.3.2 PADDLE GUARD

C10-4: InfiniBand boards **shall** utilize a paddle guard, a plastic shroud that fits over the board connector tab to protect the contacts during insertion and withdrawal of the board from the backplane connector. The paddle guard also actuates the closure of the high speed contacts and serves as a pin alignment and pin sequencing mechanism. 30 31 32 33 34

C10-5: The mechanical design shown in <u>Figure 132</u> through <u>Figure 135</u> **shall** be used for the paddle guard used on InfiniBand boards.

The paddle guard is designed to touch the InfiniBand backplane (as indicated by Datum B in Figure 132) when the module is fully inserted. The paddle guard offsets the IB board itself from the backplane; the exact relationships between the connector, board, and backplane are defined beginning in Section 9.3.

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C10-6: The paddle guard contact window design shown in Figure 133 shall be used for the high-speed contacts on the primary side of Infini-Band boards.

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C10-7: The paddle guard contact window design shown in Figure 134 shall be for low-speed/power contacts on the secondary side of Infini-Band boards.

This pattern provides for four levels of low-speed signal pin make/break timing. The use of these levels is defined in Chapter 12: Power / Hot Plug. Pin sequencing is controlled by the design of the openings in the paddle guard over the board contacts.



Figure 134 Paddle guard contact window detail, board secondary side



1.6 +/- 10% 1.76 mm 2.4 +/- 10% 2.64 mm SIGNAL ASSIGNMENTS ne InfiniBand signals are defined in Chapter 4: Port Signal Defin 10-8: InfiniBand boards and backplanes shall use the pin assignre is shown in Table 99 for high-speed signals, and those in Table 19 w-speed and power signals. 10-8.1.1: Boards and backplanes supporting multiple 4x ports sh e high-speed signal pin assignments shown in Table 100. 10-8.1.2: Boards and backplanes supporting multiple 1x ports sh e high-speed signal pin assignments shown in Table 101.	
2.4 ±/- 10% 2.64 mm SIGNAL ASSIGNMENTS the InfiniBand signals are defined in Chapter 4: Port Signal Definition 10-8: InfiniBand boards and backplanes shall use the pin assignts a shown in Table 99 for high-speed signals, and those in Table 11 w-speed and power signals. 10-8.1.1: Boards and backplanes supporting multiple 4x ports she high-speed signal pin assignments shown in Table 100. 10-8.1.2: Boards and backplanes supporting multiple 1x ports she high-speed signal pin assignments shown in Table 101.	
 SIGNAL ASSIGNMENTS he InfiniBand signals are defined in <u>Chapter 4: Port Signal Defin</u> 10-8: InfiniBand boards and backplanes shall use the pin assignre shown in <u>Table 99</u> for high-speed signals, and those in <u>Table 1</u>; w-speed and power signals. 10-8.1.1: Boards and backplanes supporting multiple 4x ports she high-speed signal pin assignments shown in <u>Table 100</u>. 10-8.1.2: Boards and backplanes supporting multiple 1x ports she high-speed signal pin assignments shown in <u>Table 101</u>. 	
 InfiniBand signals are defined in <u>Chapter 4: Port Signal Defin</u> 10-8: InfiniBand boards and backplanes shall use the pin assignments shown in <u>Table 99</u> for high-speed signals, and those in <u>Table 10</u> 10-8.1.1: Boards and backplanes supporting multiple 4x ports she high-speed signal pin assignments shown in <u>Table 100</u>. 10-8.1.2: Boards and backplanes supporting multiple 1x ports she high-speed signal pin assignments shown in<u>Table 101</u>. 	
 10-8: InfiniBand boards and backplanes shall use the pin assignres shown in <u>Table 99</u> for high-speed signals, and those in <u>Table 19</u> w-speed and power signals. 10-8.1.1: Boards and backplanes supporting multiple 4x ports she high-speed signal pin assignments shown in <u>Table 100</u>. 10-8.1.2: Boards and backplanes supporting multiple 1x ports she high-speed signal pin assignments shown in<u>Table 101</u>. 	<u>tions</u> .
 10-8.1.1: Boards and backplanes supporting multiple 4x ports sh e high-speed signal pin assignments shown in <u>Table 100</u>. 10-8.1.2: Boards and backplanes supporting multiple 1x ports sh e high-speed signal pin assignments shown in<u>Table 101</u>. 	nents <u>)2</u> for
10-8.1.2: Boards and backplanes supporting multiple 1x ports sh e high-speed signal pin assignments shown in <u>Table 101</u> .	all use
e high-speed signal pin assignments shown in <u>Table 101</u> .	all use

10.3.3 BACKPLANE CONNE

	Table 99	Backplane connector board and backplane contact assignments for single port -	2
primary side		primary side	3

Interface				Ro	ow a	R	ow b
				Contact	Signal Name	Contact	Signal Name
IB Sig	gnaling	Group	- High	Speed Different	tial Inputs and Out	puts	
12x	8x	4x	1x				
T/R	T/R	T/R	T/R	ax01	IBbxIn(0)	bx01	IBbxOn(0)
				ay01	IBbxlp(0)	by01	IBbxOp(0)
				ax02	IBbxIn(1)	bx02	IBbxOn(1)
				ay02	IBbxlp(1)	by02	IBbxOp(1)
				ax03	IBbxIn(2)	bx03	IBbxOn(2)
				ay03	IBbxlp(2)	by03	IBbxOp(2)
				ax04	IBbxIn(3)	bx04	IBbxOn(3)
				ay04	IBbxlp(3)	by04	IBbxOp(3)
				ax05	IBbxIn(4)	bx05	IBbxOn(4)
				ay05	IBbxlp(4)	by05	IBbxOp(4)
				ax06	IBbxIn(5)	bx06	IBbxOn(5)
				ay06	IBbxlp(5)	by06	IBbxOp(5)
				ax07	IBbxIn(6)	bx07	IBbxOn(6)
				ay07	IBbxlp(6)	by07	IBbxOp(6)
				ax08	IBbxIn(7)	bx08	IBbxOn(7)
				ay08	IBbxlp(7)	by08	IBbxOp(7)
				ax09	IBbxIn(8)	bx09	IBbxOn(8)
				ay09	IBbxlp(8)	by09	IBbxOp(8)
				ax10	IBbxIn(9)	bx10	IBbxOn(9)
				ay10	IBbxlp(9)	by10	IBbxOp(9)
				ax11	IBbxIn(10)	bx11	IBbxOn(10)
				ay11	IBbxlp(10)	by11	IBbxOp(10)
				ax12	IBbxIn(11)	bx12	IBbxOn(11)
				ay12	IBbxlp(11)	by12	IBbxOp(11)
				sa01 - sa11 & sb02 - sb11	IB_Sh_Ret - high contacts	n speed shield; m	nultiple redundant

Table 100 Backplane connector board and backplane contactassignments for three 4x ports - primary side		
	Table 100 Backplane connector boarassignments for three 4x por	d and backplane contact ts - primary side

Intorfago	Ro	ow a	Row b							
Interface	Contact	Signal Name	Contact	Signal Name						
IB Signaling Group - High Speed Differential Inputs and Outputs										
T/R, port 1	ax01	IBbx.1In(0)	bx01	IBbx.1On(0)						
	ay01	IBbx.1lp(0)	by01	IBbx.1Op(0)						
	ax02	IBbx.1In(1)	bx02	IBbx.1On(1)						
	ay02	IBbx.1lp(1)	by02	IBbx.1Op(1)						
	ax03	IBbx.1In(2)	bx03	IBbx.1On(2)						
	ay03	IBbx.1lp(2)	by03	IBbx.1Op(2)						
	ax04	IBbx.1In(3)	bx04	IBbx.1On(3)						
	ay04	IBbx.1lp(3)	by04	IBbx.1Op(3)						
T/R, port 3	ax05	IBbx.3In(0)	bx05	IBbx.3On(0)						
	ay05	IBbx.3lp(0)	by05	IBbx.3Op(0)						
	ax06	IBbx.3In(1)	bx06	IBbx.3On(1)						
	ay06	IBbx.3lp(1)	by06	IBbx.3Op(1)						
	ax07	IBbx.3In(2)	bx07	IBbx.3On(2)						
	ay07	IBbx.3lp(2)	by07	IBbx.3Op(2)						
	ax08	IBbx.3In(3)	bx08	IBbx.3On(3)						
	ay08	IBbx.3lp(3)	by08	IBbx.3Op(3)						
T/R, port 2	ax09	IBbx.2In(0)	bx09	IBbx.2On(0)						
	ay09	IBbx.2lp(0)	by09	IBbx.2Op(0)						
	ax10	IBbx.2In(1)	bx10	IBbx.2On(1)						
	ay10	IBbx.2lp(1)	by10	IBbx.2Op(1)						
	ax11	IBbx.2In(2)	bx11	IBbx.2On(2)						
	ay11	IBbx.2lp(2)	by11	IBbx.2Op(2)						
	ax12	IBbx.2In(3)	bx12	IBbx.2On(3)						
	ay12	IBbx.2lp(3)	by12	IBbx.2Op(3)						
	sa01 - sa11 & sb02 - sb11	IB_Sh_Ret - high speed shield; multiple redund contacts								

Interface	R	ow a	Row b							
Interface	Contact	Signal Name	Contact	Signal Name						
IB Signaling Group - High Speed Differential Inputs and Outputs										
T/R, port 1	ax01	IBbx.1In(0)	bx01	IBbx.1On(0)						
	ay01	IBbx.1lp(0)	by01	IBbx.1Op(0)						
	ax02		bx02							
	ay02		by02							
	ax03		bx03							
	ay03		by03							
	ax04		bx04							
	ay04		by04							
T/R, port 3	ax05	IBbx.3In(0)	bx05	IBbx.3On(0)						
	ay05	IBbx.3lp(0)	by05	IBbx.3Op(0)						
	ax06		bx06							
	ay06		by06							
	ax07		bx07							
	ay07		by07							
	ax08		bx08							
	ay08		by08							
T/R, port 2	ax09	IBbx.2In(0)	bx09	IBbx.2On(0)						
	ay09	IBbx.2lp(0)	by09	IBbx.2Op(0)						
	ax10		bx10							
	ay10		by10							
	ax11		bx11							
	ay11		by11							
	ax12		bx12							
			h. 40							

The physical locations of the signals on the backplane are defined in <u>Sec-</u> 33 tion 10.4. 34

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z12

z13

z14

z15

z16

z17

z18

Backplane connector board and backplane contact assignments - secondary side								
Contact	Signal Name							
z01	VA_Ret							
z02	VA_In							
z03	IMxDat							
z04	IMxClk							
z05	IMxPReq_L							
z06	IMxInt_L							
z07	VBxPFW_L							
z08	VBxCap							
z09	IMxPRst							
z10	VBxEn_L							
z11	VB_Ret(0)							

VB_In(0)

VB_In(1)

VB_Ret(2)

VB_In(2)

VB_In(3)

VB_Ret(3)

VB_Ret(1)

Table 102

C10-9: Signals shall utilize physical contact locations on the paddle and paddle guard as shown in Figure 136.





InfiniBand TM Architecture Release 1.2 VOLUME 2 - PHYSICAL SPECIFICATIONS	Backplane Connector Specification	October, 2004 FINAL
10.3.4 BACKPLANE WIRING		
	C10-9.1.1: Backplane wiring shall be designed with 10 ferential impedance.	0+/- 10% Ohms dif- 2 3
10.3.5 BOARD WIRING		4
	C10-9.1.2: Board wiring shall be designed with 100+/- ential impedance.	- 10% Ohms differ- 6 7
10.4 CONNECTOR TO BACKPLA	ANE PHYSICAL REQUIREMENTS (MOUNTING SPECIFIC)	8
10.4.1 BACKPLANE INTERFACE	- INITIAL COMPRESSION / PRESS-FIT MOUNTING	9
	The initial backplane connector is based on compression high-speed differential contacts and conventional press the low-speed and power contacts. Press-fit posts are tional mounting points on the primary board side.	on mounting for the ss-fit mounting for also used as addi- 12 13
	While this mounting technique is initially believed to or nation of high speed signal integrity and manufactural acknowledges that other mounting techniques may ev these designs will require additional specification require fore, sections are reserved and will be added as require sions of this standard.	ffer the best combi- bility, this standard rolve over time and irements. There- ired in future revi-
	C10-10: Backplane connectors used for connection to shall be intermateable with the board paddle and padd in Sections $10.3.1$ and $10.3.2$.	InfiniBand boards 21 lle guard described 22 23
	Figure 137 shows a drawing one example of a backpl housing of this type.	ane connector 24 25 26
	C10-11: The external dimensions of backplane connernection to InfiniBand boards shall not exceed the outlin shown in Figure 137.	ctors used for con- ine dimensions 28 29 30 31 32 33 34 35 36 37 38 39 40 40 41



Figure 137 Compression/press-fit backplane connector housing

Figure 138 indicates the resting location of the contacts on the board with respect to the connector housing. The high speed contacts are on the left, and the low speed/power on the right.



Figure 138 Contact resting locations on board

10.4.1.1 BACKPLANE INTERFACE REQUIREMENTS

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This section defines the backplane interface for high-speed compression / low-speed press-fit mounted backplane connectors.

The contact footprint shown in <u>Figure 139</u> should be used for a 12x implementation using a compression/press-fit backplane connector.

Backplane Connector Specification

October, 2004 FINAL

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The signal contact assignment shown in <u>Figure 140</u> should be used on 12x backplanes 12x using a compression/press-fit backplane connector.

Note

Should the designer choose to do so, the 1x/4x connector footprint may be implemented omitting signal contacts ax5-ax12, bx5-bx12, and s5-12, as shown in <u>Figure 141</u>. However, all remaining contacts must be included as shown, and the 12x contact pattern shown in <u>Figure 129</u> and <u>Figure 130</u> must still be included on the module board.



Table 103Recommended hole dimensions for
compression/press-fit backplane connectors

Hole type	Drilled hole size	Finished hole size	Units
Low speed/power	0.701±0.025	0.61±0.05	mm
Retention pins (on high speed side of connector)	1.150±0.025	1.02±0.076	mm

Notes

1. In the event that the press-fit holes are solder plated, the finished hole dimension is the diameter after solder plating.

2. Nickel plating shall not be used in press-fit contact holes.

The requirements for contacts used on InfiniBand backplanes are defined in <u>Section 10.4.1.2</u>.

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It is also recommended that a compression / press-fit style backplane connector meet the requirements in <u>Table 105</u>.

Symbol	Parameter	Minimum	Maximum	Units	Comment
t _{bp}	Backplane thickness	1.44	not limited by connec- tor design	mm	1.6 mm nominal
W _{bp}	Backplane coplanarity/ warpage		0.2	mm / 100 mm	
t _{pm}	Contact pad finish, high speed contacts	0.76 min. Au over 1.27 min. Ni		μm	Electroplated. Nickel plating shall not be used in press-fit contact holes
	Contact surface finish	TBD	N/A		

Table 104 Backplane requirements - compression / press-fit

Recommendation

To insure reliable connection, backplane contacts should be free of any residues from the board manufacturing processes (such as solder flux, contact masking tape adhesive, etc.) as well as subsequent handling.

Table 105 Recommended connector to backplane mechanical parameters

Symbol	Parameter	Applicable contacts	Minimum	Maximum	Units	Conditions/Comment	
F _{ncp}	Contact normal force	high speed	100		cN	per conductor	3
S _{hcp}	Contact Hertz stress	all	170		kpsi	per contact beam	3
D _{wp}	Contact Wipe	high speed	0.13		mm	backplane interface only	

10.4.2 BACKPLANE INTERFACE – SURFACE SOLDER MOUNTING

The definition of this interface may be present in future versions of this specification.

10.4.3 BACKPLANE INTERFACE – PRESS-FIT MOUNTING

The definition of this interface may be present in future versions of this specification.

10.5 MECHANICAL PERFORMANCE REQUIREMENTS

C10-13: Connectors to be used for connection to InfiniBand boards and contacts on those boards shall meet or exceed the physical and mechan-ical performance requirements listed in Table 106.

Table 106 Backplane connector to board mechanical performance requirements

Symbol	Parameter		Applicable Contacts	Minimum	Maximum	Units	Conditions/Comment
N	Durability		All	250		mat- ing cycles	With paddle guard installed; no more than 1% of contacts with exposed base metal. The specified low level con- tact resistance shall not be exceeded.
Fi	Insertion force	1x/4x			30	Ν	
		12x			75	-	
F_w	Withdrawal force	1x/4x			30	Ν	
		12x			75		
F _{rc}	Housing contact retention force		All	5		Ν	Backplane interface only
d _{1I}	Distance between con tact mating on board insertion/withdrawal		low speed	4.5		mm	First to last low speed con- tacts
t _{pm}	Contact finish in con- tact area option 1			0.76 Au over 1.27 Ni		μm	
t _{pm}	Contact finish in con- tact area option 2			0.51 PdNi with Au flash over 1.27 Ni		μm	Min. 75% Pd in PdNi alloy
F _{rpg}	Paddle guard reten- tion force			100		N	to board paddle

It is further recommended that the backplane connector contact interface to the board meet the mechanical parameters specified in Table 107.

Note

Inserting a paddle guard alone into a backplane connector without a board may cause the paddle guard to be irretrievably retained in the connector, and may cause damage to the connector.
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Table 107 Recommended connector to board mechanical parameters

Symbol	Parameter	Applicable contacts	Minimum	Maximum	Units	Conditions/Comment
F _{ncb}	Contact Normal Force	low speed	100		cN	per conductor
		high speed	100		cN	per conductor
S _{hcb}	Contact Hertz stress	all	170		kpsi	per contact beam
D _{wb}	Contact wipe	low speed	1.5		mm	board interface only
		high speed	1.5		mm	board interface only

10.6 ELECTRICAL PERFORMANCE REQUIREMENTS

C10-14: Backplane connectors to be used for connection to InfiniBand boards shall meet or exceed the electrical performance requirements listed in Table 108.

Table 108 Connector electrical performance requirements

Symbol	Parameter	Applicable contacts	Minimum	Maximum	Units	Conditions/Comment
LLCR	Low level contact resistance - initial	low speed/ power		15	mΩ	through testing per EIA 364-23
		high speed		30	mΩ	-
∆LLCR	Low level contact resistance - change	low speed/ power		10	mΩ	through testing per EIA 364-23, as a result of any test group step
		high speed		20	mΩ	-
I _{max}	Current rating	low speed/ power	2.5		A	per EIA-364-70 or IEC 512-5-1 Test 5a, at 30° C. temperature rise above ambient with all contacts energized
		high speed	0.5		A	per conductor pair, per EIA-364-70 or IEC 512-5-1 Test 5a, at 30° C. temperature rise above ambient
L _{IS}	Inductance	low speed/ power		30	nH	measured as loop inductance of two adjacent pins per EIA 364-69 at 1 MHz

Table 108 Connector electrical performance requirements

Z _{dco} (peak)	Differential Imped- ance (peak)	high speed	90	110	Ω	Average value measured over the propagation delay of the connector at	
Z _{dco} (nom)	Differential Imped- ance (average)	high speed	95	105		100 ps rise time (at the connector), per draft EIA 364-108; includes con- nector, board and backplane pads, and vias	
L _{co}	Insertion loss	high speed		0.75	dB	frequencies up to 1.25 GHz, per EIA 364-101	
S _{cop}	Within pair skew	high speed		5	ps	by design; measurement not required.	
J _{co}	Jitter	high speed		10	ps	by design; measurement not required.	
NEXT _c	Near end crosstalk	high speed		3	%	measured differentially with all adja- cent neighbor pairs driven at 100 ps rise time, per EIA 364-90	

10.7 Environmental Performance Requirements

C10-15: Connectors to be used for connection to InfiniBand boards **shall** meet or exceed the environmental performance requirements of EIA-364.1000.01, including exposure to benign dust and Mixed Flowing Gas consistent with the required product life as defined in <u>Section 10.1</u>.

Unless otherwise noted, successful completion of a given test is indicated by an acceptable Low Level Contact Resistance measurement upon completion of the test, as defined above.

CHAPTER 11: LOW SPEED ELECTRICAL SIGNALING

		3
		4
11.1 INTRODUCTION		5
	This chapter describes the electrical signaling used on the low speed con-	6
	tacts of the InfiniBand backplane connector. Specifically, these are those	/
	Signals within the Bulk Power, Auxiliary Power and System Management	0
		10
11.2 GENERAL REQUIREMENTS	FOR ALL GROUPS	11
11.2.1 ESD		12
	C11-1: InfiniBand signal and power contacts shall withstand ESD volt-	13
	ages as defined in Section 6.3.1, "ESD," on page 178.	14
		15
11.3 BULK POWER GROUP		16
	This section provides the electrical specifications for the Bulk Power	17
	power design. The parameters reference the topologies in Section 12.1.3	10
	on page 457.	20
		21
11.3.1 VB_IN		22
	The bulk power input is provided on the VB_In pins and provides for either 25W or 50W of power capability.	23 24
	C11-2: The backplane shall supply 25W of power capability on the VB_In pins.	25 26 27
	o11-1 . The backplane may optionally provide an additional 25W on the	28
	VB_In pins for a total of 50W capability.	29
		30
	C11-3: If the backplane only provides 25W of power to a port, it shall not	31
	assent the VDXCap signal for that port.	32
	o11-2: If a module has multiple power groups available, the VB_In pins	33
	shall not be connected between power groups (ports). The outputs of the local DC-DC converter(s) may be connected together.	34 35
	The electrical parameters for these pips are shown in Table 109 on page	36
	<u>436</u> .	37
		30 20
11.3.2 VB_RET		40
	The VB_Ret connections are specified on the connector to support the isolated configuration. These Power returns may be connected locally to	41 42

Low Speed Electrical Signaling

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logic ground on the IB Module to support Class I, or left isolated on the IB Module to be connected at a common point in the system to support Class II. The IB Modules power class must be reported in the modules *ModuleInfo*. The detailed description of the *ModuleInfo* information is located in <u>Section 13.3.2.10</u>.

11.3.3 BULK POWER PARAMETERS

C11-4: The Bulk Power pins, **VB_In** and **VB_Ret**, **shall** conform to the values defined in <u>Table 109</u>.

The nominal bulk voltage is 12V.

Note: All capacitance values specified in <u>Table 109</u> include the tolerances 11 of the components implemented.

Symbol	Parameter	Minimum	Maximum	Units	Comment
Board					
V _{Bulk}	Operational Voltage - Static	10	14	V	Measured at the bottom of the backplane connector.
	Operational Voltage - Tran- sient		16 ^a	V	Maximum voltage that can be dealt with for 1 ms and still operate. Measured at the bot- tom of the backplane connec- tor.
I _{BAvg}	Average Current		2.5	A	The average current shall not exceed the values shown within any 1 sec. sliding win- dow under all conditions.
I _{BRefRip}	Reflected Ripple Current (Peak-Peak)		100	mA	The ripple that the board may produce into a resistive load equivalent to the module's maximum load. This is mea- sured from 5Hz to 20MHz.
I _{BMax}	Peak Current		2.8	A	The current that the board shall provide limiting for applicable during power-on sequences and during nor- mal operation
I _{BLeakage}	Leakage Current		20	mA	The maximum current that a module may draw when VBxEN_L is de-asserted. (Power is disabled)

Table 109 Bulk Power Parameters

	Symbol	Parameter	Minimum	Maximum	Units	Comment
	didt _{BMax}	Current Transient		40	A/ms	The current transient that the board shall provide limiting for applicable during power- on sequences and during normal operation. I _{BMax} must not be violated.
	t _{BCT}	Current Transient Time		28	ms	I _{BMax} / didt _{BMax}
	C _{BIn}	Initial Hot Plug Capacitance		5000	pf	Capacitance at hot plug con- nector mating.
	C _{BBulk}	Input Capacitance		500	μf	Refer to <u>Figure 152 on page</u> <u>458</u> and <u>Figure 153 on page</u> <u>459</u> .
	t _{BOn}	Turn-on Time	-	500	ms	This is measured from the AND of VBxPFW_L being asserted inactive AND VBxEn_L being asserted active AND <u>Local Power</u> <u>Enable</u> being asserted active to when the converter is enabled and within regula- tion.
	t _{BOff}	Turn-off Time		1	ms	This is measured from the deassertion of VBxEn_L deassertion time is the hot removal case.
	a. These are backplane c event.	e the tolerance requirements, ac connector. VB_In must return to v	ross a 20 MHz within the static	z bandwidth, a c voltage speci	t the bacl fication (\	<plane infiniband<br="" of="" side="" the="">/_{Bulk}) within 1 ms after a transie</plane>
3.1 Me	EASUREMEN	ITS				
		C11-5: Bulk vo backplane side	Itages desig of the Infini	nated in <u>Ta</u> l Band backp	ole 109 plane co	shall be measured at the onnector.
4 VBx	EN_L					
		The VBxEn_L seated prior to	pin provides	s for strong	sensing ng. This) that the IB Module is full s signal is assigned on the

Table 109 Bulk Power Parameters

The signal is terminated as shown in Figure 142 on page 438. The backplane provides for the overriding "Asserted" level by drawing current through the VBxEn_L pin. The maximum current required to drive the VBxEn_L signal asserted is I_{VBxEN_ol} . The voltage level required to assert the VBxEn_L signal is implementation dependent. The module pro-

to break".

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vides for the default "Not Asserted" level. The "Not Asserted" voltage level is implementation dependant, the circuit shown in Figure 142, has a "virtual"² pull-up R_{PU} to VB_In as an indication to use the bulk voltage rail to drive the level. The maximum voltage level on VBxEn_L that may applied to the backplane is $V_{VBxEN\ Max}$ Please see Table 110 on page 443 for the values of V_{VBxEN_Max} and $I_{VBxEN_ol}.$ Not Asserted (Bulk Power Disabled) Asserted (Bulk Power Enabled) VB In VB In **R**_{PU} R_{PI} Power Power **VBxEn VBxEn** L Sequence Sequence Circuit Circuit VB_Ret Backplane Module Backplane Module >>> indicates backplane connector Figure 142 VBxEn_L Termination 11.3.4.1 GENERAL RULES C11-6: The VBxEn L signal shall conform to the DC parameters defined in Table 110 on page 443. 11.3.4.2 MODULE RULES C11-7: The module shall provide the VBxEn_L signal for each power port. Also see Section 12.4, "Module Power Rules," on page 467 for additional rules pertaining to this signal on the module. 11.3.4.3 CHASSIS RULES o11-3: A "Managed Chassis" may optionally control the VBxEn_L signal to selectively enable or disable the power sequence circuit of the module. Also see Section 12.5, "Chassis Power Rules," on page 470 for additional rules pertaining to this signal on the chassis.

2. "Virtual", in this context, means it is to behave from the outside as a pull up to something like 5 Volts but it is to get its source of power from the **VB_In** for a Class II module. A Class I module may use either **VB_In** or **VA_In**.

11.3.5 VBxCAP

The Bulk Capability (**VBxCap**) signal is bidirectional and indicates the power capability provided by the chassis and the power required by the IB Module.

For modules requiring between 25 and 50W, a backplane must be capable of delivering this power on the **VB_In** pins. IB Modules (single wide high or double wide standard) monitor the level of the **VBxCap** pin to determine if the backplane in which the module is plugged is capable of delivering this power. A low level (not asserted) indicates that the port is only capable of 25W; a high level (asserted) indicates that 50W is available. The "level" is referenced to **VA_Ret.** Refer to Figure 143 on page 439 and Figure 144 on page 440 for termination structures.

A 50W IB Module supplies a pull-down R_{PD} on the board to provide an initial 25W indication to the IB Management Link Controller. The signal can be 1) driven high by a 50W backplane with a pull-up R_{PU} to indicate a 50W capability or 2) be grounded by a 25W backplane. In the second situation, the backplane does not provide the power required by the IB module. The module must therefore either a) not power on or b) recognize that it is plugged into a backplane that will only deliver 25W and take appropriate actions to limit its power accordingly.

25W Capable Backplane Example (Not Asserted)

50W Capable Backplane Example (Not Asserted)





Backplane

VA In

Module

indicates backplane connector

Figure 143 VBxCap Termination - 25W IB Module

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					2
25W Capable Backplane Example (N	lot Asserted)	50W	Capable Backp	lane Example (Asserted)	2
	,		I I I I I I I I I I I I I I I I I I I		4
			VA_In		5
					6
Ì]	R _{PU}		7
VBxCap		,	VBxCap		8
					9
– R _{PD}				R _{PD}	10
					11
Backplane Modu	le		Backplane	Module	12
>>> indicates backplane connect	ctor		I I I		13
Fig	ure 144 VBx	Cap Terminatio	on - 50W IB M	odule	14
11.3.5.1 GENERAL RULES		•			15
	C11 0. The		- k - II <i>f</i>	to the DC representation defined	16
	in Table 110	on page 443	shall conform	to the DC parameters defined	10
		on page 110.			10
	The para	ameters V _{VBxCap_}	$_{\mathrm{ph}}$ and $\mathrm{v}_{\mathrm{VBxCap}_{-1}}$	Ja define the required voltage	20
	levels fo	r the InfiniBand I	Management I	Device (IBMD) and backplane.	21
	I ne para	ameter I _{VBxCap_Lea}	_{akage} defines the	e maximum leakage current	22
	R _{PD} defir	e the allowed va	alues for the pu	Ill-up and pull-down devices re-	23
	spective	ly. The values fo	r these param	neters are defined in Table 110	24
	on page	<u>443</u> .			25
11.3.5.2 MODULE RULES					26
	C11-0- A po	wer port on a mo	dule requiring	25W or less shall directly con-	27
	nect VBxCa	p to VA Ret to	communicate	to a 50W capable backplane	28
	that the port	will consume no	o more than 2	5W.	29
					30
	C11-10: A p	ower port on a m	odule requirin	g between 25W and 50W shall	31
		cified in Table 1	10 on page 4/	13	32
	value as spe		TO OIL PAYE 4	<u></u> .	34
	Implement	tation Note			35
					36
	Typically a	vailable 10% res	isters of 2.2K	Ω for R _{PU} and 3.0KΩ for R _{PD} are	37
	recommen	ded for use on tl	he VBxCap si	gnal.	38
	-44.4.1/		a alula ini		39
	011-4: It a p	ower port on a r	noaule require	es between 25W and 50W, the	40
	plane in whi	ch the module is	s plugged is ca	apable of delivering this power.	41
			1 335576	,	42

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	If the port detects a voltage less than or equal the module shall either a) not draw power fro nize that it is plugged into a backplane that w take appropriate actions to limit its power dra	to v_{VBxCap_ol} on VBxCap , om the port or b) recog- vill only deliver 25W and aw accordingly.
11.3.5.3 CHASSIS RULES		4
	C11-11: A power port on a chassis that delivers rectly connect VBxCap to VA_Ret .	less than 50W shall di- 6 7
	C11-12: A power port on a chassis that can delive vide R_{PU} pull-up to VA_In .	er at least 50W shall pro- 9 10
11.3.6 VBxPFW_L		11
	The Bulk Power Fail Warning (VBxPFW_L) sign system or chassis power supply and serves two	al originates from the 13 functions. 14
	 When it transitions from deasserted (high) to alerts the IB Module that bulk power may be fied tolerance, and is only guaranteed to rem t_{VBINVALID}. When an adapter sees this transitie ever house keeping functions it deems neces power loss. 	asserted (low), this about to go out of speci- nain within tolerance for on, it may begin what- ssary to prepare for
	 When it transitions from asserted to deasser Module card that bulk power has been within at least t_{VBVALID}. Modules should not begin in signal has been sampled deasserted. 	ted, this alerts the IB o specified tolerance for itialization until this 24
11.3.6.1 GENERAL RULES		25 26
	C11-13: The VBxPFW_L signal shall conform to fined in <u>Table 110 on page 443</u> and the AC param 443.	o the DC parameters de- neters <u>Table 111 on page</u> 28 29
11.3.6.2 MODULE RULES		31
	o11-5: IB Modules may optionally utilize VBxPF	W_L functionality.
	Recommendation to System Designer	34
	Buffering of this signal on a slot basis prevents of from affecting adjacent slots.	glitches on VBxPFW_L 36 37
11.3.6.3 CHASSIS RULES		38
	C11-14: The Chassis shall provide the defined very port.	VBxPFW_L function for 40 41 42

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Low Speed Electrical Signaling

	C11-15: Once the VBxPFW_L signal transitions to asserted, it shall remain asserted for a minimum of t _{PW_low} even if the bulk power did not go out of specification.	1 2 3
	C11-16: Once the VBxPFW_L signal transitions to deasserted, it shall remain deasserted for a minimum of t_{PW_high} even if the bulk power immediately indicates a failure is imminent.	4 5 6
11.3.7 VBx* SIGNAL PARAME	TERS	7 8
	This section defines the electrical parameters for the control signals within the Bulk Power group.	9 10
	If parameters apply to all signals beginning with " VBx ", they are referred to as " VBx *"; the "*" indicates a generic placeholder. If parameters apply to specific signals, these are named explicitly.	11 12 13
		14
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		39 39
		-10

-0 41 Table 110 VBx* DC Specifications

11.3.7.1 VBx* DC SPECIFICATIONS

Symbol	Parameter	Minimum	Maximum	Units	Comments
V _{VBxEn_Max}	VBxEn_L maximum voltage		5.5	V	See <u>Figure 146 on page</u> <u>446</u> .
I _{VBxEn_ol}	VBxEn_L output low	4		mA	See <u>Figure 146 on page</u> <u>446</u> .
I _{VBxEn_il}	VBxEn_L input low		4	mA	See <u>Figure 146 on page</u> <u>446</u> .
V _{VBxCap_oh}	VBxCap output high - module	2.1	3.63	V	See <u>Figure 143 on page</u> <u>439</u> .
	VBxCap output high - backplane	2.1	5.50	V	See <u>Figure 143 on page</u> <u>439</u> .
V _{VBxCap_ol}	VBxCap output low	-0.5	0.8	V	See <u>Figure 143 on page</u> <u>439</u> .
R _{PU} ^a	Pull-up Termination	1.870	2.500	KΩ	
R _{PD} ^a	Pull-down Termination	2.625	3.630	KΩ	
I _{VBxCap_Leakage}	VBxCap leakage current		+/- 100	μA	See <u>Figure 143 on page</u> <u>439</u> .
V _{VBxPFW_L_il}	VBxPFW_L Input Low Voltage	-0.5	.8V	V	See <u>Figure 145 on page</u> <u>445</u> .
$V_{VBxPFW_L_ih}$	VBxPFW_L Input High Voltage	2.1	3.63	V	See <u>Figure 145 on page</u> <u>445</u> .

a. The values specified for this parameter do not include all tolerances of implemented components.

11.3.7.2 VBxPFW_L AC SPECIFICATIONS

Table 111 VBxPFW_L AC Timing Specifications

Symbol	Parameter	Minimum	Maximum	Units	Comments	3
t _{VBINVALID}	VBxPFW_L Asserted To VB_In	2		ms	See Figure 145 on page	= 3
	Invalid				<u>445</u>	3
						3
						Э
						З
						З
						3
						3
						4
						4
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Symbol	Parameter	Minimum	Maximum	Units	Comments
VBVALID	VB_In Valid to VBxPFW_L Deasserted	100		ms	See <u>Figure 145 on page</u> <u>445</u>
t _{PW_low}	Signal Pulse Width Low	1		ms	See <u>Figure 145 on page</u> <u>445</u>
PW_high	Signal Pulse Width High	10		μs	See <u>Figure 145 on page</u> <u>445</u>
t _{Fall}	Fall Time		300	ns	See <u>Figure 145 on page</u> <u>445</u>
t _{Rise}	Rise Time		1000	ns	See <u>Figure 145 on page</u> <u>445</u>



	VB_In ////	1
	VB_PFW_L	2 3 4
	$\underbrace{VBxEN_L}$	5 6
	LocalPowerEnable	7
	V _{Out}	8 9 1(
	$\underbrace{ VBxEN_L } \underbrace{ t_{BOff} \rightarrow } $	11 12 13
	I _{BLeakage}	14
	Figure 146 VBxEn_L Timing Measurements	10 17 18
11.4 AUXILIARY POWER GROU	IP	19 20
	This section provides the electrical specification for the Bulk Power Group Pins and contains the pertinent parameters needed by the board power design. The parameters reference the topologies in <u>Section 12.1.3 on</u> <u>page 457</u> .	2 22 23 24
11.4.1 VA_IN		2:
	Auxiliary power input is provided on the VA_In pin and provides for up to 2.4W based on form factor as defined in <u>Table 116 on page 461</u> .	27 28 29
11.4.2 VA_RET		3(
	The VA_Ret connection provides the return path for the Auxiliary power functions and is connected to logic ground on the board.	3 3 3
11.4.3 AUXILIARY POWER PAR	AMETERS	34 21
	C11-17: The Auxiliary Power pins, VA_In and VA_Ret , shall conform to the values defined in <u>Table 112</u> .	3
	The nominal auxiliary voltage is 5V.	3
	Note : All capacitance values specified in <u>Table 112</u> include the tolerances of the components implemented.	4 4 4

Symbol	Parameter	Minimum	Maximum	Units	Comment
Board					
V _{Aux}	Operational Voltage - Static	4.60	5.50	V	Measured at the bottom backplane connector.
I _{AAvg}	Average Current		.260	A	The average current shall not exceed the values showr within any 1 sec. sliding win- dow under all conditions.
I _{AMax}	Peak Current		.390	A	The current that the board shall provide limiting for applicable during power-on sequences and during nor- mal operation
didt _{AMax}	Current Transient	-	0.1	A/ms	The current transient that the board shall provide limiting for. This is applicable during power-on sequences and during normal operation
LS					
C _{AIn}	Initial Hot Plug Capacitance		1000	pf	Capacitance at hot plug con- nector mating.
C _{ABulk}	Input Capacitance		100	μf	
t _{AOn}	Turn-on Time		2	S	This is measured from the presence assertion of the IMxPRst pin. See Figure 147 on page 448.

Auxiliary Power Parameters Table 112

	<u>VA_In ////</u>
	IMxPRst ////
	$\underbrace{\mathbf{IBMD}_{\text{Ready}}}_{\text{Hon}} \underbrace{\mathbf{t}_{\text{AOn}}}_{\text{Hon}} \underbrace{\mathbf{t}_{\text{AOn}}}_{\text{Hon}}$
	VA_In
	$\mathbf{IMxPRst} \qquad \qquad$
	IBMD _{Ready}
	Figure 147 VA_In Timing Measurements
11 5 System Management G	
TT.S OTSTEM MANAGEMENT C	
	The system management group consists of the InfiniBand Management Link IB-ML (IMxClk and IMxDat), the management interrupt (IMxInt_L), the module presence and reset (IMxPRst)), and the power request (IMxPReq_L) signals.
11.5.1 IMxClк, IMxDat	
	The IMxClk and IMxDat signals provide a serial management interface which supports communication between an IB module and a chassis.
11.5.1.1 GENERAL RULES	
	C11-19: The IMxDat and IMxCIk signals shall conform to the DC parameters defined in <u>Table 113 on page 453</u> and the AC parameters <u>Table 114</u> on page 455.
	C11-20: IB-ML devices on modules that are powered down shall provide a mechanism to isolate the device from the management link. The load presented by the isolated devices shall be less than I _{Isolate} .
11.5.1.2 MODULE RULES	
	C11-21: A module shall not present a capacitive load on the IB-ML greater than C _{IBML_Module} . The IB Module shall not present a current leakage load on the IB-ML greater than I _{IBML_Module} .

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	C11-22: A module shall provide pull-ups to 3.3V on the xDat signals. The pull-up value shall be designed for th on the module and chassis.	IMxClk and IM- e maximum load	1 2 3
	Please see <u>Annex A2: IB-ML Design Guidelines on</u> sign guidelines in selecting an appropriate value.	page 767 for de-	4 5
11.5.1.3 CHASSIS RULES			6
	C11-23: The chassis shall not present a capacitive load greater than C _{IBML_Chassis} . The chassis shall not present a load on the IB-ML greater than I _{IBML_Chassis} .	d on the IB-ML a current leakage	7 8 9 10
	C11-24: The chassis shall provide pull-ups to 3.3V on th xDat signals. The pull-up value shall be designed for th on the module and chassis.	e IMxCIk and IM- e maximum load	11 12 13
	Please see <u>Annex A2: IB-ML Design Guidelines on</u> sign guidelines in selecting an appropriate value.	page 767 for de-	14 15 16
11.5.2 IMxInt_L			17
	The Management Interrupt (IMxInt_L) signal originates Module to indicate that an attention condition has arisen CME. See <u>Section 13.3.2.8</u> , "IMxInt L," on page 515 for	from the IB to a present an operational	18 19 20
	description.		21
	C11-25: A Module shall provide the IMxInt_L signal on implemented IB-ML.	all ports with an	22 23
11 5 2 1 GENERAL RULES			24
THUS 2.1 OLNERAL ROLLS	C11.26: The IMVINT I signal shall conform to the DC pa	ramators defined	26
	in <u>Table 113 on page 453</u> and the AC parameters defined page 456.	d in <u>Table 115 on</u>	27 28
			29
11.5.3 IMxPRst			30
	The IMxPRst signal is bidirectional and provides the cha	assis with the	31
	to perform a reset of the IB module, if necessary.	aule in a slot and	32 33
11.5.3.1 PRESENCE DETECT			34
	The Presence function is achieved through the Repure a	nd Reeds resis-	35
	tors. The values chosen would have R _{PRdn} being weak	er than R_{PRup} so	37
	that an inserted module would have IMxPRst being pulle high level. An empty slot would have Rppdp pulling IMxI	ed to an asserted PRst to VA Ret	38
	which represents the deasserted level. A chassis would	monitor the level	39 40
	(as defined by VII and VIII in <u>Table 113 IMx* DC Specific</u> <u>453</u>) to determine module presence.	ations on page	41
			42

Implementation Note

Typically available 10% resisters of $2.2K\Omega$ for R_{PRup} and $3.0K\Omega$ for R_{PRdn} are recommended for use on the **IMxPRst** signal.

Upon auxiliary power being available to a module, an amount of time is necessary to allow the functions implemented on auxiliary power to achieve the reset condition. Thus, upon detection of a module in a slot, the chassis needs to wait before attempting operations on IB-ML to that slot (See t_{AOn} in Table 112 on page 447).

11.5.3.2 RESET

The Reset function is provided to allow a chassis to effect a slot reset, including the functions implemented on the Auxiliary power domain, without power cycling the **VA_In** inputs. This reset is to place the module into the state that would have been achieved by a cold power on of both auxiliary and primary power.

Referring to Figure 148 IMxPRst Termination on page 451, the reset indication is achieved by the module monitoring the level of the **IMxPRst** signal for a low level. Under normal operations, the **IMxPRst** is held at a high level by the strong R_{PRup} resistor. The chassis can implement an ac-

	tive override mechanism to pull the IMxPRst signal low to achieve the				
	Backp	lane	Module	2	
	VA In			3	
	<u> </u>			4	
				5	
			RPRup	6	
				/ 0	
	IMxPRst			0 Q	
	Slot_Reset		LocalReset	10	
		KPRrdn		12	
	KPKrst			14	
	VA Ret			16	
	VA_Ket			17	
		Backplane Connecto	or	18	
	Note: RPRst	is implementation depen	ident.	19	
	Figure 14	8 IMxPRst Term	ination	20	
11.5.3.3 GENERAL RULES				21	
	C11-27: The IMxPRst signal sh in <u>Table 113 on page 453</u> and th page 456.	all conform to the ne AC parameters	DC parameters defined defined in <u>Table 115 on</u>	22 23 24	
				25	
TI.J.J.4 WODULE RULES	C11-28: A module shall implem mented backplane ports.	nent the IMxPRst	signal on all imple-	20 27 28 29	
	Architectural Note			30	
	This provides a means for the fully inserted.	chassis to determ	nine that the module is	31 32 33	
	C11-29: The module shall prov VA_In reaching V _{Aux} (min) or ot	ide for an initial re her means.	eset condition upon	34 35 36	
	C11-30: Upon release of the re- IB-ML agent state machines, re values, and perform any module within <i>ModulePowerInfo.InitTim</i>	set condition, the turn the MME fac e specific function ne. (See <u>Table 156</u>	module shall clear the ilities their "default" is that would take place <u>5 on page 622</u>).	37 38 39 40 41	

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11.5.3.5 CHASSIS RULES		4	4
	o11-6: The chassis may monitor the level of IMxPRs	t to determine	1 2
	module presence from a backplane port.	3	3
	o11-7: If the chassis uses IB-ML, the chassis shall wa	ait for the time spec- 4	1
	ified by t _{AOn} (See <u>Table 112 on page 447</u>) before attem	pting operations on 5	5
	IB-ML to that slot.	6) 7
	o11-8: The chassis may perform a reset through an ad	ctive override mech- 8	3
	anism to pull the IMxPRst signal low to achieve the r	eset. If the override g)
	minimum of t_{Reset} as defined in <u>Table 115</u> .)	1 be deasserted a	10 11
	o11-9. The chassis may perform a reset prior to mod	lule operation 1	12
		1	13
11.5.4 IMxPREQ_L		1	4
	The IMxPReq_L pin signals the chassis that the IB M	lodule is requesting 1	15 16
		1	10 17
	This signal is controlled by the Baseboard Manager a	and WakeRequest-	18
	Event.	1	19
11.5.4.1 GENERAL RULES		2	20
	C11-31: The IMxPReq_L signal shall conform to the	DC parameters de-	21 22
	fined in <u>Table 113 on page 453</u> and the AC paramete	rs defined in <u>Table</u> 2	23
		2	24
11.5.4.2 MODULE RULES		2	25
	o11-10: If the module supports power management a	as specified in 2	26 27
	IMxPReq_L signal on each backplane port.	2 2 2 2 2	-1 28
		2	29
11.5.4.3 CHASSIS RULES	e11 11 . The change may support the respection of the	f nower aubayatama	30
	with the IMxPReq_L signal as outlined in <u>Chapter 14</u> :	OS Power Manage-	31
	ment.	3	32 33
11.5.5 IMX* SIGNAL PARAMETI	ERS	3	34
	This section defines the electrical parameters for the	System Manage- 3	35
	ment group.	3	36 27
	If parameters apply to all signals beginning with "IMx	् , they are referred 3	יג 38
	to as "IMx*"; the "*" indicates a generic placeholder. I	f parameters apply 3	39
	to specific signals, these are named explicitly.	4	10
		4	11
		4	12

11.5.5.1 IMx* DC SPECIFICATIONS

Symbol	Parameter	Minimum	Maximum	Units	Comments
Vil	Input Low Voltage	-0.5	.8V	V	
Vih	Input High Voltage	2.1	3.63	V	
Vol	Output Low Voltage		0.4	V	at Ipullup Max.
Voh	Output High Voltage	2.2	3.63	V	
Ipullup	Pullup Current		4.0 ^a	mA	
C _{IBML_Module}	Module Segment Capacitance		200	pF	
C _{IBML_Chassis}	Chassis Segment Capacitance		100	pF	
I _{IBML_Module}	Module Segment Leakage Cur- rent		+/- 80	μA	
I _{IBML_Chassis}	Chassis Segment Leakage Cur- rent		+/- 40	μA	
I _{Isloate}	Isolation Current		+/- 10	μA	
R _{PRup} b	Pull-up Termination	1.870	2.500	KΩ	
R _{PRdn} ^b	Pull-down Termination	2.625	3.630	KΩ	
V _{PU}	IBML Termination Voltage	3.036	3.63	V	Nominal 3.3V

a. The maximum value includes both the current through the pull-up resistor and current from all bus agents. In this context the parameter lpullup is equivalent to IoI. The minimum value is implementation dependant

b. The values specified for this parameter do not include all tolerances of implemented components.

11.5.5.2 IMxDat, IMxCLK AC SPECIFICATIONS

Figure 149shows the electrical timing parameters for the IMxDat and IM-30xClk signals. The specification values for these parameters are found in
Table 114.3132

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Figure 149 IMxDat, IMxClk Timing Measurements

Symbol	Parameter	Minimum	Maximum	Units	Comments
f _{IBML}	IB-ML Operating Frequency		100	KHz	
IBML _{TP}	IB-ML Throughput	10		KHz	
t _{FALL}	Clock/Data Fall Time		300	ns	See note ^a
t _{RISE}	Clock/Data Rise Time		1000	ns	See note ^a
t _{OF}	Output fall time from V _{IH} min to V _{IL} max with a bus capacitance from 10 pF to 400 pF		250	ns	See note ^b
t _{BUF}	Bus free time between Stop and Start Condition	4.7		μs	See Figure 149 on page 454
t _{HD:STA}	Hold time after (Repeated) Start Condition. After this period, the first clock is generated.	4.0		μs	See Figure 149 on page 454
t _{SU:STA}	Repeated Start Condition setup time	4.7		μs	See Figure 149 on page 454
t _{SU:STO}	Stop Condition setup time	4.0		μs	See Figure 149 on page 454
t _{HD:DAT}	Data hold time	300		ns	See Figure 149 on page 454
t _{SU:DAT}	Data setup time	250		ns	See Figure 149 on page 454
t _{LOW}	Clock low period	4.7		μs	
t _{HIGH}	Clock high period	4.0	50	μs	See note ^c

Table 114 IMxDat, IMxClk AC Timing Specifications

a. Rise and fall time are defined as follows: $T_{RISE} = (V_{IL}MAX - 0.15)$ to $(V_{IH}MIN + 0.15)$, $t_{FALL} = 0.9V_{PU}NOM$ to $(V_{IL}MAX - 0.15)$

b. The maximum t_{FALL} for the IMxCIk and IMxDat lines specified is longer than the specified maximum t_{OF} for the output stages. This allows series protection resistors (Rs) to be connected between the IMxCIk/IMxDat pins and the IMxCIk/IMxDat lines without exceeding the maximum specified t_{FALL} .

c. t_{HIGH} MAX provides a simple guaranteed method for devices to detect bus idle conditions.

11.5.5.3 IMXINT_L, IMXPRST, IMXPREQ_L AC SPECIFICATIONS

Table 115 IMxInt_L, IMxPRst, IMxPReq_L AC Timing Specifications

	= ,	,		5		4
Symbol	Parameter	Minimum	Maximum	Units	Comments	5
t _{IMxFALL}	Fall Time		300	ns	See note ^a	— 6 7
t _{IMxRISE}	Rise Time		1000	ns	See note ^a	8
t _{Reset}	IMxPRst pulse width	1		ms		9

a. Rise and fall time for the **IMxPRst** signal is defined as follows: $t_{RISE} = V_{IL}MAX$ to $V_{IH}MIN$, $t_{FALL} = V_{IH}MIN$ to $V_{IL}MAX$. Rise and fall time for the **IMxInt and IMxPReq_L** signals are defined as follows: $t_{RISE} = V_{OL}MAX$ to $V_{OH}MIN$, $t_{FALL} = V_{OH}MIN$ to $V_{IL}MAX$. $V_{IL}MAX$.



Figure 150 IMxPRst, IMxInt, IMxPReq_L Timing Measurements



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CHAPTER 12: POWER / HOT PLUG

12.1 INTRODUCTION

This chapter defines the power use and control of the module form factors defined by this specification. Where necessary, backplane requirements are stated to produce module to chassis interoperability as intended by the architecture.

The power control of non-IB devices that are sub-ordinate to xCAs (e.g. I/O controllers) are outside of the scope of this specification.

Due to the point-to-point nature of the InfiniBand link, the issues with data signal isolation that exist with multi-dropped bus topologies are not present. However, power needs to be controlled so as to not damage a module due to high in-rush currents.

12.1.1 LOCAL DC-DC POWER CONVERTER(S)

The DC-DC power converter(s) on the IB adapter module supply local power to on-board devices at their required voltage(s). This allows the IB standard to be independent of the unique voltages required by any particular adapter.

12.1.2 POWER CLASSES

Two Power Classes are defined for InfiniBand modules:

- Class I implementations utilize converters that may or may not isolate VB_Ret from logic ground on the module.
- Class II implementations ONLY utilize converters that isolate
 VB_Ret from logic ground on the module.

See <u>Section 12.4, "Module Power Rules," on page 467</u> for the parametric definition of isolation for Class II.

The local DC-DC power converter(s) incorporated on an IB adapter may 35 be implemented under either of the two power classes. 36

12.1.3 POWER TOPOLOGIES

InfiniBand adapters that draw from bulk power have a representative topology as depicted in <u>Figure 152 Class I Power Topology on page 458</u> and <u>Figure 153 Class II Power Topology on page 459</u>. 40 41 42





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12.1.4 POWER PORTS

4 Power is supplied from the backplane within a chassis to the module 5 through the "Bulk Power Group" and "Auxiliary Power Group" contacts. These groups collectively define a "Power Port". Figure 154: Module Bulk 6 Power Ports (Logical) depicts the relationship of Power Port to physical 7 modules. 8



12.2 MODULE POWER PORT AND CONSUMPTION RULES

C12-1: All modules shall limit their power consumption to the values defined in <u>Table 116</u> for their respective form factor.

C12-2: All modules shall have at least one power port located at Primary Port 1 as defined by Figure 154 and Section 12.5, "Chassis Power Rules," on page 470. 42 **o12-1:** Tall or Wide modules **may** have additional power ports as defined in <u>Table 116</u> for the respective form factor.

Table 116 Module Form Factor Power Summary						
Module Form Factor	Power Ports	Maximum Bulk Power Consumed	Maximum Auxiliary Power Consumed	Maximum Thermal Dissipation ^{ab}		
Standard, Single Wide	1	25W	1.2W	25W		
Standard, Double Wide	1or 2	50W	1.2W	50W		
Tall, Single Wide	1 or 2	50W	2.4W	50W		
Tall, Double Wide	1, 2, 3, or 4	100W	2.4W	100W		

a. Dissipation is integrated over a 5 second interval

b. The module must ensure that the dissipated power does not exceed the Dissipation value for the form factor regardless of input power sources.

12.3 MODULE / CHASSIS COMPATIBILITY

This section defines the compatibility of the defined chassis and module types.

In this section, the terms "Redundancy" or "Redundant" refer to the design technique where power is drawn from multiple power ports, if available, in such a manner that if a power port fails, the full module power may be drawn through other power ports. Conversely, "Not Redundant" indicates that additional power ports are not available to take on the full load; this could be due to the lack of additional physical power ports (i.e. a standard module) or by design (i.e. a 100W double wide tall module).

12.3.1 STANDARD MODULE, STANDARD CHASSIS

The compatibility of Standard InfiniBand modules within a Standard Chassis from a power view is defined in <u>Table 117</u>.

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Table 117 Standard Module, Standard Chassis Slot Power

Sta	andard Typ	Mod be	ule		Backplane Slot Connections ^b	
Width ^c	Power ^d	Boards	Redundancy ^e	Slot ^a	Power Port 1, 25W	Power Port 1, 50W
S	25	1	Ν	Ρ	25W	25W
D	25	1	N	Ρ	25W	25W
D	25	I	IN	А	No Connection	No Connection
	25	0	×	Ρ	25W	25W
D	25	2	ř	А	25W(R)	25W(R)
	50	1	Ν	Ρ	Not Supported	50W
D	50	I	IN	А	No Connection	No Connection
				Р	Not Supported	50W
D	50	2	N	Af	No Connection for Power	No Connection for Power
D	50	2	Ν	Ρ	25W	25W
U	50	2	IN	A	25W	25W
D	50	2	v	Ρ	Not Supported	50W
	50	2	T	А	Not Supported	50W(R)

a. "P" - Primary slot; "A" - Adjacent slot to the right as viewed from the I/O Plate. Adjacent is applicable for Double Wide modules only.

b. A port must be enabled with **VBxEn_L** being asserted (low). "25W" at a Power Port indicates that **VBxCap** is driven low by the backplane; "50W" at a Power Port indicates that **VBxCap** is pulled high by the backplane.

- c. "S" Single wide; "D" Double wide.
- d. Power value stated is the maximum allowed.

e. Indicates whether the particular module supports redundant power ports. "N" - No; "Y" - Yes. If "Y", one or more power ports are designated as "redundant" with the form "xxW(R)" where "xx" is the maximum power drawn.

f. While this module type has 2 boards and may contact the backplane for attachment of links, it is not contacting the power contacts to avoid the need for multiple converters. Rather, the module is pulling all of its power from the Primary slot.

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1	9
2	0
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2	7
2	2
2	0
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Recommendation to Module Designer:

While it is possible for a Standard Double Wide module to draw 50W from two adjacent 25W ports, it is recommended that the module draw its power from only the primary port. (See recommendation below.)

Recommendation to System Designer

The chassis may provide 50W to each port unconditionally.

If the power delivery requirement for a slot is exceeded (25W for this case), the chassis may disable power to the adjacent port to the right. This is because only a double wide standard module can draw more than 25W (via **VBxCap**) and it inherently occupies the adjacent slot to the right.

12.3.2 TALL MODULE, TALL CHASSIS

The compatibility of Tall InfiniBand modules within a Tall Chassis from a power view is defined in <u>Table 118</u>.

				Tak		dule, Tall Chass	is Slot Fower		
Tall Module Type			pe		Backplane Slot Connections ^b				
Width ^c	Power ^d	Boards ^e	Redundancy ^f	Slot ^a	Power Port 1, 25W	Power Port 1, 50W	Power Port 2, 25W	Power Port 2, 50W	
S	25	1	Ν	Ρ	25W	25W	No Connection	No Connection	
S	25	1	Υ	Ρ	25W	25W	25W(R)	25W(R)	
S	50	1	Ν	Ρ	25W (Requires Port 2)	50W	25W	Don't Care	
S	50	1	Υ	Ρ	Not Supported	50W	Not Supported	50W(R)	
D	D 50 1	1	N	Ρ	25W (Requires Port 2)	50W	25W	Don't Care	
			А	No Connection	No Connection	No Connection	No Connection		
				Ρ	25W	50W	25W	Don't Care	
D 50	2	N	Ag	No Connection for Power	No Connection for Power	No Connection for Power	No Connection for Power		
D	D 50	2	N	Ρ	25W	25W	No Connection	Don't Care	
D 50	2	IN	А	25W	25W	No Connection	No Connection		
D	D 50	2	X	Ρ	25W	50W	25W(R)	Don't Care	
D 50	2	T	А	25W	50W(R)	25W (R)	Don't Care		
D 100	1	N	Ρ	Not Supported	50W	Not Supported	50W		
			A	No Connection	No Connection	No Connection	No Connection		
P	100	2	N	Ρ	25W	50W	25W	Don't Care	
100	100	2		A	25W	50W	25W	No Connection	
P		_	V	Ρ	Not Supported	50W	Not Supported	50W(R)	
100	2	r	А	Not Supported	50W	Not Supported	50W(R)		

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a. "P" - Primary slot; "A" - Adjacent slot to the right as viewed from the I/O Plate. Adjacent is applicable for Double Wide modules only.

b. A port must be enabled with VBxEn_L being asserted (low). "25W" at a Power Port indicates that VBxCap is driven low by the backplane; "50W" at a Power Port indicates that **VBxCap** is pulled high by the backplane.

c. "S" - Single wide; "D" - Double wide.

d. Power value stated is the maximum allowed.

e. Indicates the number of PCBs implemented within the form factor that connect to the backplane.

f. Indicates whether the particular module supports redundant power ports. "N" - No; "Y" - Yes. If "Y", one or more power ports are designated as "redundant" with the form "xxW(R)" where "xx" is the maximum power drawn. g. While this module type has 2 boards and may contact the backplane for attachment of links, it is not contacting the power contacts to avoid the need for multiple converters. Rather, the module is pulling all of its power from the Primary slot.

Recommendation to Module Designer:

While it is possible for a Tall Double Wide module to draw 100W from two adjacent 50W ports, it is recommended that the module draw its power from only the primary slot's Port 1 and Port 2. (See recommendation below.)

Recommendation to System Designer

The chassis may provide 50W to each port unconditionally.

Alternatively, if the power delivery required for a slot is exceeded (50W for this case of a tall module), the chassis may disable power to the right adjacent slot's Port 1 and Port 2. This is because only a double wide tall module can draw more than 50W (via **VBxCap**(s)) and it inherently occupies the adjacent slot to the right.

12.3.3 STANDARD CHASSIS, TALL CHASSIS

The compatibility of Standard InfiniBand modules within a Tall Chassis from a power view is defined in <u>Table 119</u>.

Standard Module Type			Backplane Slot Connections ^b														
Width ^c	Power ^d	Boards ^e	Redundancy ^f	Slot ^a	Power Port 1, 25W	Power Port 1, 50W	Power Port 2, 25W	Power Port 2, 50W									
S	25	1	Ν	Ρ	25W	25W	No Connection	No Connection									
D	D 25 1	1	N	Р	25W	25W	No Connection	No Connection									
D		N	А	No Connection	No Connection	No Connection	No Connection										
D	25 2	2		V		v	V	V	Ρ	25W	25W	No Connection	No Connection				
D 25 2	Ť	А	25W(R)	25W(R)	No Connection	No Connection											
		1	4	1	1	Ν	Ρ	Not Supported	50W	No Connection	No Connection						
D 50 1	N	А	No Connection	No Connection	No Connection	No Connection											
_		2	2	2	2	2	2						Ρ	Not Supported	50W	No Connection	No Connection
D 50 2	2							N	2 N	Ag	No Connection for Power	No Connection for Power	No Connection	No Connection			
			0			Ρ	25W	25W	No Connection	No Connection							
D 50 2	2	IN	А	25W	25W	No Connection	No Connection										
D	D 50	2	v	Ρ	Not Supported	50W	No Connection	No Connection									
00 0	2		А	Not Supported	50W(R)	No Connection	No Connection										

Table 119 Standard Module, Tall Chassis Slot Power

a. "P" - Primary slot; "A" - Adjacent slot to the right as viewed from the I/O Plate. Adjacent is applicable for Double Wide modules only.

b. A port must be enabled with **VBxEn_L** being asserted (low). "25W" at a Power Port indicates that **VBxCap** is driven low by the backplane; "50W" at a Power Port indicates that **VBxCap** is pulled high by the backplane.

c. "S" - Single wide; "D" - Double wide.

d. Power value stated is the maximum allowed.

e. Indicates the number of PCBs implemented within the form factor that connect to the backplane.

f. Indicates whether the particular module supports redundant power ports. "N" - No; "Y" - Yes. If "Y", one or more power ports are designated as "redundant" with the form "xxW(R)" where "xx" is the maximum power drawn. g. While this module type has 2 boards and may contact the backplane for attachment of links, it is not contacting the power contacts to avoid the need for multiple converters. Rather, the module is pulling all of its power from the Primary slot.



This section defines power rules that apply to all modules defined by this 38 specification. 39

C12-3: A module that draws power from **VB_In shall** supply a bulk DC-DC converter.

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C12-4: The module **shall** disable its port-specific DC-DC converter(s) upon the sensing of a deasserted level on **VBxEn_L** on that port.

C12-5: The module shall not draw more than I_{BLeakage} current while VBxEn_L is deasserted. Upon VBxEn_L going from asserted to deasserted, the module shall reduce its current draw to I_{BLeakage} or less within the time specified by t_{BOff}.

Note: Chassis are not required to provide I_{BLeakage} current while **VBxEn_L** is deasserted.

C12-6: The module power converter **shall** provide input fault current limiting³ and set its threshold at less than 200% of I_{BMax} . The current limiting **shall** be activated within 20µs of crossing the current limit threshold.

Implementation Note

The current limit implementation is intended to be located in the hotplug circuit, where the Hot-plug FET is turned off or controlled for a over-current fault. Thus, protection for over current faults or shorts on the regulator's output, internal to the regulator and of the Secondary Rail (after the hot plug FET) are covered. Examples of acceptable over current protection methods are:

- Fold Back Over current limit is reached and FET is controlled to fold back the allowed current
- Hiccup A failure mode where the power sequencer supplies power to the voltage converter, current limiting occurs, and power is removed. This sequence can continuously repeat.
- Latch off Over-current cause hot plug FET to turn off, and an on/off command is required to reset

C12-7: The module shall set Interrupt-

ClearStatus.Power_Converter_Fault upon the detected violation of the IBMax parameter or any condition that causes the DC-DC converter to be off.

C12-8: The module **shall** provide over voltage protection sufficient to not $_{\text{produce a voltage greater than } V_{\text{RHP}}$ defined in <u>Table 20 Receiver Char</u>- $_{37}$

3. The faults for which the fault current limiting is intended are shorts to ground
on the Secondary Rail, within the DC-DC converter, or for V_{Out}. (Refer to Figure
152 on page 458 for terminology references). Shorting faults across any active
current limiting components (series FETs for example) are not considered
covered by this mechanism.384142
acteristics for 2.5 Gb/s on page 192 on the **IBsxIw** or **IBsxOw** signals, even in the presence of "let-through" converter fault.

Implementation Note

Many ASIC driver and receiver designs intrinsically supply clamping circuitry (typically diodes) to prevent signal levels from exceeding the input power supply specifications of that ASIC. Many of these clamping circuits can allow fault generated over-voltage conditions to pass on to the external (off-ASIC) portion of the driver or receiver and cause a violation of far end parameters (V_{RHP} specifically). Designers should take this possibility into account when selecting components and designing over-voltage protection.

C12-9: The module **shall** set the *ModulePowerInfo.PowerClass* field to reflect the implemented Power Class.

o12-2: If the *ModulePowerInfo.PowerClass* field indicates Class II, the module **shall** provide a minimum isolation of 2.0 M Ω DC resistance @ 500V of isolation between **VB_Ret** and **Varlet** and a minimum isolation of 2.0 M Ω DC resistance @ 500V between **VB_Ret** and **IB_Sh_Ret**.

Note to Module Implementers

A Class II chassis is not required to permit Class I adapters to power on. A Class I chassis must permit Class II adapters to power on if their power requirements do not exceed the chassis/slot limit.

C12-10: A module **shall** support "Hot Add" functionality as defined in <u>Section 12.6.1 on page 471</u>.

C12-11: A module **shall** support "Surprise Hot Removal" functionality as defined in <u>Section 12.6.2 on page 473</u>.

C12-12: A module shall draw auxiliary power only from the VA_In contact 3 of Primary Port 1. 3

C12-13: The module **shall** set the *ModulePowerInfo.RedundantPower* field to reflect implemented redundant power port connections.

12.4.2 MULTIPLE POWER PORTS

If a module contains more than one power port, the rules of this subsection apply.

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o12-3: If a module contains more than one power port, it **shall not** connect the **VB_In** signals from multiple power ports together.

Implementation Note

The above non-bridging requirement implies that when power multiple connections are made (using multiple power ports), a DC-DC converter per port is required.

12.4.3 TALL DOUBLE WIDE

o12-4: A Tall Double Wide module **may** consume up to 2.4W only from **VA_In** from Primary Port 1.

12.5 CHASSIS POWER RULES

This section states the chassis power requirements for supporting the modules defined by this specification.

For vertical module orientations, the "primary" slot is defined to be the leftmost slot of an adjacent pair as viewed from the I/O plate. For horizontal module orientations, the "primary" slot is defined to be the lower-most slot of an adjacent pair as viewed from the I/O plate. Refer to <u>Section 9.1.3.1.</u> <u>"Slot Designations," on page 360</u>.

12.5.1 GENERAL

This section defines the power rules for a chassis that accepts a module defined by this specification. 26

C12-14: An Unmanaged standard height chassis shall be capable of supplying a minimum of 25W on VB_In at any existent port. 29

o12-5: An Actively Managed standard chassis **may** choose to manage the power distribution according to *ModulePowerInfo* rather than providing 25W to all existent ports simultaneously.

C12-15: The chassis **shall** provide for the assertion of the **VBxEn_L** signal per power port for which it intends to supply power.

C12-16: The chassis power supply(s) **shall** be capable of supplying a minimum of 1.2W on **VA_In** at every slot simultaneously.

o12-6: If a chassis accepts Tall modules, it **shall** provide distribution and any protection mechanisms that allow a minimum of 2.4W to be delivered to **VA_In** at any Port 1.

Implementation Note

The module does not inherently provide 240VA protection. This is left to the system implementation.

Implementation Note

High Availability chassis will need to account for a dead short between any contacts on a module prior protection circuitry.

12.6 HOT PLUG

12.6.1 HOT ADD

"Hot Add" is defined as the insertion of an InfiniBand module into a backplane that has both V_{Bulk} and V_{Aux} present. The module powers up and initiates a training sequence.

The InfiniBand backplane connector defines four (4) mating contact levels and that are referred to as Level 1, Level 2, Level 3 and Level 4. See <u>Chapter 10: Backplane Connector Specification</u>. The contact sequencing that takes place upon module insertion, referred to a "mate order", is de-

InfiniBand TM Architecture Release 1.2 VOLUME 2 - PHYSICAL SPECIFICATIONS	Power / Hot Plug	3	October, 2004 FINAL
pio de	cted in <u>Figure 155: Module</u> escribed.	e Insertion Contact Sequ	<u>lence</u> and then further 1
	Module I	Direction	3 4 5
			ESD 6 7
	VB_Ret, VA_Ret	Grounds	Level 1 9
	VB_In, VA_In	Bulk, Aux Pow	Level 2 11 /er 12
IM	xClk, IMxDat, IMxInt_L, VBxPFW_L, IM	VBxCap, xPReq_L Aux Sigr	Level 3 13 14 nals 15
IBsxI	w(n:0), IBsxOw(n:0), IB_	_ Sh_Ret High Speed Sig	High Speed 17 gnals 19
	VBxEn_	L, IMxPRst Enable, Pres	Level 4 20 ence 22
	Legend:		23
	Module Enclosu	Secondary Side F re Connector C	Primary Side 25 Connector 26
	Figure 155 Mod	ule Insertion Contact	Sequence 28
1)	ESD: Upon insertion of springs provide a path f	the module in the chase or ESD from the module	29 sis slot, the EMI 30 e to the chassis. 31
2)	Level 1 Mate: VB_Ret, current return contacts	VA_Ret and IB_Sh_Re and establish reference	t mate to provide32voltage levels.33
3)	Level 2 Mate: Power co	ontacts VB_In and VA_I	n mate. 34
	The bulk domain does r pulled high (deasserted VBxEn L Termination o	not begin ramping due t) through pull-up termin <u>on page 438</u> for details.	o VBxEn_L being ation. See <u>Figure 142</u> 37 37
	The auxiliary domain be C _{ABulk} .	egins ramping based on	input capacitance 38
4)	<u>Level 3 Mate</u> : The IMxI VBxPFW_L, VBxCap o	Dat, IMxClk, IMxInt_L, I contacts mate to allow fo	MxPReq_L, or IB-ML functionality.

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	High Speed Mate: The high speed li IBsxOw, mate.	nk interface contacts, IBsxIw and
	The timing relationship between Ler is connector dependent and not spe of Hot Add, this relationship is unim High Speed Mate to Level 4 Mate; th nector (See <u>Chapter 10: Backplane</u> <u>409</u>).	vel 3 Mate and High Speed Mate cified. However, for the operability portant. What is important is the his is strictly controlled by the con- <u>Connector Specification on page</u>
	Level 4 Mate: The VBxEn_L contact enablement. IMxPRst mates to sign nection is now present on this IB po	ct mates to allow for bulk power nal the backplane that a con- ort.
	For a Unmanaged Chassis, the VB the on-board sequencer to be enab	xEn_L must be asserted to allow led.
	For a Managed Chassis, the VBxE backplane to prevent the enablement the componentry implemented on a ements to make whatever determine VBxEn_L . The sequencer, seeing to VBulk (Min), and having been control <u>Enable</u>), will turn on the input to the the module logic to be powered from	n_L may be deasserted by the nt of the sequencer. A CME, using uxiliary power, may read VPD el- ation appropriate before asserting hat VB_In has reached enabled (VBxEn_L , <u>Local Power</u> DC-DC converter. This allows for m the output of the converter.
12.6.2 SURPRISE HOT REMOVAL		
	urprise Hot Removal" is defined as the m a backplane that has both V_{Bulk ar} aced in a quiescent state.	e removal of an InfiniBand module nd V _{Aux} present without first being
	e InfiniBand backplane connector def d are referred to as Level 1, Level 2, : Backplane Connector Specification	ines four (4) mating contact levels Level 3 and Level 4. See <u>Chapter</u>

InfiniBand TM Architecture Release 1.2 Volume 2 - Physical Specifications	Power / Hot	Plug		October, 2004 FINAL
	The contact sequencing to a "break order", is dep <u>quence</u> and then furthe	g that take picted in <u>F</u> r describe	s place upon module <u>igure 156: Module Re</u> d.	removal, referred moval Contact Se-
	Modu	ıle Directi	on	
				ESD
	VB_Ret, VA_Ret		Crounda	Level 1
	VB_In, VA_In			Level 2
I	IMxClk, IMxDat, IMxInt	_L, VBxC	ap,	Level 3
	VBXPFW_L,	, IMXPRed	Aux Signals	1
IBs	sxlw(n:0), IBsxOw(n:0)	, IB_Sh_R	Ret High Speed Signal	High Speed
	VBx	En_L, IM>	PRst	Level 4
			Enable, Presenc	e
	Legend:			
	Moc Enc	losure	Connector Coni	ary Side nector
	Figure 156 M	odule Rei	moval Contact Sequ	ence
	1) <u>Level 4 Break</u> : The I break from a power down and have the	Bulk Powe view. The current dr	er control signal, VBxB e module must initiate aw below I _{BLeakage} w	En_L, is the first to e converter shut- vithin t _{BOff} .
	2) <u>Level 3 Break</u> : The VBxPFW_L, VBxC	IMxDat, II ap contac	MxClk, IMxInt_L, IMx ts break to disconnec	t IB-ML.
	<u>High Speed Break:</u> Power to the logic fi moved due to VBxE	The IBsxI unction dr E n_L bein	w and IBsxOw conta iving the IBsxOw sign g deasserted.	cts disengage. nals must be re-
	The timing relations is connector depend of Surprise Hot Ren	hip betwee dent and u noval, this	en Level 3 Break and inspecified. However, relationship is unimp	High Speed Break for the operability ortant. What is im-

portant is the Level 4 Break to High Speed Break timing relationship 1 which is strictly controlled by the connector. 2 Level 2 Break: Power contacts VB_In and VA_In break. The current 3 being below IBLeakage on VB_In prevents contact damage upon the 4 break. VA_In can break at full current (IAMax) without contact 5 damage. 6 4) Level 1 Break: Return contacts VB_Ret, VA_Ret and IB_Sh_Ret 7 break. 8 ESD: This allows for residual charge to be dissipated. 9 12.6.3 GRACEFUL HOT REMOVAL 10 11 "Graceful Hot Removal" is the removal of an adapter module that has first been placed in a quiescent state. V_{Bulk} may or may not be on. 12 13 For the case that **V_{Bulk}** is still on, the Graceful Hot Removal is dependent 14 on the Surprise Hot Removal functionality described in Section 12.6.2 and 15 required in Section 12.4 on page 467. 16 17 The features required for the achievement of the guiescent state are de-18 scribed in Section 13.3.2.4, "Graceful Hot Removal," on page 503. 19 20 **12.7 POWER MANAGEMENT WAKE-UP** 21 12.7.1 BEACON SEQUENCE - CHASSIS POWER ON 22 This sequence assumes that the module has been inserted into a chassis 23 and that the chassis is in a "Full On" condition. (both Auxiliary and Bulk 24 Power are available to the slot). Additionally, it is assumed that the module 25 was powered down by setting the PowerDown bit, which is derived from the *ModulePMControl.PMState* field; this would deassert Local Power 26 Enable to the sequencer. 27 28 A beaconing sequence is detected. 29 30 PowerDown is reset. This causes Local Power Enable to assert as-31 suming the absence of other environmental faults. 32 Additionally, the **IMxPReq_L** is asserted to an existent CME or power 33 subsystem control element. 34 35 The sequencer is enabled (VBxEn L is asserted due to assumed 36 proper mating with backplane and **VB** In being at assumed appro-37 priate level). 38 The sequencer, seeing that VB_In has reached V_{Bulk}(Min), and 39 having been control enabled (VBxEn_L, Local Power Enable), will 40 turn on the input to the DC-DC converter. This allows for the module 41 logic to be powered from the output of the converter.

Power / Hot Plug

12.7.2 BEACON SEQUENCE - CHASSIS POWER OFF

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Thi and Po the rive <u>Lo</u>	is sequence assumes that the module has been inserted into a chassis d that the chassis is in a "Off but Power Available" condition. (Auxiliary wer is on, Bulk Power is off to the slot). Additionally, it is assumed that e module was powered down by setting a <u>PowerDown</u> bit, which is de- ed from the ModulePMControl.PMState field; this would deassert cal Power Enable to the sequencer.	2 3 4 5 6
1)	A beaconing sequence is detected under Auxiliary Power.	7 8
2)	<u>PowerDown</u> is reset. This causes <u>Local Power Enable</u> to assert as- suming the absence of other environmental faults.	9 10
	Additionally, the IMxPReq_L is asserted to the backplane.	11
	The sequencer is enabled (VBxEn_L is asserted due to assumed proper mating with backplane). However, VB_In is off due to the chassis being "Off but Power Available". The sequencer will monitor the availability of voltage on VB_In to enable the converter(s).	12 13 14 15
3)	The chassis, being in the "Off but Power Available" condition, sees the assertion of IMxPReq_L . This indication allows the chassis to enable the Bulk Power.	16 17 18
	The means by which the chassis was put into the "Off but Power Avail- able" state are not specified; it is outside the scope of the InfiniBand specification. It is likely that a chassis which implements this type of functionality will have a CME of some form.	19 20 21 22
4)	VB_In ramps up through the chassis power-on. The sequencer, seeing that VB_In has reached V _{Bulk} (Min), and having been control enabled (VBxEn_L, Local Power Enable), will turn on the input to the DC-DC converter. This allows for the module logic to be powered from the output of the converter.	23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38

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CHAPTER 13: HARDWARE MANAGEMENT

13.1 INTRODUCTION

	Th ph res po <u>QE</u> fac vid	is chapter describes the functions that manage, control, and monitor ysical components of InfiniBand Modules and the Chassis in which they side. This chapter addresses hardware management for InfiniBand to- logies mentioned in <u>Section 6.8, "Compliance Channel - DDR and</u> <u>DR," on page 203</u> . The xCAs and Switches that are packaged in a form ctor other than those defined by this specification, which optionally pro- le the defined hardware management functionality, are also described.	6 7 8 9 10 11 12
	Ad fini Ch Ch	ditionally, this chapter defines required and optional features of the In- Band IB-Modules, the InfiniBand Chassis, the InfiniBand Target annel Adapters, the InfiniBand Switches, and the InfiniBand Host annel Adapters to support the following:	13 14 15 16
	1)	Communication with the Baseboard Manager	17
	2)	In-Band and Out-of-Band facilities for Graceful Hot Removal	19
	3)	Standard visual indicators to assist the user in Hot Add and Hot Re- moval of IB-Modules	20 21
	4)	Access to IB-Module Vital Product Data (VPD)	22
	5)	Access to IB-Module optional environmental variables	23
	6)	Access to IB-Module's LEDs	25
	7)	Remote control of a Chassis power state	26
	8)	Provide In-band facilities to manage Chassis and IB-Modules on the InfiniBand Fabric	27 28
13.1.1 NOMENCLATURE			29
	Fo tra do ifie live	r consistency with <i>InfiniBand Architecture Specification, Volume 1.</i> nsfers on IB-ML (defined in <u>Section 13.3.2.2, "IB-ML." on page 495</u>) are ne most significant byte, most significant bit first unless otherwise spec- id. Multi-field structures, as shown in tabular form in this chapter, are de- ered from the top of the table to the bottom.	30 31 32 33 34 35
13.2 OVERVIEW			36
	Th me IB- Ma	is section briefly describes IB-Module Interfaces, Hardware Manage- ent Methods, Managed Units, Classes of Management Transactions, Module Management, Non-Module Device Management, and Chassis anagement.	37 38 39 40 41
			42

13.2.1 MANAGEMENT MODEL

<u>Figure 157</u> shows the generic Baseboard Management model for an InfiniBand Module as described in *InfiniBand Architecture Specification, Volume 1*, Chapter "General Services", Section "Baseboard Management".



Figure 157 Baseboard Management Architecture

Figure 158 shows a generic management model for an InfiniBand Module.



Figure 158 Module Management Model

An InfiniBand Module includes at least one InfiniBand Link, a Baseboard Management Agent (BMA: See *InfiniBand Architecture Specification, Volume 1*, Chapter "General Services", Section "Baseboard Management"), one IB-ML Agent (an interface to the InfiniBand Management Link (IB-ML)), one Module Management Entity (MME), and the applications (functions) the Module performs. The Module, through the logical MME, includes (or emulates) a SEEPROM as a non-volatile storage to hold ModuleInfo (including Vital Product Data, VPD), InfiniBand-required LEDs, local Power Regulation, and other optional management devices. The IB-ML interface is the means by which an optional Chassis Management Entity (CME) may appropriately monitor and control certain aspects of a Module.

InfiniBand does not specify how to implement the required IB-ML and the IB-ML functional blocks. The Module may implement these functions using discrete components on a PCB, integrate them into the IB ASIC, or use a micro-controller; however, they must all be visible via the InfiniBandspecified methods on the IB-ML and the IB Link. Please see <u>Table 120</u> Module Feature Requirements on page 494 for a list of the required and optional features and <u>Table 126 Module Facility Requirements on page</u> <u>520</u> for requirements for facilities supporting the features on Modules.



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13.2.2 MANAGED UNITS

	The Baseboard Manager desires to have knowledge of the following units:	2
	HCA	3
	IB Modules	4
	Non-Module xCA ID	э 6
	Non-Module xCA_NID	7
	Non-Module Switch NID	8
	Non-Module Switch ID	9
	Switches	10
	Routers	11
	Repeater Modules	13
	Chassis into which the above are resident	14
	A unit is considered "manageable" if it provides basic information about it-	15
	self and where it is located. This information is called "Vital Product Data"	16
	(VPD). The InfiniBand specification defines the minimal information re-	17
	ageable".	19
		20
	C13-1: For the purposes of Baseboard Management, a Router shall be considered equivalent to a Switch	21
	considered equivalent to a Owneri.	22
13.2.3 MANAGEMENT METHODS	6	23
	• HCA	24
	IB Modules	26
	Non-Module xCA_ID	27
	Non-Module xCA_NID	28
	Non-Module Switch NID	29
	Non Modulo Switch ID	31
		32
	Switches	33
	Routers	34
	Repeater Modules	35
	Chassis into which the above are resident	37
	A unit is considered "manageable" if it provides basic information about it-	38
	self and where it is located. This information is called "Vital Product Data"	39
	(VPD). The InfiniBand specification defines the minimal information re-	40
	ageable".	41
		42

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Hardware Management

13.2.3.1 IN-BAND MANAGEMENT

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	In-band management refers to the monitoring and the control of InfiniBand components using messages transferred on their IB Fabric Link. After connecting to the fabric, IB components establish their physical link automatically and are able to receive Management Datagram (MAD) packets on QP0 and QP1.	2 3 4 5 6
	In-band hardware management messages are Baseboard Management messages that traverse the InfiniBand Fabric. This class is defined in <i>In-finiBand Architecture Specification, Volume 1</i> , Chapter "General Services". The Baseboard Management Software (referred to as the "Baseboard Manager") uses these messages to gather health and inventory information about InfiniBand-attached devices and Chassis. The Baseboard Manager may also perform management control operations such as reset or power control on InfiniBand-attached devices and Chassis. Also see <i>InfiniBand Architecture Specification, Volume 1</i> , Chapter "General Services", Section "Baseboard Management".	7 8 9 10 11 12 13 14 15
	InfiniBand Architecture Specification, Volume 1 defines HCAs, Switches, Routers, and TCAs as protocol-aware units and can therefore process In- band management messages; conversely, Repeaters are not protocol- aware and do not comprehend management messages.	16 17 18 19
	All protocol-aware Modules that receive Baseboard class management messages on their General Services Interface (GSI) forward those mes- sages onto the BMA implemented within the Module. As specified in <i>In- finiBand Architecture Specification, Volume 1</i> , the Baseboard class uses the General Service Interface (GSI) on QP1 or a redirected QP.	20 21 22 23 24 25
	An agent across the IB Link may query <i>this</i> IB-Module's management information (ModuleInfo), or the Chassis management information (ChassisInfo) <i>via</i> this IB-Module.	26 27 28
13.2.3.1.1 Management by Proxy	Non-protocol-aware units are not directly addressable on the InfiniBand fabric; a proxy is required to be manageable from the fabric. Chassis and Repeater Modules require proxies.	29 30 31 32 33
	A proxy is a device that provides InfiniBand Baseboard Management access on behalf of an entity that does not accept InfiniBand Baseboard Management messages. For example, an xCA Module or a Switch may act as a proxy for accessing a Chassis Management Entity (CME) (See Section 13.6.3.2, "Ib2CME," on page 574 and Section 13.5.2.7, "Chassis-Info Device." on page 548) while a Chassis Management Entity (CME) or a Switch may act as a proxy for accessing a Repeater Module (See Section 13.5.2.6, "IB-ML Selector Proxy." on page 548).	 34 35 36 37 38 39 40 41 42

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13.2.3.2 OUT-OF-BAND MANAGE	EMENT	1
	Out-of-band management messages traverse a transport other than the InfiniBand fabric.	2 3 4
13.2.3.2.1 IB-ML		5
	InfiniBand specification defines an interface called InfiniBand Manage- ment Link (IB-ML). IB-ML is a multi-drop, multi-master, two-wire serial bus which uses SMBus 1.1-based data transfer and arbitration protocols[24]. This interface connects IB-ML devices on IB-Modules with the Chassis. IB-ML does not electrically connect to more than one IB-Module or more than one Backplane connector. (See <u>Table 113 IMx* DC Specifications on</u> <u>page 453</u> and <u>Table 114 IMxDat</u> , IMxClk AC Timing Specifications on <u>page 455</u> .)	6 7 8 9 10 11 12
	IB-ML Out-of-Band messages, along with other side-band signals such as Power Request (IMxPReq_L), Presence Detect (IMxPRst), and Interrupt (IMxInt_L) allow communication between Chassis and Module entities. IB-ML is available even when the InfiniBand fabric is not operational and before a link is connected. For example, at power up, a Chassis back- plane may use the out-of-band IB-ML to enumerate Modules and deter- mine their power requirements prior to enabling their Bulk power.	14 15 16 17 18 19 20
	IB-ML, primarily, provides an out-of-band access media for Modules; how- ever, Switches, Routers, and other Channel Adapter applications may use IB-ML as well.	21 22 23
13.2.3.2.2 VIRTUAL IB-ML		24 25
	A Channel Adapter or a Switch may provide access to an IB-ML via Base- board Management messages received via the InfiniBand fabric. To soft- ware sending IB-ML access messages on InfiniBand, it is unimportant whether there is a physical IB-ML or not, as long as the messages are ac- cepted and responded to correctly.	26 27 28 29 30
	A device may respond to Baseboard Management messages for IB-ML accesses without implementing a physical IB-ML. This specification refers to such a device as having a Virtual IB-ML.	31 32 33 34
13.2.3.2.3 MULTI-PORTED IB-MODU	LES	35
	Using IB-ML, a Managed InfiniBand Chassis provides some Slot-specific Information (SlotInfo) to every Backplane IB connector. Using a TCA's BMA and IB-ML, the Baseboard Manager accesses the SlotInfo provided by the Chassis. From a backplane's point of view, the SlotInfo for every slot resides at the same location. See <u>Section 13.5.2.7.1, "SlotInfo," on page 549</u> .	36 37 38 39 40 41

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A double-wide IB-Module connects to two adjacent backplane connectors and occupies two slots. The Chassis provides the same ChassisGUID to each slot but different SlotInfo to the two slots.

A Standard or Tall Double-wide IB-Module may connect one or more of its Backplane Connectors to multiple TCAs, to some ports of a multi-ported TCA, or to only one port of a TCA, Switch, Router, or Repeater. The IB-Module ModuleInfo describes the number of TCAs, Ports, and IB-MLs connected to its Backplane Connector. See <u>Section 13.3.2.10, "Mod-</u> <u>uleInfo Device," on page 517</u>.

As an example, <u>Figure 159</u> depicts a two-ported IB-Module which implements two IB-MLs. It shares ModuleInfo and the <u>MME Function Registers</u> 11 while it provides individual <u>MME IbML2Ib Registers</u> for the two IB-MLs. A four-ported IB-Module follows a similar concept. 13

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13.2.3.4 INTER-METHOD OPERATIONS

Baseboard management messages may contain requests for an IB-ML access. The BMA maps these messages into a Write/Read IB-ML transaction. Some of these transactions will return data from IB-ML in the Baseboard Management response message sent back via IB. Other transactions may be split-transactions that cause an IB-ML device to later return a separate IB-ML response back to IB. See <u>Section 13.6.1, "IB-to-</u> <u>MME (Baseboard MAD) Commands," on page 549</u>.

13.2.3.5 CLASSES OF MANAGEMENT TRANSACTIONS

InfiniBand Hardware Management recognizes the following classes of transactions:

- 1) In-band, directed at a Module in a Chassis
- In-band, directed at a non-Module device supporting a BMA in a Chassis
- 3) In-band, directed at the CME (The CME has a direct IB connection.)
- 4) Out-of-band, from a CME, directed at a Module (The Chassis or CME accesses the Module via IB-ML.)
- 5) Out-of-band, from a CME, directed at a non-Module device supporting IB-ML
- 6) Out-of-band, from a Module, directed at the CME (An entity on the Module accesses the CME via IB-ML. Typically, this access will be via IB using an IB to IB-ML access.)
- 7) Out-of-band from a CME to IB (The CME has a physical or virtual IB-ML to IB connection).

13.2.4 MODULE MANAGEMENT

Functions such as IB Module VPD data are modeled as physical devices that are accessed via IB-ML. Common functions, such as VPD, are put at fixed "well-known" addresses on IB-ML.

IB-ML access from IB is accomplished via a single "IB to IB-ML" (IB2IBML) baseboard management message. Encapsulated within that message are parameters that can be used to direct a low-level transaction to a physical IB-ML. This is done to allow separation of the entity that performs IB to IB-ML operations from the functions on IB-ML, as follows.

The device that interprets the IB2IBML message can perform the request transaction without caring about what operation the transaction is performing on IB-ML. This makes it possible to create a device that does the IB to IB-ML operation independent from the functions being accessed on IB-ML. Such an implementation can allow new functions to be added to the IB-ML without impacting the IB to IB-ML device. 41 42

evice may implement IB to IB-ML with a virtual IB-ML that d within the device, or is implemented using proprietary kample, a channel adapter may be designed to provide nting a proprietary non-volatile storage mechanism. As seboard management messages are responded to cor- nentation will be transparent to management software ac- e via IB. resents its Temperature Sensor and SEEPROM informa- at IB-specified addresses. ts a manageable single ported TCA Module. As de- <u>n 13.2.1, "Management Model," on page 478</u> , in-band dule Management Entity (MME) occurs through the In- the BMA. Out-of-band access to the MME occurs _ Agent. Neither the logical partitioning of the TCA, BMA, Agent and IOCs nor the interfaces between any of them
resents its Temperature Sensor and SEEPROM informa- at IB-specified addresses. ts a manageable single ported TCA Module. As de- <u>n 13.2.1, "Management Model," on page 478</u> , in-band dule Management Entity (MME) occurs through the In- the BMA. Out-of-band access to the MME occurs L Agent. Neither the logical partitioning of the TCA, BMA, Agent and IOCs nor the interfaces between any of them
ts a manageable single ported TCA Module. As de- <u>n 13.2.1, "Management Model," on page 478</u> , in-band idule Management Entity (MME) occurs through the In- the BMA. Out-of-band access to the MME occurs L Agent. Neither the logical partitioning of the TCA, BMA, Agent and IOCs nor the interfaces between any of them
ts a manageable single ported TCA Module. As de- <u>n 13.2.1, "Management Model," on page 478</u> , in-band idule Management Entity (MME) occurs through the In- the BMA. Out-of-band access to the MME occurs L Agent. Neither the logical partitioning of the TCA, BMA, Agent and IOCs nor the interfaces between any of them
ides an interrupt line to the Chassis in the form of the ector signal IMxInt_L . All sources of interrupts (power arnings, Hot Removal operations, etc.) on the Module in to this interrupt. See <u>Section 13.3.2.8. "IMxInt L." on</u> inction description of this signal and <u>Table 140 MME</u> rs on page 584 for the definition of the interrupt sources.
ivironmental events or Graceful Hot Removal Requests, ay send traps to the Baseboard Manager using a Base- ent Trap (BMTrap). Additionally, a mechanism is speci- <i>I</i> E to trigger these traps with an IB-ML command to a fodule. See <u>Section 13.3.2.7, "BMTrap," on page 514</u> .
lude the LEDs defined in <u>Section 13.3.2.6, "Module Indi-</u> on page 508.



Repeater Modules include the same LEDs as other Modules to provide a consistent user interface. See <u>Section 13.3.2.6</u>, "<u>Module Indicators</u> (<u>LEDs)</u>," on page 508.



Figure 161 Manageable Retiming Repeater Module

13.2.5 NON-MODULE DEVICE MANAGEMENT

A protocol-aware device is considered "Non-Module" if it is not packaged in an InfiniBand module form factor.

A Non-Module Switch_ID is a Switch that is not on an InfiniBand Module and provides ChassisGUID. A Non-Module xCA_ID is an xCA that is not on an InfiniBand Module and provides ChassisGUID. A Non-Module Switch_NID is a Switch that is not on an InfiniBand Module and does not provide ChassisGUID. A Non-Module xCA_NID is an xCA that is not on an InfiniBand Module and does not provide ChassisGUID.

The Baseboard Manager may use <u>ReadVPD</u> to assess the physical location of a Non-Module device through ChassisInfo.

A Non-Module device only provides a subset of Baseboard information as specified in <u>Section 13.3.2.10</u>, <u>"ModuleInfo Device," on page 517</u> and <u>Section 13.7.7</u>, <u>"ChassisInfo Record," on page 612</u>.

InfiniBand ¹ ³⁰ Architecture Release 1.2 Volume 2 - Physical Specifications	Hardware Management	Final
13.2.5.1 TCA		
	Non-Module TCAs perform InfiniBand operations of part of an InfiniBand defined Module form factor. T mounted to be permanently associated with a give types of TCAs follow the same in-band programmi Modules so that they may be managed in the same band interface is not specified; if one exists, IB-ML	on the link, but are not hey are typically in Switch port. These ng model as the TCA e manner. Their out-of- . may be used.
3.2.5.2 Switch		
	Non-Module Switches perform InfiniBand defined s are not part of an InfiniBand defined Module form fa aware device, a Switch provides a BMA; Baseboar may be directed to a Switch in-band. The out-of-ba specified; however, IB-ML may be used.	switch operations, but actor. Being a protocol- d Management MADs and interface is not
	A form of non-Module Switch is one that may be mo and provide a number of ports to slots which accep Such a Switch may directly provide IB-ML proxy fu supports or it may interface or emulate a CME. See <u>ML Selector Proxy," on page 548</u>	unted within a Chassis t InfiniBand Modules. Inctions for the slots it e <u>Section 13.5.2.6, "IB-</u>
13.2.6 CHASSIS MANAGEMENT		
	Within the scope of InfiniBand Hardware Managen collection of InfiniBand Modules and their associat resources housed within a single mechanical pack	nent, a Chassis is the ed power and cooling age.
	A Chassis can be Unmanaged, Passively Managed	d, or Actively Managed.
13.2.6.1 ACTIVELY MANAGED CI	HASSIS	
	An Actively Managed Chassis provides an InfiniB and physical Slot Information to every InfiniBand M unique IB-ML. In addition, it provides a Chassis Ma (CME) on at least one InfiniBand Module's IB-ML. In Chassis, the Slot Information (SlotInfo) for every M that identifies all of the Slot(s) that may access the	and specified GUID odule on the Module's anagement Entity n an actively managed lodule provides a field cME.
	Figure 162 depicts a system with an actively mana system may be a server (including a CPU, memory or a Box of Slots. Several IB-Modules plug into the The Switch may reside on an IB-Module or on the	aged Chassis. This complex, and an HCA) Chassis backplane. Chassis backplane.
	A system with an actively managed Chassis includ ment Entity (CME). The CME has direct connectio ment Link (IB-ML) to at least one Module and option to the Switch. The CME and the Baseboard Manag	es a Chassis Manage- ns via the IB Manage- nally to all Modules and ger use these links to

move management data and commands between the CME and IB-Modules and Switches.

The CME is a proxy for Chassis specific elements (power, thermal, security, etc.). A CME may optionally support a private management link to connect to another Chassis. This private link is outside of the scope of InfiniBand specification. The CME may provide a proxy for communication between Modules (See Section 13.5.2.6, "IB-ML Selector Proxy," on page 548).



Figure 162 Actively Managed Chassis

The CME may maintain management information for the Chassis as a whole and may store this data in non-volatile storage located on a private management bus. The CME may use this private management bus for sensors and other Chassis management devices.

The CME may optionally connect to the Power Enable (**VBxEn_L**) signals on the InfiniBand backplane connectors (not shown in <u>Figure 162</u>). The Power Enable signals allow the CME to power-up or power-down IB-Mod-

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ules. See <u>Chapter 4: Port Signal Definitions</u> for a description of the **VBxEn_L** signals.

IB-Modules contain their own management data. These data are available to the CME via IB-ML and to agents on the InfiniBand fabric via IB.

<u>Table 129 Chassis Feature Requirements on page 544</u> identifies the optional and required features of an actively managed Chassis.

13.2.6.2 PASSIVELY MANAGED CHASSIS

A **Passively Managed** Chassis provides an InfiniBand specified ChassisGUID and physical Slot Information to every InfiniBand Module on the Module's unique IB-ML. See <u>Section 13.2.6.4</u>, "Globally Unique Identifiers," on page 492 and <u>Section 13.5.2.7</u>, "ChassisInfo Device," on page 548.

Figure 163 shows an example of a passively managed Chassis. The ChassisInfo blocks depict the ChassisGUID, the ChassisInfo, and the Slot-specific Information (SlotInfo). These ChassisInfo blocks are separate from their ModuleInfo counterparts on IB-Modules.



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<u>Table 129 Chassis Feature Requirements on page 544</u> identifies the optional and required features of a passively managed Chassis.

13.2.6.3 UNMANAGED CHASSIS

An *Unmanaged* Chassis does not implement any IB-specified GUID or Slot Information and leaves Module IB-ML unconnected.

13.2.6.4 GLOBALLY UNIQUE IDENTIFIERS

For the purposes of Hardware Management, two EUI-64 compliant Globally Unique Identifiers (GUIDs) are defined for the physical elements of an IB-Module and a Chassis. These GUIDs allow a Baseboard Manager to create a logical to physical mapping of the elements that comprise an InfiniBand fabric. These identifiers are:

- ModuleGUID: associated with the physical entity on which an xCA, Switch or Repeater resides
- ChassisGUID: associated with the physical entity into which a Module is plugged

If an xCA or Switch is permanently affixed to a Chassis (i.e. Non-Module), the ModuleGUID and ChassisGUID may be the same.

When used in conjunction with the Globally Unique Identifiers defined in *InfiniBand Architecture Specification, Volume 1*, Chapter "IBA Addressing", the mappings created with these GUIDs allow a Baseboard Manager to determine physical relationship of fabric elements for operations where actions to one element may affect other elements. Such operations include physical Module removal with multiple xCAs present, power management with multiple xCAs present, repeater management, and partitioning. Figure 164 depicts the logical view of these GUIDs for an

IB-Module and its associated Chassis. (In this context, PortGUID depicts a combination of NodeGUID and Port#).



13.3 MODULE FEATURES

13.3.1 MODULE FEATURE REQUIREMENTS

This section defines the required and optional features for various types of InfiniBand devices and physical packages.

The column cells of <u>Table 120</u> shall have the following definition:

- **Req** A Module **shall** implement the facility labeled **Req** in the "Requirement" column.
- **Rec** A Module **may** implement the feature labeled **Rec** in the "Requirement" column. It is recommended that the feature be provided. If the feature is provided, the Module **shall** follow the provisions of the feature description section.
- **Opt** A Module **may** implement the features labeled **Opt** in the "Requirement" column. If the feature is provided, the Module **shall** follow the provisions of the feature description section.
- **N/A** The feature is not applicable to the package being addressed.

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C13-2: An InfiniBand defined Module containing an InfiniBand protocolaware device **shall** provide those features and the dependent facilities labeled as "**Req**" in the "Protocol-aware Module" column of <u>Table 120</u>.

C13-3: An InfiniBand defined Module not containing an InfiniBand protocol-aware device **shall** provide those features and the dependent facilities labeled as "**Req**" in the "Non-Protocol-aware Module" column of <u>Table 120</u>.

C13-4: An InfiniBand Channel Adapter device mounted on a package other than an InfiniBand Module **shall** provide those features and the dependent facilities labeled as "**Req**" in the "Non-Module xCA" column of <u>Table 120</u>.

C13-5: An InfiniBand Switch device mounted on a package other than an InfiniBand Module **shall** provide those features and the dependent facilities labeled as "**Req**" in the "Non-Module Switch" column of <u>Table 120</u>.

Feature	Protocol- aware Module	Non-Protocol- aware Module	Non-Module xCA	Non-Module Switch
BMA	Req	N/A	Req ^a	Req ^a
IB-ML (physical)	Req	Req	Opt	Opt
Module Management Entity (MME) (via IB)	Req	N/A	Req ^a	Req ^a
MME Function Registers	Req ^b	Req ^b	Opt	Opt
MME IbML2Ib Registers	Req ^b	N/A	Opt	Opt
MME Commands	Opt	N/A	Opt	Opt
Graceful Hot Removal	Req	Req ^c	Opt	Opt
P Key, Q Key, and B Key	Req	N/A	Req ^d	Req ^d
Module Indicators (LEDs)	Req	Req	Opt	Opt
<u>BMTrap</u>	Req	N/A	Opt	Opt
IMxInt_L	Req	Req	Opt	Opt
Presence Detection	Req	Req	Opt	Opt
ModuleInfo Device	Req	Req	Opt ^{e f}	Opt ^{g f}
ChassisInfo Device	N/A	N/A	Req ^{i h}	Req ^{i j}

Table 120 Module Feature Requirements

a. Require packaged provide Me	d to support the "ReadVPD" and "WriteVPD" Baseboard MAD command, especially when on a removable form factor. To provide a logical-to-physical association, an assembly shall oduleGUID and ChassisGUID.	1 2
b. Access	to this feature can be implemented either using a register interface, or using MME_	3
<u>Command</u> c. Only the	<u>s</u> . • CME_RTR and CME_CTR facilities, accessed via IB-ML, are required. The MME_CTR	4
facility, ac	essed via IB-ML, is optional. The SW_RTR and SW_CTR facilities are not applicable.	5
d. Require detailed fie	d since BMA is required. See <u>Section 13.3.2.10, "ModuleInfo Device," on page 517</u> for ald requirements	6
e. Optiona	I for non-Module xCA_ID only if ChassisInfo Device is present. Required for non-Module	7
xCA_ID if f_Instead.c	ChassisInfo Device is not present.	8
Device.		9
g. Optiona Switch JD	I for non-Module Switch_ID only if chassisInfo Device is present. Required for non-Module if ChassisInfo Device is not present	10
h. Require	d for non-Module xCA_ID if ModuleInfo Device is not present.	12
i. Via a col	nection (such as IB-ML) to the Chassis that this Unit attaches.	13
J. Required		14
13.3.2 MODULE FEATURE DES	CRIPTIONS	15
13.3.2.1 BMA		16
	The Baseboard Management Agent (BMA) is a logical entity that accepts.	17
	responds to, and potentially generates Baseboard Management MADs as	18
	defined in InfiniBand Architecture Specification, Volume 1, Chapter "Gen-	19
	eral Services", Section "Baseboard Management" and interfaces with the	20
	on page 497) to perform the provided MAD commands.	21
	<u>on page ter</u>) to perform the provided in the commander	22
13.3.2.2 IB-ML		23
	IB-ML is a multi-drop, multi-master, two-wire serial bus which uses sig-	24
	naling and arbitration protocols similar to that of the SMBus 1.1 bus [24].	26
	It primarily allows for access to defined facilities on the Module from the	27
	Chassis, but it also allows for certain defined operations to be sourced	28
	from the module to the Chassis.	29
	IB-ML is architecturally considered "point-point" in that the address space	30
	from one IB-ML port is not shared with the address space of any other	31
	port. This allows for the same device address assignments to be used on	32
	techniques	33
		34
	An IB-ML is made up of 2 Backplane Connector signals: IMxClk and IM-	35
	xDat . See <u>Section 11.5.1</u> , "IMxClk, IMxDat," on page 448 and <u>Annex A2</u> :	30
	MI signals.	38
		39
	C13-6: An IB-Module shall implement an IB-ML on its Primary Backplane	40
	Connector (Port 1) (See <u>Section 12.5, "Chassis Power Rules," on</u>	41
	page 470 for the definition of the Primary connector.). It may implement	42

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IB-MLs on other available Backplane Connectors; if so, it **shall** keep the multiple IB-MLs electrically isolated from each other.

Logical slave devices on the IB-ML allow access to the ModuleInfo (See <u>Section 13.3.2.10, "ModuleInfo Device," on page 517</u>) and the MME Registers (See <u>Section 13.6.5, "MME Function Registers," on page 581</u>).

C13-7: All Modules **shall** respond as IB-ML slaves for Read and Write access to the device addresses labeled as "**Req**" in the "Access" column of <u>Table 121</u>.

C13-8: A Module **shall not** respond as an IB-ML slave for Read and Write access to the device addresses labeled as Not Permitted "NP" in the "Access" column of <u>Table 121</u>.

o13-1: Modules **may** respond as IB-ML slaves for Read and Write access to the following device addresses labeled as "Opt" in the "Access" column of <u>Table 121</u>.

Function	Device Address ^a			Deferrer	
Function	Hex	Binary	Access	Reference	
ModuleInfo Device	A0h	1010_000b	Req	Section 13.3.2.10 on page 517	
Reserved for future IB definition	A2h	1010_001b	NP		
Reserved for future IB definition	A4h	1010_010b	NP		
Module Specific Use	A6h	1010_011b	Opt		
Module Specific Use	ACh	1010_110b	Opt		
Module Specific Use	AEh	1010_111b	Opt		
ChassisInfo Device	A8h	1010_100b	NP ^b	Section 13.5.2.7 on page 548	
Chassis Specific Use	AAh	1010_101b	NP		
CME Slave	E8h	1110_100b	NP	Section 13.5.2.3.1 on page 547	
MME Function	E0h	1110_000b	Req ^c	Section 13.6.5 on page 581	
MME IbML2Ib	E2h	1110_001b	Req ^c	Section 13.6.5 on page 581	
MME Command	E4h	1110_010b	Opt	Section 13.3.2.3.3 on page 498	

Table 121 Module IB-ML Slave Addresses

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a. This 7-bit Binary notation for IB-ML slave addresses leaves out the Write/Read direction bit which is encoded as the least significant bit on the IB-ML bus during the address phase. The accompanied Hex notation follows this Binary notation by left justifying the 7-bit IB-ML address to fit into an 8-bit wide byte and setting the list significant bit to 0. b. "NP" for this Chassis device address means that the Module, **as a slave, shall not** (not permitted to) implement the resources associated with these addresses. It means that the slave device for this address is present outside of the Module. It **does not** mean that accesses to these addresses using the "<u>ReadVPD</u>" Baseboard MAD command to this address are denied if a physical or virtual IB-ML exists.

c. Access to this feature can be implemented either using a register interface, or using MME Commands. This table lists the required slave address to be used if the feature is implemented using the register interface.

<u>Table 122</u> shows the only other slave addresses that InfiniBand Modules may use.

Slave 8-bit Hex Function Address notation 0100 000 -40h-46h Module-specific use. Typically used for 8574-8-bit and 8575-type 16-bit I²C latches. 0100 011 0101 001 -50h-5Eh Module-specific use. LM78/ADM1024 and other "Heceta"-type monitoring devices. 0101 111 1001 000 -90h-9Eh Module-specific use. Typically used for LM75-style temperature sensors. 1001 111 1011 110 -BCh-BEh Module-specific use. 1011 111 SMBus Device Default. Module Devices that use this address must do so per the 1100 001 C2h SMBus 2.0 specification. 1101 110 -DCh-DEh Module-specific use. 1101 111 1110 011 E6h Module-specific use. Often used for PCA9544-style I²C bus multiplexer.

Table 122 Other Allowed Addresses for InfiniBand Modules

13.3.2.3 MODULE MANAGEMENT ENTITY (MME)

The MME provides a logical view of the applicable specified Module facilities for access in-band via the BMA and Baseboard Management MADs and out-of-band via IB-ML.

C13-9: All Modules, at a minimum, **shall** implement a logical Module Management Entity that implements the required elements of this specification for Baseboard Management and IB-ML operations.

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Module designs are free to choose any implementation mechanism; these may consist of, but are not limited to: discrete components, ASICs, micro-controllers, or Integration with xCA components.

Implementation Note

For example, the ModuleInfo portion of the MME may be implemented as a discrete SEEPROM device directly on IB-ML, be emulated as part of a micro-controller, or be included as part of the same chip containing the xCA attached to IB-ML.

13.3.2.3.1 MME FUNCTION REGISTERS

The MME Function Registers, described in <u>Section 13.6.6</u>, "<u>MME Func-</u> <u>tion Register Summary</u>," on page 583, provide facilities for the CME to access Module functions via IB-ML and for the Baseboard Manager to access the Module functions via IB and via BMA. See also <u>Figure 159</u> <u>Multi-ported IB-Module (an example) on page 484</u>.

The MME Function Registers can be implemented in two ways: As 'physical' registers that are written and read using IB-ML 'register' transactions via address E0h, or as 'logical' registers that are written and read using the <u>WriteMMERegister</u> and <u>ReadMMERegister</u> MME Commands using a 'split-transaction' via address E4h. In either case, <u>Table 140 on page 584</u> is used to specify the register selector and data bytes for the MME Function Registers.

13.3.2.3.2 MME IBML2IB REGISTERS

The MME IbML2Ib Registers, described in Section 13.6.9, "MME IbML2Ib25Register Descriptions," on page 588, provide facilities for the CME to send26messages and traps to the Baseboard Management LID. See also Figure159 Multi-ported IB-Module (an example) on page 484.2728

The MME IbML2Ib Registers can be implemented in two ways: As 'phys-29ical' SendBMTrap and SendIbML2BM registers that are written using IB-30ML 'register' transactions via address E0h, or as split-transaction SendB-31MTrap and SendIbML2BM MME Commands via address E4h. Table 14132on page 588 specifies the data format for the physical 'E0h' register access, while Table 123 on page 499 provides the format for the MME command.333435

13.3.2.3.3 MME COMMANDS

MME commands are split-transaction IB-ML request and response trans-
actions, as described in section 13.6.1.4 IB-ML Split-transaction Mes-
saging on page 561. MME commands are part of the InfiniBand Hardware
Management command set (Section 13.6.1.7. "IB-ML CMD Set Specific
Fields," on page 564). The MME performs the requested operation, for-
mats a response using the sequence number that was passed in the re-37

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quest. MME Commands are transferred on IB-ML via the MME Command address specified in <u>Table 121 on page 496</u>.

For the standard MME commands (commands other than OEM CMD 3 messages), the Source Device ID in the request determines where the MME delivers the response to the commands. The response **shall** be sent as an IB-ML split-transaction response to the slave address specified by the Source Device ID in the request. 7

o13-2: If an entity implements an MME with the features described in 8 <u>Table 123</u>, it shall follow the definitions of <u>Section 13.3.2.3.3</u>, "MME Com-<u>mands," on page 498</u>.

Table 123defines the split-transaction commands for CMD Set = IB-ML11sent to the MME Slave Address. See Section 13.6.1.7, "IB-ML CMD Set12Specific Fields," on page 564for CMD field placement in the split-transaction message.13

Command	CMD	Requirement	Request data	Response data	17 18 19 20 21
GetCMDSetVersion (13.3.2.3.4)	00h	Req	none	<u>byte 1:</u> completion status ^a <u>byte 2:</u> Version of MME command set (CMD Set = IB-ML) that this controller supports. BCD encoded. Initial value = 10h for CMD Set version 1.0	22 23 23 24 25
<u>GetVendorID</u> (<u>13.3.2.3.5</u>)	01h	Opt ^b	none	byte 1: completion status ^{a.} bytes 2+ - A series of one or more 3-byte IDs for each vendor or organization that have defined controller-specific (OEM) commands implemented by this MME. FFFFFh if no controller-specific com- mands. 3-byte ID uses same format as the vendor ID field in ChassisGUID.	26 27 28 29 30 31
Reserved	02h				- 32
<u>ReadVPD</u> (<u>13.3.2.3.6</u>)	03h	Opt ^c	<u>byte 1</u> - VPD Device Selector (address) <u>byte 2</u> - VPD number of bytes to read (1- based. 0 count is allowed)	<u>byte 1: </u> completion status ^{a.} <u>bytes 2+</u> - read data bytes (if any)	34 35 36 37
			<u>bytes 3:4</u> - VPD offset to read (2 bytes)		38 39 40

Table 123 MME Commands

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Command	CMD	Requirement	Request data	Response data
<u>WriteVPD</u> (<u>13.3.2.3.7</u>)	04h	Opt ^c	byte 1 - VPD Device Selector (address) byte 2 - # bytes to write (2-bytes, 1- based. 0 count is allowed) byte 3:4 - VPD offset to read-write bytes 5+: - write data (N bytes)	<u>byte 1:</u> completion status ^a .
<u>OEM</u> (<u>13.3.2.3.8</u>)	05h	Opt	<u>bytes 1-3:</u> vendor ID <u>bytes 4+:</u> vendor-specific data	<u>byte 1:</u> completion status ^{a.} <u>bytes 2-4:</u> vendor ID <u>bytes 5+:</u> vendor-specific response data
Reserved	06h- 0Fh			
WriteMMERegister (13.3.2.3.9)	10h	Opt ^d	<u>byte 1</u> - register selector per <u>Table 140</u> <u>bytes 2+</u> - write data per <u>Table 140</u>	byte 1: completion status ^{a.}
ReadMMERegister (13.3.2.3.10)	11h	Opt ^d	<u>byte 1</u> - register selector per <u>Table 140</u>	byte 1: completion status ^{a.} bytes 2+ - read data corresponding to bytes 1+ per <u>Table 140</u>
Reserved	12h- 1Fh			
<u>SendBMTrap</u> (<u>13.3.2.3.11</u>)	20h	Opt ^e	<u>byte 1</u> - BMTrapDataLength = count of following bytes, per <u>Table 141</u> <u>byte 2</u> - BMTrapType per <u>Table 141</u> <u>byte 3:5</u> - BMTrapTypeModifier varies based on trap type per <u>Table 141</u> <u>byte 6</u> + - BMTrapData per <u>Table 141</u> .	byte 1: completion status ^{a.} Includes com- mand-specific status per <u>Table 141</u>
<u>SendIbML2BM</u> (13.3.2.3.12)	21h	Opt ^e	byte 1 - BMDataLength per Table 141	<u>byte 1:</u> completion status ^{a.} Includes com- mand-specific status per <u>Table 141</u>

Table 123 MME Commands

c. Required if the ModuleInfo Device or ChassisInfo Device features are required per <u>Table 120 Module Feature Requirements on</u> page 494, but it is not implemented via address A0h.

d. Required if the MME Function feature is required per <u>Table 120</u>, but it is not implemented via address E0h.

e. Required if the MME IbML2Ib feature is required per <u>Table 120</u>, but is not implemented via address E2h.

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InfiniBand TM Architecture Release 1.2 VOLUME 2 - PHYSICAL SPECIFICATIONS	Hardware Management	October, 2004 FINAL	-
13.3.2.3.4 GETCMDSETVERSION			1
	GETCMDSETVERSION is an IB-ML split-transaction the version of the IB-ML command set (CMD Set by the MME. The version information is stored in imal) format, where the most-significant nibble h number and the least-significant nibble holds the For example, a value of 09h corresponds to IB-M 0.9.	on command that returns at = IB-ML) implemented BCD (binary coded dec- olds the major version a minor version number. AL command set version	2 3 4 5 6 7 8 9
13.3.2.3.5 GETVENDORID			1
	GetVendorID command is an IB-ML split-transaturns the ID for the vendor that has defined content = OEM) messages for the MME. The vendor ID for used in the ChassisGUID. If no CMD Set = OEM a value of 00_00_0 oh shall be returned in the repossible for more than one set of vendor-specific mented on an MME.	ction command that re- roller-specific (CMD Set ormat is the same as that 1 messages are defined, esponse. Note that it is c commands to be imple-	1 1 1 1 1 1 1 1 1 1
13.3.2.3.6 READVPD			1
	ReadVPD command is used to retrieve data from that is selected by the "Device Selector" field. If a vice is not provided at address IB-ML address A be used to provide a logical VPD Device that is a Selector" field value of A0h. The amount of data the by the overall IB-ML command length limit of 36-b through PEC, inclusive.	n the logical VPD Device physical ModuleInfo De- 0h, this command shall ccessed using a "Device hat can be read is limited bytes from Slave address	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2
	Architectural Note		2
	The ReadVPD Number of Bytes to Read (NBR) bytes so as to 1) allow for larger data abstraction may not use physical IB-ML devices that are lime ability and 2) to accommodate emerging physical 16KB of address ability.) field is defined to be 2 on implementations that ited to 256B of address al devices that allow for	3 3 3 3 3 3
13.3.2.3.7 WRITEVPD			3
	WriteVPD command is used to write data to the is selected by the "Device Selector" field. If a phy is not provided at address IB-ML address A0h, thused to provide a logical VPD Device that is accelector" field value of A0h. The amount of data that	logical VPD Device that vsical ModuleInfo Device his command shall be ssed using a "Device Se- t can be written is limited	3 3 3 4 4

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	by the overall IB-ML command length limit of 36-by through PEC, inclusive.	tes from Slave address 1
	Architectural Note	3
	The <i>WriteVPD</i> Number of Bytes to Write (NBW) for bytes so as to 1) allow for larger data abstraction may not use physical IB-ML devices that are limited ability and 2) to accommodate emerging physical 16KB of addressablity.	Field is defined to be 25implementations that6ed to 256B of address7devices that allow for89
13.3.2.3.8 OEM		1(
	This IB-ML split-transaction message allows a ver define additional MME functions. The message inc that helps ensure that data parameter values spec organization do not interfere or need to be reconci lected by another vendor or organization. All other fied by the vendor or organization identified by the	ndor or organization to ludes a vendor-ID field cified by one vendor or iled with the values se- data fields are speci- e vendor-ID field.
	The OEM MME command specified here is within Set (<u>Table 123: MME Commands</u>) and shall utilize fields (Destination Device ID, Source Device ID, R etc.) as the other standard MME commands speci	the IB-ML Command the same message s, CMD Set, Length, fied in this section.
13.3.2.3.9 WRITEMMEREGISTER		22
	WriteMMERegister command provides the mechalogical MME Function Register. The "register select data" field contents are obtained from the "Registe Data" columns in <u>Table 140 MME Function Register</u> spectively.	nism to write to a given ctor" value and "write r (selector)" and "Write <u>ers on page 584</u> , re- 20 21
13.3.2.3.10 READMMEREGISTER		28
	logical MME Function Register. The "register selected data" field contents are obtained from the "Register Data" columns in <u>Table 140 MME Function Register</u> spectively.	r (selector)" and "Read rers on page 584, re-
13.3.2.3.11 SENDBMTRAP		34
	SendBMTrap command provides the mechanism send a BMTrap method message to the Baseboar The Module uses the components of the BM.Class "BMTrap Type", "BMTrapTypeModifier" and "IBMT SendBMTrap in <u>Table 123 on page 499</u>) to form th as defined in InfiniBand Architecture Specification "General Services", Section "Baseboard Managen BMTrapData field is limited by the requirement that	to direct the MME to and Management LID. sPortInfo and the arapData" fields (See the datagram message , Volume 1, Chapter nent". The size of the at MME commands be

limited to an overall length of 36-bytes from slave address through PEC, inclusive.

Architecture Note

This command is intended to be used by a CME to communicate with the Baseboard Manager and should be used in lieu of the *SendIBML2BM* command. A node running the Baseboard Manager can use the method in the Baseboard class MAD (BMTrap) to direct the MAD to the Baseboard Manager versus the node's BMA as a BMA is only to act upon BMSend methods with the R bit being 0 (requests). See Table 131 Common MAD Field usage for Baseboard Management on page 551.

13.3.2.3.12 SENDIBML2BM

SendIbML2BM command provides the mechanism to direct the MME to send a "BMSend" method message to the Baseboard Management LID. The Module uses the components of the BM.ClassPortInfo and the "BM-Data" fields (See SendIbML2BM in <u>Table 123 on page 499</u>) to form the datagram message as defined in InfiniBand Architecture Specification, Volume 1, Chapter "General Services", Section "Baseboard Management". The size of the BMData field is limited by the requirement that MME commands be limited to an overall length of 36-bytes from slave address through PEC.

This command is not recommended for use and is subject to removal in future versions of the specification. A CME should use the <u>SendBMTrap</u> command with "OEM CME" TrapType to communicate with the Baseboard Manager. TrapType of "Generic CME" is defined as a placeholder for potential future definition of IB2CME.

13.3.2.4 GRACEFUL HOT REMOVAL

"Graceful Hot Removal" is the removal of an IB Module that has first been placed in a quiescent state where no activity is present that would cause disruption upon link detachment. V_{Bulk} may or may not be on.

The quiescent state is under control of a central software agent running from across InfiniBand fabric that has access to the B_Key for a given IB Module and claims or otherwise arbitrates ownership of the Module.

In this description, the Baseboard Manager serves as the central software entity; however, depending on implementation, this central agent may be a real Baseboard Manager, be a component of some other software entity that acts as a Baseboard Manager, or be some other software entity with the Baseboard Manager acting as a proxy. Additionally, software implementations may allow for Claiming to be directly controlled by other, non-Baseboard Manager that has been given the B_Key for that IB Module.

The term "interested software entities" refers to those elements that are dependent on the presence of a given IB Module for operation. 2 3 The following facilities or bits are used for interaction with the Baseboard 4 Manager to accomplish Graceful Hot Removal: 5 **CME_RTR** (CME Request to Remove) 6 7 **SW_RTR** (Software Request to Remove) 8 MME_RTR (MME Request to Remove) 9 **CME_CTR** (CME Clear to Remove) 10 11 SW_CTR (Software Clear to Remove) 12 **MME CTR** (MME Clear to Remove) 13 An implementation may elect to make these bits accessible either by im-14 plementing the MME Function feature at address E0h, or by implementing 15 the ReadMMERegister and WriteMMERegister MME commands. See 16 Section 13.6.7, "MME Function Register Descriptions," on page 586 for 17 detailed bit locations. 18 19 Additionally, the **BMTrap** MAD mechanism is used to notify the Base-20 board Manager that a CME or an MME Request to Remove is pending. 21 22 **Operation** 23 To allow for Graceful Hot Removal, it is required that software "Claim" the 24 IB devices on the Module using the SW CTR bit to indicate that software 25 is presently using or preparing to use the Module. 26 27 At power-up, the **SW_CTR** is set to 1b. Once the **SW_CTR** bit is set to 0b, 28 the LEDs on the IB Module indicate that it is not OK to Remove the Module 29 (See Section 13.3.2.6, "Module Indicators (LEDs)," on page 508 for a full 30 description). 31 32 Once an xCA is claimed, the general steps of Graceful Hot Removal are: 33 1) A software process (e.g. a console application), the MME on the 34 Module, or a CME on the Chassis containing the IB device initiates a 35 request for removal to the Baseboard Manager. 36 37 a) For the case that a software process initiates the removal, the Baseboard Manager shall issue a BMSend.SetMod-38 uleState(SW_RTR) prior to collecting the necessary responses 39 from the interested software entities. This allows for the IB Mod-40 ule to indicate the "transition" condition through the blinking of an 41 LED.
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	b) For the case that the request is coming from shall set CME_RTR and then forms and se message on IB-ML to the IB Module. Base the Module shall blink the Module Status L	m a CME, the CME nds a " Send BMTrap " 1 d on the CME_RTR, 2 ED. 3
	Upon receipt of a BMTrap or equivalent polling CME_RTR is 1b, the Baseboard Manager shal ModuleState(SW_RTR)=1 . The setting of the S as an acknowledgement to the setting of CME polling or BMTrap and stops the assertion of the <u>CME RTR Trap Timeout</u> facility.	g means that indicates I issue a BMSend.Set - SW_RTR bit to 1b acts RTR through either ne 9
	Based on the setting of the SW_RTR bit to 1b, the IMxInt_L interrupt to the CME if the CME h moval Status Change interrupt. While awaiting to 1b, the CME shall retry the BMTrap message pRetryPeriod for t _{BMTrapTimeout} Period of time. Se Timeout Parameters.	ne Module shall assert 10 nas enabled the Re- SW_RTR bit to be set 12 ge once every t _{BMTra-} e <u>Table 144: IB-ML</u> 12
2	The Baseboard Manager notifies all interested removal request and determines when all such dependence on the xCA. This is termed "Claim"	software entities of the 10 entities have released 17 n Release".
:	For the case that not all interested software en claim release, the Baseboard Manager shall is ModuleState(SW_RTR)=0 to cancel the reque	tities concur with the ssue a <i>BMSend.Set-</i> 20 est. 21
	For the case that not all responses are received Manager specific time-out period, the Baseboar a BMSend.SetModuleState(SW_RTR)=0 to c Failure to issue this operation will leave the Mod for an indefinite period of time; the LED state for that the Module is not OK to Remove.	d within a Baseboard rd Manager may issue ancel the request. lule in a transition state or this case indicates
2	For the case that all interested software entities devices on the Module, the Baseboard Manage BMSend.SetModuleState(SW_CTR)=1. This software contribution to the Module Status LEE OK to Remove.	s have released the IB 28 er issues a 29 completes the 30 D indication for being 32
Ę	i) If the CME had previously set <i>RemovalControl</i> upon the CME detecting a state change of <i>Inter</i> either through an interrupt or polling, CME may cific actions to prepare for removal. The CME state alControl/Status.CME_CTR=1 to contribute to being OK to Remove.	VStatus.CME_CTR=0, ruptSource.SW_CTR, perform Chassis spe- shall then set <i>Remov</i> - the LED indication for
e	i) If the Module has implemented Module specific a contribution to the LED indication of being OK set <i>RemovalControl/Status.MME_CTR=0</i> . Upo these Module specific functions are in an approximately and the specific functions.	to Remove, it should n determining that opriate state for re-

moval, it **shall** set *RemovalControl/Status.MME_CTR=1* to contribute to the LED indication for being OK to Remove.

See <u>Section 13.4.2, "Removal Control/Status Facility Descriptions," on</u> page 526 for a detailed description of each of the facilities used above.

C13-10: All InfiniBand Modules **shall** implement the MME and Module operations outlined in <u>Section 13.3.2.4</u>, "<u>Graceful Hot Removal," on page 503</u>.

C13-11: The Baseboard Manager **shall** implement the Baseboard Management operations outlined in <u>Section 13.3.2.4, "Graceful Hot Removal,"</u> on page 503.

o13-3: All actively managed InfiniBand Chassis that implements a Module Request-to-Remove function **shall** implement the CME operations outlined in <u>Section 13.3.2.4</u>, "Graceful Hot Removal," on page 503.

13.3.2.4.1 STATE DIAGRAM

The Graceful Hot Removal process is summarized in the state diagram of <u>Figure 165</u> and generally depicts the behavior of the Module Status LED. (See <u>Section 13.3.2.6.3</u>, "Module Status (Green) LED," on page 510).



for QP 1 whose Q_Key is not 0x80010000 are discarded. GMPs destined Management class utilizes the GSI and may be forwarded across subnets. See *InfiniBand Architecture Specification, Volume 1*, Chapter "General Services", Section "MAD Usage Model" for the details on P_Key and Q_Key used for GSIs.

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	For flexible Baseboard Management, xCAs reserve a board Manager(s). If there is a P_Key available for th ager, devices from different data partitions can belon Partition, and the Baseboard Manager can manage t data partition boundaries and therefore regardless of System or Software running on those data partitions.	a P_Key for Base- ne Baseboard Man- g to one Baseboard hem regardless of the Operating
	The Baseboard Management Key (B_Key) provides authentication that helps protect against receipt of ba quest messages. The Baseboard Manager includes to MAD to obtain authorization. The B_Key is used to au source. Similar to the model used for the M_Key, this the fabric has some level of physical security. While t in the header of the BM MAD, B_Key handling deper MAD contains a <i>request</i> or a <i>response</i> message or is <i>finiBand Architecture Specification, Volume 1</i> , Chapt vices", Section "B_Key Usage" for the details on B_K	a separate level of ad management re- he B_Key in the BM uthenticate a trusted model assumes that he B_Key is located nds on whether BM s a BMTrap. See <i>In</i> - er "General Ser- Key.
13.3.2.6 MODULE INDICATORS (I	_EDs)	
	Two functionally independent single-colored LEDs pr tions to the user to show if the Module is Removable tion, Claimed by some software entity, or Requires A Function is also provided.	rovide visual indica- , in Removal Transi- ttention. An Identify
	C13-12: All IB-Modules shall implement two LEDs a <u>Section 13.3.2.6, "Module Indicators (LEDs)," on page</u> sections.	s defined by <u>e 508</u> and its sub-
	o13-4: If a Non-Module InfiniBand assembly implement claim InfiniBand behavior, it shall implement two LEI <u>Section 13.3.2.6, "Module Indicators (LEDs)," on page</u> sections.	ents indicators to Ds as defined by <u>e 508</u> and its sub-
	C13-13: All InfiniBand Modules shall implement the Merations outlined in <u>Section 13.3.2.6, "Module Indicate page 508</u> .	IME and Module op- tors (LEDs)," on
	o13-5: All actively managed InfiniBand Chassis that in Request-to-Remove function shall implement the CN lined in <u>Section 13.3.2.6</u> , "Module Indicators (LEDs),"	nplements a Module ME operations out- <u>" on page 508</u> .

Table 124 summarizes the behavior of the two LEDs.

Table 124 Module Indicator LED Summary^a

Green odule Status)	Amber (Attention)	Definition	Comment
OFF	Х	Module is Removable	
Blink	X	Bulk power is stable Module's DC-DC converter is enabled. Removal Transition is in progress. Module is considered Claimed. Module is not Removable.	Blink Rate is defined in <u>Table 125</u> .During an IB Mod- ule Request-to-Remove negotiation, if the Module Status LED blinks and then goes OFF, the request for OK-to- Remove was successful. If the Module Status LED blinks and then returns to ON, the Request-to- Remove was rejected for some reason. For example the CME timed out waiting for the acknowledgement to CME_RTR BMTrap (SW_RTR stays 0b for "too long") or the system soft- ware could not relinquish the devices (SW_CRT stays 0b and SW_RTR goes back to 0b).
ON	X	Module is Claimed (normal opera- tion or in a power managed state) Module is not removable.	Module Power Management State and the Module LEDs are independent of each other. In a Power Man- aged State, the Module Power may be off while the Module is still Claimed. In that case, the Module Sta- tus LED is accordingly ON.
Х	OFF	No Attention or Identify to the Mod- ule is requested.	
x	Blink	Module Identify is active	Blink rate is defined in <u>Table 125</u> . The CME may invoke the Module Identify Function when Module Power is OFF. The CME may act as a proxy to invoke the Identify Function.
x	ON	The Module, the CME, or the S/W has requested Attention to the Module.	Module Power Management State and the Module LEDs are independent of each other. Due to an attention event, the Module Attention LED may be ON when the Module is in a Power Managed State or when V_{Bulk} is not available or when the Module's DC-DC converter is off.
			If the Module has power, the nature of the requested attention can be determined from status bits on the Module using the BMSend . GetModuleStatus command.
Slow Blink	Slow Blink	Bulk power is stable. Module's DC-DC converter is enabled. LED Test Module is not removable.	Slow Blink rate is defined in <u>Table 125</u> . After Module Insertion, the LEDs blink to provide an LED Test, and then go OFF.

13.3.2.6.1 BLINK DEFINITIONS AND RATES

When used in this specification, the terms defined in <u>Table 125</u> **shall** apply 2 to the repetitive ON/OFF behavior of the LED indicators.

C13-14: An InfiniBand Module **shall** implement the LED Blink Rates as defined in <u>Table 125</u>.

Table 125 Blink Rate Definitions

Term	Frequency	Units	Period	Duty Cycle	Units	Comments
Blink	2	Hz	500ms	50 +/- 5	%	Nominally 250ms ON, 250ms OFF
Slow Blink	1/4	Hz	4s	50 +/- 10	%	Nominally 2s ON, 2s OFF

13.3.2.6.2 COLOR AND INTENSITY

The physical requirements of the LED indicators are specified in <u>Section 9.2.8, "Module Indicators," on page 382</u>.

13.3.2.6.3 MODULE STATUS (GREEN) LED

The Module Status LED generally indicates the removal status of the Module and may take on three states: OFF, ON, or Blinking. For a detailed description of a Graceful Hot Removal, refer to section <u>Section 13.3.2.4</u>, <u>"Graceful Hot Removal," on page 503</u>. It also participates in the LED Test functions. See <u>Section 13.3.2.6.6</u>, <u>"LED Test," on page 513</u> for a detailed description.

Operation

The Module MME causes the Module Status LED to go ON whenever the
Module is "Claimed" by the Software. In this context, being "claimed by
software" means that the unexpected removal of the Module might cause
unexpected software behavior such as a loss of data or a software hang
condition. The user is strongly encouraged not to remove the IB-Module
when the Module Status LED is not OFF.30303132333435

The Module MME causes the Module Status LED to start to Blink when an
IB Software entity such as the Baseboard Manager sets the SW_RTR bit
(Software Request-to-Remove) or when the CME sets the CME_RTR.
(The CME initiates the CME_RTR BMTrap.)36
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The Module MME causes the Module Status LED to continue to Blink until the IB Software entity sets the **SW_CTR** (Software Clear-to-Remove) bit 42

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to indicate that the removal request was granted, or until the IB Software removes the **SW_RTR** bit (SW denied the removal).

3 The CME uses SW RTR as an acknowledgement that the Request-to-Remove BMTrap has been received. Since there is a small possibility that 4 the Request-to-Remove BMTrap could get "lost" due to a data corruption 5 or other error, the CME shall periodically re-send the Request-to-remove 6 BMTrap while waiting for SW_RTR. (See SECTION 13.3.2.4, "GRACEFUL 7 HOT REMOVAL," ON PAGE 503.) If the CME times out waiting for the 8 SW RTR, the CME shall clear the CME RTR bit and shall set the Atten-9 tion LED using the CME_RTR_Trap_Timeout status bit. While SW_RTR is 0b, in response to CME_RTR getting cleared, the Module MME shall 10 cause the Module Status LED to go ON (back to the "SW claimed" state). 11

To indicate that it is "OK to Remove" the IB-Module, the Module MME shall cause the Module Status LED to go OFF when the SW_CTR, CME_CTR, and the MME_CTR are all asserted.

There might be several reasons for which a request for removal may be delayed or denied.

- The MME **may** hold **MME_CTR** negated while it is logging events or performing a shut-down operation such as flushing data buffers.
- The CME may hold CME_CTR while it performs Chassis specific operations.
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- The Software may hold SW_CTR while it is in the process of bringing the Module into a quiescent state.
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<u>Control</u>

C13-15: Using the following pseudo-code, the Module's MME shall implement the composite behavior of the Module Status LED with priority of facilities:

if <u>Initiate LED Test</u> is 1b	30
the Module Status LED "slow blinks" as defined in Table 125;	31
else If <u>LED_Enable</u> is 0b,	32
the Module Status LED is OFF;	33
else If <u>CME_Force_OKTR</u> is 1b,	34
the Module Status LED is OFF;	25
else If <u>Module_OKTR</u> is 1b,	30
the Module Status LED is OFF;	36
else If <u>SW_RTR</u> , <u>MME_RTR</u> , or <u>CME_RTR</u> is 1b, but (<u>SW_CTR</u> ,	37
<u>MME_CTR</u> , <u>CME_CTR</u>) is not 111b,	38
the Module Status LED "blinks" as defined in <u>Table 125;</u>	39
else If <u>Module_OKTR</u> is 0b,	40
the Module Status LED is ON;	41
else,	10

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	Error since all cases are supposed to have been covered by now!
	Status
	The status of the Module Status LED is provided through the
	Module Status LED State facility (See Section 13.4.3.7 on page 532).
3.3.2.6.4 ATTENTION (AMBER) LEI)
	The Attention LED actively indicates that an Attention condition has been
	raised for the Module. It also participates in the LED Test and Module
	Identify functions. See <u>Section 13.3.2.6.6, "LED Test," on page 513</u> and
	<u>Section 13.3.2.6.7, Module Identity, on page 513</u> for detailed descrip-
	The Module MME keeps the Attention LED OFF when neither the CME,
	the Module, nor the IB Software has detected any problem with the
	Module to request attention.
	The Module MME turns the Attention LED ON when the CME, the Module
	or the IB Software is requesting attention to the IB-Module.
	The Module MME causes the Attention LED to perform a "Blink" cycle as
	defined in <u>Table 125 Blink Rate Definitions on page 510</u> when the <u>Module</u>
	the Module Identify being deasserted, the Attention I FD returns to indi-
	cating whether an Attention condition exists or not.
	Control
	C12-16: Using the following pseudo-code, the Module's MME shall imple-
	ment the composite behavior of the Attention LED with priority of facilities.
	The Attention LED shall reflect the Module's Attention state while VAux is
	available.
	It <u>Initiate LED Test</u> is 1b
	alse If LED Enable is 0b
	the Attention LED is OFF:
	else lf Module Identify is 1b.

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else,

the Attention LED "blinks" as defined in Table 125;

the Attention LED is ON if any of the following is set:

MME Module Attention

CME Module Attention

CME RTR Trap Timeout

SW Module Attention

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13.3.2.6.5 Status			1
	The status of the Attention LED is provided throu <u>Attention LED State</u> facility (See <u>Section 13.4.3</u>)	gh the <u>6 on page 531</u>).	2
13.3.2.6.6 LED TEST			4 5
	LED Test is defined as a single "Slow Blink" cycle on page 510) of both indicators in synchronism a turned to the state indicating the current Module are ON when the test is to occur, they both turn O the "Slow Blink" cycle.	(as defined in <u>Table 125</u> fter which they are re- condition. If both LEDs FF for 2 seconds before	6 7 8 9 10
	C13-17: All Modules shall perform an LED Test a lowing:	as indicated by the fol-	11 12 13
	 A Module shall initiate an LED Test upon verter's <u>Vout</u> reaching its valid voltage lev 	the Module DC-DC con- vel.	14 15
	 b) A Module shall initiate an LED Test upon Status.Initiate_LED_Test register on IB-M 	a write to the LEDTest- L.	17 18
	 A Module shall initiate an LED Test upon ModuleAttention(Initiate_LED_Test) from 	receipt of BMSend.Set- n an IB link.	19 20
			22
	Software Implementation Note		23 24
	Before B_Keys are assigned, any IB Software n Send.SetModuleAttention(assert Module Ide feature serves as a diagnostic tool. After B_Key Node checks Baseboard MADs (including the S tribute) against B_Key to restrict access.	nay issue the BM- ntify) command. This s are assigned, the etModuleAttention At-	25 26 27 28 29
13.3.2.6.7 MODULE IDENTIFY			30 31
	Module Identify is a modified extension to the LED the Baseboard Manager or the CME may repeate LED to Identify the Module.	Test operation whereby edly Blink the Attention	32 33 34 35
	The Baseboard Manager, using BMSend.SetMo <i>tion</i> (Assert_Identify), or the CME, using the LED Status.Assert_Identify IB-ML register, may period Identify operation.	<i>duleAtten-</i> Test- ically re-arm the Module	36 37 38 39
	C13-18: If the Module Identify operation is rearmed being complete, the MME shall repeat the Module	ed prior to the operation le Identify operation.	40 41 42

Software Implementation Note

The CME or the Baseboard Manager **should** repeat the Module Identify command within the "IdentifyPeriod" interval (as defined in <u>Table 128</u> on page 530) so that the viewer perceives the LED blinking continuously.

13.3.2.6.8 LED BEHAVIOR IN POWER MANAGEMENT STATES

The meaning of the Module Status and Attention LEDs do not change when a power management state is entered.

Architectural Note

By definition, if the Module is claimed by a software entity, it is not OKto-Remove. If the Module is in a power managed state, the Module Status LED reflects whether it is "claimed" or not. If the Module is claimed, the Module Status LED is ON.

The Attention LED reflects whether the Module requires attention regardless of its power management state.

13.3.2.7 BMTRAP

The Baseboard Management Trap (BMTrap) is defined in *InfiniBand Architecture Specification, Volume 1*, Chapter "General Services", Section "BM Methods" and the related sections supporting this method. It is a mechanism that a Module can use to send an unsolicited Unreliable Datagram to the Baseboard Manager in response to environmental events or Graceful Hot Removal Requests. Additionally, a Module may be used by a CME to inject a **BMTrap** as a part of the Graceful Hot Removal process (See <u>Section 13.3.2.4, "Graceful Hot Removal," on page 503</u>).

InfiniBand Architecture Specification, Volume 1 defines that each of the General Service classes have the attribute **ClassPortInfo**. Information in the **BM.ClassPortInfo** allow for **BMTrap** to be routed through the fabric to the Baseboard Manager. Namely, the following components of this attribute are directly applicable; the other components apply as defined in *InfiniBand Architecture Specification, Volume 1*:

- CapabilityMask:0 Indicates whether BMTraps are supported
- TrapGID GID to use in a GRH for global routing
- TrapLID LID to use in the LRH for local routing
- TrapQ_Key Q_Key associated with the QP through which the BMTrap is sent

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	The Module embeds the GID of the Baseboard Mana Baseboard Management Class MAD Trap to the Bas See <u>Section 13.6.9.1, "SendBMTrap," on page 588</u> for BMTrap.	ager and sends a seboard Manager. ¹ r the format used for ² 3 4	
	A Module may send a generic Baseboard Managemover IB when it detects Module-specific events.	ent Trap (BMTrap) 5 6	
	As Baseboard Management Traps use Unreliable Da should attempt to send three (3) BMTraps for every e suppressed upon the receipt of a BMTrapRepress M <i>finiBand Architecture Specification, Volume 1</i> , Section	atagrams, Modules event. Traps may be IAD as defined in <i>In-</i> n 13.4.9.	0
	The Baseboard Manager should read the Module Sta source of the event. See <u>Section 13.6.3.16</u> , "GetMod page 579 for a description of this command.	tus to determine the 1 tuleStatus," on 1 1	2 3 4 5
13.3.2.8 IMxInt_L		1	5 6
	IMxInt_L is a Backplane Connector signal that a Mossponse to a state change of any event that the CME Module.	dule asserts in re- has enabled on the 1 2	7 8 9
	An interrupt facility has the following four (4) defined a	associated functions: 2	:1
	 Status - indicates that a state change has occurre "Clear" operation 	ed since the last 2 2	2 :3
	2) Clear - clears the Status function of the facility	2	:5
	 Source - indicates whether the condition is prese ically is the actual "interrupt generating device" in of the MME Function. 	ntly active. This typ- ² nplemented as part ² 2	.6 7 8
	 Control - indicates whether the status indication i the IMxInt_L signal 	s allowed to assert 2 3	9
	These facility functions are accessed by the CME three registers:	ough three (3) MME	123
	InterruptClearStatus (Section 13.6.7.1 on pace)	ae 586) 3	4
	InterruptSource (Section 13.6.7.2 on page 58	3 <u>6)</u> 3	5
	InterruptControl (Section 13.6.7.3 on page 58	3 3 <u>6)</u> 33	6
	Every bit in the <u>InterruptSource</u> register has a corres <u>terruptClearStatus</u> and a bit in the <u>InterruptControl</u> re ister bit definition in <u>InterruptClearStatus on page 584</u> <u>page 584</u> , and <u>InterruptControl on page 585</u> for the in terrupts. Requirements for the individual interrupt source	ponding bit in the <u>In-</u> gister. See the reg- , <u>InterruptSource on</u> dividual specified in- urce facilities are	8 9 0 1

shall not have any side effects.

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found in <u>Section 13.4.1. "Facility Requirements." on page 519</u>. More than one of these facilities are required for Module form factors. **C13-19:** If a Module does not implement a particular bit in <u>Interrupt-Source</u>, <u>InterruptClearStatus</u>, and <u>InterruptControl</u> registers, it **shall** return 0b in response to a read of that bit. Writes to un-implemented bits

C13-19.1.1: A Module provides the IMxInt_L signal on all ports with an ⁸ implemented IB-ML. The IMxInt_L shall comply with the operations spec-⁹ ified in <u>Section 13.3.2.8, "IMxInt_L," on page 515</u>. 10

C13-20: A Module **shall** provide the corresponding functions within the <u>In-</u> <u>terruptClearStatus</u>, <u>InterruptSource</u>, and <u>InterruptControl</u> registers for those facilities which have IB-ML "Read" access through these registers and which are labeled as "**Req**" in the "Requirements" column of <u>Table</u> <u>126</u>.

Operation

The CME sets the respective <u>InterruptControl</u> bits for which it desires to have contribution to the assertion of **IMxInt_L**. Additionally, the CME writes 1b to all locations in the <u>InterruptClearStatus</u> register to clear the status of a detected transition.

Upon one or more events occurring, the MME sets the corresponding <u>In-</u> <u>terruptSource</u> register bits to reflect the present state of the interrupt generating events. A low-to-high or a high-to-low transition on an event sets its corresponding bit in the <u>InterruptClearStatus</u> register.

Once the CME detects that **IMxInt_L** is asserted, it queries the MME to discern which event happened. The CME reads the <u>InterruptSource</u> and <u>InterruptClearStatus</u> registers to get the current status of the sources and to know which event(s) has had a transition since the last <u>Interrupt-</u> <u>ClearStatus</u> write (Clear).

34 The InterruptClearStatus is a "Write 0b to clear, Write 1b has no effect" 35 register (See 13.6.7.1 on page 586). Thus, using the data returned from 36 the InterruptClearStatus command, the CME can write to Interrupt-37 <u>ClearStatus</u> to clear the contributions of those facilities to **IMxInt L**. The "Clear" operation to InterruptClearStatus only affects the Interrupt-38 <u>ClearStatus</u> register -- not the <u>InterruptSource</u> register. The Clear Interrupt 39 command does not affect the InterruptSource register. The Interrupt-40 Source register always reflects the present state of the interrupt gener-41 ating event. 42

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13.3.2.9 PRESENCE DETECTION		
	Module presence detection is provided by the IMxPRst s Backplane Connector (See <u>Section 11.5.3</u> , "IMxPRst," or	ignal on the <u>page 449</u>).
	A Module supports the IMxPRst signal on every Backpla implements.	ne Connector it
13.3.2.10 MODULEINFO DEVICE		-
	The ModuleInfo Device holds data that provide Vital Proc and other capability information necessary to allow the H agement of an IB Module. The ModuleInfo Device consis VPD device and zero or more extension VPD devices. Th vice always resides at the ModuleInfo Device address sp <u>121: Module IB-ML Slave Addresses</u>	luct Data (VPD) ardware Man- ats of one base be base VPD de- becified in <u>Table</u>
	See <u>Section 13.7, "xInfo Format," on page 598</u> for the for ture of records and fields in ModuleInfo.	mat and struc-
13.3.2.10.1 SPECIFIED READABLE A	REA	
	These areas are readable via IB and IB-ML.	
	ModuleInfo may be obtained using the Baseboard Manag General Signaling Interface (GSI) over QP1. It may also be IB-ML.	er (BM) and the e obtained using
13.3.2.10.2 MODULEPOWERINFO RE	CORD	
	The ModulePowerInfo record returns information about the sumption, startup characteristics, and power management a Module. See <u>Section 13.7.10</u> , "ModulePowerInfo Record for a list of Module power management attributes. See <u>S</u> "xInfo Format," on page 598 for the format, requirements, records and fields in ModulePowerInfo.	he power con- nt capabilities of <u>d." on page 622</u> <u>ection 13.7.</u> and structure of
13.3.2.10.3 IOCPMINFO		
	The IOCPMINFO record indicates the power management the IOCs associated with an IOUnit. If a Module contains and several IOCs, the information about all such IOCs ap tially in the IOCPMInfo record. See <u>Section 13.7</u> , " <u>xInfo F</u> <u>page 598</u> for the format, requirements, and structure of re in IOCPMINFO.	capabilities of multiple IOUnits opear sequen- <u>format," on</u> cords and fields
13.3.2.10.4 CHASSIS SPECIFIC NONV	OLATILE WRITABLE AREA	
	C13-21: IB-Modules shall implement 64 bytes of non-vol area in ModuleInfo out of which the first 32 bytes are reso Chassis. The Module may implement this writable area in	latile writable erved for the n the base VPD

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	device or in an extension VPD device. Also See <u>xlr</u> <u>13.7 on page 598)</u> for more information.	nfo Format (Section 1
	This area is readable and writable via IB-ML and IE	3. 3
	The data in these specified writable areas shall foll format. See <u>Table 159 OEM Record on page 628</u> .)	low the OEM Record 5
13.3.2.10.5 BASEBOARD MANAGER	SPECIFIC NONVOLATILE WRITABLE AREA	7
	C13-22: IB-Modules shall implement at least 64 bytable area in ModuleInfo out of which the first 32 bytes Chassis and the second 32 bytes are reserved for ager. It is recommended that Modules provide an abytes for OEM-software. The Module may implement the base VPD device or in an extension VPD device Format (Section 13.7 on page 598) for more inform	tes of non-volatile writ- es are reserved for the the Baseboard Man- additional 64 writable nt this writable area in te. Also See <u>xInfo</u> nation.
	This area is readable and writable via IB-ML and IE	3. 16 17
	The data in these specified writable areas shall foll format. See <u>Table 159 OEM Record on page 628</u> .)	low the OEM Record 18
13.3.2.11 MODULE PRIVATE ARE	AS	21
	 o13-6: For private use, IB-Modules may optionally or writable non-volatile data areas using IB-ML devisioned in Module IB-ML Slave Addresses (Section 1496). Also See xInfo Format (Section 13.7 on pages tion. These devices are readable via IB-ML and IB. 	implement read-only rices that are men- <u>Table 121 on page</u> <u>598)</u> for more informa- 26 27 28 29
13.4 MODULE FACILITIES		30
	Module Facilities provide for status and logical contr features of an InfiniBand Module. As outlined in oth chapter, in-band (Baseboard MADs) and out-of-bar paths are architected for many features; however, i cess is not the same. For example, a given facility m from both paths, but only one path is architecturally a section details which paths are architected for each For the Baseboard MAD path, facilities are accessed that are summarized in <u>Table 136 Baseboard MAD</u> <u>570</u> . For the IB-ML path, facilities are accessed usin summarized in <u>Table 140 MME Function Registers</u>	31ol of the managementber sections of thison d (IB-ML) accesson many cases, the ac-ay be read accessibleay be read accessibleallowed to write it. Thison facility.ad using "commands"commands on pageon page 584.

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C13-23: For each of the Module facilities described in this section, a "default" state is indicated. Upon a power-on or reset, a Module **shall** force the facilities to the default state values unless otherwise noted.

See <u>Section 13.4.1, "Facility Requirements," on page 519</u> for a list of requirements for all facilities by physical packaging and for a list of the applicable Baseboard commands and IB-ML registers that enable access to those facilities. Special considerations that apply to any of the access paths are noted in the individual facility description.

13.4.1 FACILITY REQUIREMENTS

13.4.1.1 MODULES

Table 126 summarizes the defined facilities for an InfiniBand Module.

C13-24: A Module containing an InfiniBand protocol-aware device **shall** provide those facilities labeled as "**Req**" in the "Requirements" column of <u>Table 126</u>.

C13-25: A Module containing an InfiniBand non-protocol-aware device **shall** provide those facilities labeled as "**Req**" in the "Requirements" column of <u>Table 126</u>. Only the "IB-ML" Access Path applies.

The "Requirement" column cells of the <u>Table 126</u> **shall** have the following definition:

- **Req** A Module **shall** implement the facility labeled **Req** in the "Requirement" column.
- Opt The Module may implement the facility labeled Opt in the "Requirement" column. If the facility is provided, the Module shall implement it in accordance with the provisions of this section. If the facility is not provided, the Module shall provide the default values for read accesses that are specified for the facility bit(s); write accesses shall not cause updates to occur from the default value for the facility.

The "Access Path" columns of <u>Table 126</u> **shall** have the following definitions:

- Baseboard, Read The ability to read the current state of the named facility through the noted command and associated response as detailed in <u>Table 136 Baseboard MAD Commands on</u> page 570 under "Response Data".
- Baseboard Access Write The ability to update the state of the facility with the value in a noted received command as detailed in Table 136 Baseboard MAD Commands on page 570 under "Request Data".

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	 IB-ML Access - Read - The ability to renamed facility through the noted register <u>MME Function Registers on page 584</u> (cessing the facility either through physice) E0h, or via the WriteMMERegister MMI 	ead the current state of the er as defined in <u>Table 140</u> under "Read Data" by ac- cal registers via address E Command	1 2 3 4
·	IB-ML Access - Write - The ability to u the named facility through the noted reg <u>140 MME Function Registers on page</u> accessing the facility either through phy E0h, or via the WriteMMERegister MMI	pdate the current state of gister as defined in <u>Table</u> 584 under "Write Data" by sical registers via address E Command	5 6 7 8 9
The defin	"Access Path" column cells of the <u>Table 12</u> hitions:	6 shall have the following	10 11
·	NP - The Module shall not permit accer path indicated by the column.	ess to the facility with the	12 13
	 NS - Access to the facility with the acce column is not specified. 	ess path indicated by the	14 15
	"cmd/reg" - If the cell contains the nam mand or an MME register as applicable the Module shall permit access to the f cated by the column. Note that in the ca a register, the access may be implement physical register via E0h or via the corr tion Write/ReadMMERegister MME corr	ne of a Baseboard com- e to the access path, then facility with the path indi- ase that the access path is inted either by using a responding split-transac- nmand via E4h.	17 18 19 20 21 22

Table 126 Module Facility Requirements

	ent		A	ccess Path	
Facility	uirem	Bas	eboard ^a	IE	3-ML
	Requ	Write	Read	Write	Read
Removal Control and S	tatus				
Module OKTR	Req	NP	<u>GetModuleStatus</u>	NP	RemovalControlStatus
Attention Status Change	Req	NS	NS	InterruptClearStatus, InterruptControl	InterruptClearStatus, InterruptControl, InterruptSource
Removal Status Change	Req	NP	NS	InterruptClearStatus, InterruptControl	InterruptClearStatus, InterruptControl, InterruptSource
MME_RTR	Opt	NS	GetModuleStatus	NP	RemovalControlStatus
MME_CTR	Opt	NS	GetModuleStatus	NP	RemovalControlStatus
CME_Force_OKTR	Req	NS	GetModuleStatus	RemovalControlStatus	RemovalControlStatus

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	ent	Access Path			
Facility	uiremo	Baseboard ^a		IE	B-ML
	Requ	Write	Read	Write	Read
CME_RTR	Req	NP	<u>GetModuleStatus</u>	RemovalControlStatus	RemovalControlStatus
CME_CTR	Req	NP	<u>GetModuleStatus</u>	RemovalControlStatus	RemovalControlStatus
<u>SW_CTR</u>	Req	SetModuleState	<u>GetModuleStatus</u>	RemovalControlStatus	RemovalControlStatus
<u>SW_RTR</u>	Req	SetModuleState	<u>GetModuleStatus</u>	RemovalControlStatus	RemovalControlStatus
Indicator Control and S	Status				
Module Identify	Req	NP	<u>GetModuleStatus</u>	NP	LEDTestStatus
Assert Identify	Req	SetModuleState	NS	LEDTestStatus	NS
MME Module Attention	Opt	NS	<u>GetModuleStatus</u>	NP	LEDTestStatus
CME Module Attention	Req	NP	<u>GetModuleStatus</u>	LEDTestStatus	LEDTestStatus
SW Module Attention	Req	<u>SetModuleAttention</u>	<u>GetModuleStatus</u>	NP	LEDTestStatus
Attention LED State	Req	NP	<u>GetModuleStatus</u>	NP	LEDTestStatus
Module Status LED State	Req	NP	<u>GetModuleStatus</u>	NP	LEDTestStatus
LED Enable	Req	NP	<u>GetModuleStatus</u>	LEDTestStatus	LEDTestStatus
LED Test	Req	NP	<u>GetModuleStatus</u>	NP	LEDTestStatus
Initiate LED Test	Req	SetModuleAttention	NS	LEDTestStatus	NP
Interrupt Control and S	tatus				
CME RTR Trap Timeout	Req	NP	<u>GetModuleStatus</u>	ModuleControlStatus	ModuleControlStatus
Power Converter Fault	Req	NP	<u>GetModuleStatus</u>	InterruptClearStatus, InterruptControl	InterruptClearStatus, InterruptControl, InterruptSource
Environmental Fault	Opt	NP	<u>GetModuleStatus</u>	InterruptClearStatus, InterruptControl	InterruptClearStatus, InterruptControl, InterruptSource
Functional Fault	Opt	NP	GetModuleStatus	InterruptClearStatus, InterruptControl	InterruptClearStatus, InterruptControl, InterruptSource
Hard Fault	Opt	NP	NS	NP	LEDTestStatus
Degraded Fault	Opt	NP	NS	NP	LEDTestStatus
Predictive Fault	Opt	NS	GetModuleStatus	InterruptClearStatus, InterruptControl	InterruptClearStatus, InterruptControl, InterruptSource
Cooling Non Crit	Opt	NP	GetModuleStatus	InterruptClearStatus, InterruptControl	InterruptClearStatus, InterruptControl, InterruptSource

Table 126 Module Facility Requirements

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	ent	Access Path			
Facility	uirem	Base	board ^a	IB-ML	
	Req	Write	Read	Write	Read
poling Crit	Opt	NP	GetModuleStatus	InterruptClearStatus, InterruptControl	InterruptClearStatus, InterruptControl, InterruptSource
ooling Non Recoverable	Opt	NP	<u>GetModuleStatus</u>	InterruptClearStatus, InterruptControl	InterruptClearStatus, InterruptControl, InterruptSource
oltage Crit	Opt	NP	<u>GetModuleStatus</u>	InterruptClearStatus, InterruptControl	InterruptClearStatus, InterruptControl, InterruptSource
oltage Non Recoverable	Opt	NP	GetModuleStatus	InterruptClearStatus, InterruptControl	InterruptClearStatus, InterruptControl, InterruptSource
<u> Aodule Power On</u>	Req	NP	<u>GetModuleStatus</u>	InterruptClearStatus, InterruptControl	InterruptClearStatus, InterruptControl, InterruptSource
Iodule Control and St	atus				•
wr Conv Redundancy	Opt	NP	GetModuleStatus	NP	ModulePower
<u>akeOnIB</u>	Opt	NP	NS	InterruptClearStatus, InterruptControl	InterruptClearStatus, InterruptControl, InterruptSource
VakeOnWRE	Opt	NP	NS	InterruptClearStatus, InterruptControl	InterruptClearStatus, InterruptControl, InterruptSource
MxInt L State	Req	NP	NS	NP	ModuleControlStatus
akeOnIB Enable	Opt	NP	NS	ModuleControlStatus	ModuleControlStatus
AxInt L Enable	Req	NP	NS	ModuleControlStatus	ModuleControlStatus
RE Enable	Opt	SetIOCPMControl	GetIOCPMControl	NP	ModuleControlStatus
VRE Status	Opt	SetIOCPMControl	GetIOCPMControl	NP	ModuleControlStatus

Table 126 Medule Eacility Pequirements

13.4.1.2 NON-MODULE DEVICES

Table 127 summarizes the facilities defined for "Non-Module" devices.

37 C13-26: An InfiniBand protocol-aware device mounted on a package other than an InfiniBand Module and supporting the optional Baseboard 38 Management Agent (BMA) shall provide those facilities labeled as "Req" 39 in the "Requirement" column of Table 127.

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The "Requirement" column cells of the <u>Table 127</u> **shall** have the following definition:

- Req A Non-Module shall implement the facility labeled Req in the "Requirement" column.
- Opt A Non-Module may implement the facility labeled Opt in the "Requirement" column. If the facility is provided, the Module shall implement it in accordance with the provisions of this section. If the facility is not provided, the Module shall provide the default values for read accesses that are specified for the facility bit(s); write accesses shall not cause updates to occur from the default value for the facility.

The "Access Path" columns of <u>Table 127</u> **shall** have the following definitions:

- Baseboard, Read The ability to read the current state of the named facility through the noted command and associated response as detailed in <u>Table 136 Baseboard MAD Commands on</u> <u>page 570</u> under "Response Data".
- Baseboard Access Write The ability to update the state of the facility with the value in a received noted command as detailed in <u>Table 136 Baseboard MAD Commands on page 570</u> under "Request Data".
- IB-ML Access Read The ability to read the current state of the named facility through the noted register as defined in <u>Table 140</u>
 <u>MME Function Registers on page 584</u> under "Read Data".
- **IB-ML Access Write** The ability to update the current state of the named facility through the noted register as defined in <u>Table</u> <u>140 MME Function Registers on page 584</u> under "Write Data".

The "Access Path" column cells of the <u>Table 127</u> **shall** have the following definitions:

- **NP** The Module **shall not** permit access to the facility with the path indicated by the column.
- **NS** Access to the facility with the access path indicated by the column is not specified.
- "cmd/reg" If the cell contains the name of a Baseboard command, or an MME register as applicable to the access path, then the Module shall permit access to the facility with the path indicated by the column. Note that in the case that the access path is

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a register, the access may be implemented either by using a physical register via E0h or via the corresponding split-transaction Write/ReadMMERegister MME command via E4h.

Table 127 Non-Module Device Facility Requirements

	ent	Access Path			
Facility	uirem	Baseboard		IE	3-ML
	Requ	Write	Read	Write	Read
Removal Control and S	atus		•		
Module OKTR	Opt	NP	<u>GetModuleStatus</u>	NP	RemovalControlStatus
Attention Status Change	Opt	NS	NS	InterruptClearStatus, InterruptControl	InterruptClearStatus, InterruptControl, InterruptSource
Removal Status Change	Opt	NP	NS	InterruptClearStatus, InterruptControl	InterruptClearStatus, InterruptControl, InterruptSource
MME_RTR	Opt	NS	GetModuleStatus	NP	RemovalControlStatus
MME_CTR	Opt	NS	GetModuleStatus	NP	RemovalControlStatus
CME_Force_OKTR	Opt	NS	GetModuleStatus	RemovalControlStatus	RemovalControlStatus
CME_RTR	Opt	NP	GetModuleStatus	RemovalControlStatus	RemovalControlStatus
CME_CTR	Opt	NP	<u>GetModuleStatus</u>	RemovalControlStatus	RemovalControlStatus
SW_CTR	Opt	SetModuleState	GetModuleStatus	RemovalControlStatus	RemovalControlStatus
<u>SW_RTR</u>	Opt	SetModuleState	GetModuleStatus	RemovalControlStatus	RemovalControlStatus
Indicator Control and S	tatus				
Module Identify	Opt	NP	<u>GetModuleStatus</u>	NP	LEDTestStatus
Assert Identify	Opt	SetModuleState	NS	LEDTestStatus	NS
MME Module Attention	Opt	NS	<u>GetModuleStatus</u>	NP	LEDTestStatus
CME Module Attention	Opt	NP	GetModuleStatus	LEDTestStatus	LEDTestStatus
SW Module Attention	Opt	SetModuleAttention	GetModuleStatus	NP	LEDTestStatus
Attention LED State	Opt	NP	GetModuleStatus	NP	LEDTestStatus
Module Status LED State	Opt	NP	GetModuleStatus	NP	LEDTestStatus
LED Enable	Opt	NP	<u>GetModuleStatus</u>	LEDTestStatus	LEDTestStatus
LED Test	Opt	NP	GetModuleStatus	NP	LEDTestStatus
Initiate LED Test	Opt	SetModuleAttention	NS	LEDTestStatus	NP
Interrupt Control and St	atus				
CME RTR Trap Timeout	Opt	NP	<u>GetModuleStatus</u>	ModuleControlStatus	ModuleControlStatus

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Table 127 Non-Module Device Facility Requirements

	ent	Access Path			
Facility	uirem	Baseboard			IB-ML
	Requ	Write	Read	Write	Read
Power Converter Fault	Opt	NP	GetModuleStatus	InterruptClearStatus, InterruptControl	InterruptClearStatus, InterruptControl, InterruptSource
Environmental Fault	Opt	NP	GetModuleStatus	InterruptClearStatus, InterruptControl	InterruptClearStatus, InterruptControl, InterruptSource
Functional Fault	Opt	NP	GetModuleStatus	InterruptClearStatus, InterruptControl	InterruptClearStatus, InterruptControl, InterruptSource
Predictive Fault	Opt	NS	GetModuleStatus	InterruptClearStatus, InterruptControl	InterruptClearStatus, InterruptControl, InterruptSource
Cooling Non Crit	Opt	NP	GetModuleStatus	InterruptClearStatus, InterruptControl	InterruptClearStatus, InterruptControl, InterruptSource
Cooling Crit	Opt	NP	<u>GetModuleStatus</u>	InterruptClearStatus, InterruptControl	InterruptClearStatus, InterruptControl, InterruptSource
Cooling Non Recoverable	Opt	NP	<u>GetModuleStatus</u>	InterruptClearStatus, InterruptControl	InterruptClearStatus, InterruptControl, InterruptSource
<u>Voltage Crit</u>	Opt	NP	<u>GetModuleStatus</u>	InterruptClearStatus, InterruptControl	InterruptClearStatus, InterruptControl, InterruptSource
Module Power On	Opt	NP	GetModuleStatus	InterruptClearStatus, InterruptControl	InterruptClearStatus, InterruptControl, InterruptSource
Module Control and Sta	atus				
Pwr Conv Redundancy	Opt	NP	GetModuleStatus	NP	ModulePower
<u>WakeOnIB</u>	Opt	NP	NS	InterruptClearStatus, InterruptControl	InterruptClearStatus, InterruptControl, InterruptSource
WakeOnWRE	Opt	NP	NS	InterruptClearStatus, InterruptControl	InterruptClearStatus, InterruptControl, InterruptSource
IMxInt L State	Opt	NP	NS	NP	ModuleControlStatus
WakeOnIB Enable	Opt	NP	NS	ModuleControlStatus	ModuleControlStatus
IMxInt L Enable	Opt	NP	NS	ModuleControlStatus	ModuleControlStatus
WRE Enable	Opt	SetIOCPMControl	GetIOCPMControl	NP	ModuleControlStatus
WRE Status	Opt	SetIOCPMControl	GetIOCPMControl	NP	ModuleControlStatus

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13.4.2 REMOVAL CONTROL/ST	ATUS FACILITY DESCRIPTIONS	1
13.4.2.1 MODULE_OKTR		2
	Module_OKTR (Module OK to Remove) is a bit facility that the Module controls to provide a summary of the defined "Clear to Remove" facilities.	3 4
	The Module_OKTR facility has the following definition:	5 6
	0b = Module is not OK to Remove 1b = Module is OK to Remove (default)	7 8 9
	C13-27: The Module shall set the Module_OKTR bit to 1b if all of the following are set to 1b:	10 11 12
	• <u>MME_CTR</u>	13
	• <u>CME_CTR</u>	14
	• <u>SW CTR</u>	15
13 4 2 2 ATTENTION STATUS CI	HANGE	10
	Attention_Status_Change is a bit facility that the Module controls to in- dicate that a change of state has occurred on any facility bits that con- tribute to the state of the Attention LED. This bit includes state status change for the following facilities:	18 19 20 21 22
	<u>MME Module Attention</u>	23
	<u>CME Module Attention</u>	24
	SW Module Attention	25
	The following bits are included in the Attention_Status_Change facility:	26 27
	InterruptSource.Attention_Status_Change	28
	 InterruptControl.Attention_Status_Change 	29
	 InterruptClear/Status.Attention_Status_Change 	31
	These bits are associated as part of the control and status function that contributes to the backplane interrupt signal as defined in <u>13.3.2.8</u> . <u>IMxInt L on page 515</u> .	32 33 34
	The InterruptSource.Attention_Status_Change indicates whether any of the attention conditions are presently active.	35 36 37
	0b = MME_Module_Attention, CME_Module_Attention, and SW_Module_Attention are all presently 0b (default).	38 39
	1b = One or more of the MME_Module_Attention, CME_Module_Attention, or SW_Module_Attention bits are presently 1b.	40 41 42

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The InterruptStatus.Attention_Status_Change bit indicates the current interrupt condition:

0b = Attention Status bits have not changed since last Interrupt Clear. (default) 1b = At least one Attention Status bit has changed states since last Interrupt Clear.

13.4.2.3 REMOVAL_STATUS_CHANGE

Removal_Status_Change is a bit facility that the Module controls to indi-7 cate that a change of state has occurred on any facility bits of the Module 8 Removal Status register so as to contribute to the backplane interrupt 9 signal as defined in Section 13.3.2.8, "IMxInt L," on page 515. This bit includes state status change for the following facilities:

	11
<u>Module_OKTR</u>	12
• <u>MME_RTR</u>	13
• <u>MME_CTR</u>	14
CME Force OKTR	15
• CME RTR	16
• CME CTR	17
	10
• <u>SW CIR</u>	20
• <u>SW_RTR</u>	21
The following bits are included in the Removal_Status_Change facility:	22
InterruptSource Removal Status Change	23
InterruptControl Romoval Status Change	24
InterruptControl.Removal_Status_Change	25
 InterruptClear/Status.Removal_Status_Change 	26
These bits are associated as part of the control and status function that	27
Section 13.3.2.8 "IMVInt 1." on page 515	28
	29
The InterruptSource.Removal_Status_Change bit indicates the current in-	30
terrupt condition:	32
0b = All Module Removal Status bits are presently 0b (default)	33
1b = One or more of the Module Removal Status bits are presently 1b.	34
	35
The InterruptStatus.Removal_Status_Change bit indicates the current in-	36
terrupt condition:	37
0b = The Module Removal Status bits have not changed since last interrupt clear	38
(default)	39
1b = At least one bit in the Module Removal Status bits has changed states since last interrupt clear.	40
	41
	42

13.4.2.4 MME_RTR		1
	MME_RTR (MME Request to Remove) is a bit facility that the MME con-	2
	ware, and the CME to release the Module. See <u>Section 13.3.2.4</u> ,	3
	"Graceful Hot Removal," on page 503.	4
	The facility has the following definition:	6
	0h – No Request has been Initiated, or Request has been removed (default)	7
	1b = A Request is Pending.	8 9
	INTERRUPT EFFECTS	10
	bit has on the IMxInt_L signal.	11 12
13.4.2.5 MME CTR		13
_	MME_CTR (MME Clear to Remove) is a bit facility that the MME controls	14
	to indicate that Module removal is allowed. See <u>Section 13.3.2.4.</u>	15 16
	"Graceful Hot Removal," on page 503 for a description on potential uses of this facility.	17
		18
	The MME_CTR facility has the following definition:	19
	0b = Claimed	20
	1b = Not Claimed (default)	22
	INTERRUPT EFFECTS	23
	See <u>13.4.2.3 Removal Status Change on page 527</u> for implications this bit has on the IMxInt_L signal.	24
13426 CME FORCE OKTR		26
	CME Force OKTD is a bit facility that the CME controls to indicate that	27
	the Module is OK to Remove independent of the states of SW CTR.	28
	MME CTR, and CME CTR.	29
	The CME_Force_OKTR facility has the following definition:	31
	0b = Not forcing OKTR (default)	32
	1b = Force OKTR	33
13.4.2.7 CME_RTR		34
	CME_RTR (CME Request to Remove) is a bit facility that the CME con-	36
	trols to indicate that the CME is requesting the Baseboard Manager and	37
	order to enable removal of the Module.	38
	The CME RTR facility has the following definition:	39
		40 74
	0b = Claimed	42

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	1b = Not Claimed (default)		•
	INTERRUPT EFFECTS		1
	See <u>13.4.2.3 Removal Status Change on page 527</u> f bit has on the IMxInt_L signal.	or implications this	2 3 4
13.4.2.8 CME CTR			5
	CME_CTR (CME Clear to Remove) is a bit facility that to indicate that the CME has performed all Chassis are	t the CME controls	6 7
	that would allow the Module to be removed.	becine operations	8
	The CME_CTR facility has the following definition:		9 10
	0b = Not Clear to Remove		11
	1b = Clear to Remove (default)		13
	See 13.4.2.3 Removal Status Change on page 527 f	or implications this	14
	bit has on the IMxInt_L signal.		15
13429 SW CTR			16
13. 4 .2.3 GW_CTK	SW CTR (Software Clear to Remove) is a bit facility t	hat the Baseboard	18
	Manager controls to indicate that the Module is claime	d such that it is not	19
	OK to Remove this Module. See <u>Section 13.3.2.4, "Gr</u>	raceful Hot Re-	20
	moval, on page 505 for further description on the use	e of the this facility.	21
	The SW_CTR facility has the following definition:		22
	0b = Claimed		24
	1b = Not Claimed (default)		25
	INTERRUPT EFFECTS	in the line (in the line)	26
	See <u>13.4.2.3 Removal Status Change on page 527</u> f bit has on the IMxInt L signal	or implications this	27
			28
13.4.2.10 SW_RTR			23 30
	SW_RTR (Software Request to Remove) is a bit facili	ity that the Base-	31
	tions with the interested software entities to determine	e when a quiescent	32
	state can be achieved. See Section 13.3.2.4, "Gracefu	Il Hot Removal," on	33
	page 503 for further description on the use of this faci	lity.	34
	The SW_RTR facility has the following definition:		35
	0b = No Request has been Initiated, or Request has been ren	noved (default)	37
	1b = A Request is Pending.		38
	INTERRUPT EFFECTS		39
	See 13.4.2.3 Removal Status Change on page 527 f	or implications this	40 41
	bit has on the IMxInt_L signal.		42

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13.4.3 INDICATOR CONTRO	OL /S TATUS FACI	LITY DESCRIPTIONS	1	1
13.4.3.1 MODULE_IDENTIFY			2	2
	Module_lo defined in by Basebo	lentify is a bit facility that provides st Section 13.3.2.6.7, "Module Identify," ard Manager software or the CME.	atus that the LED function ³ <u>on page 513</u> was initiated 4 5	\$
	The Modu	le_ldentify facility has the following	definition: 6) 7
	0b = Not 1b = Perf	performing Identify (default) orming Identify	8	}
13.4.3.2 ASSERT_IDENTIFY			1	1
	Assert_Id	entify is a bit facility that the Basebo	bard Manager controls	2
	which initia <u>"Module Ic</u>	ates or rearms the LED function definention definention definention definentiation definentiation definentiation definentiation definentiation definentiation definentiation defined and the definition definition defined and the definition definition defined and the definition defined and the definition de	ned in <u>Section 13.3.2.6.7.</u> 1 1	3
	The Asse	The Assert_Identify facility has the following definition:		
	0b = Stop 1b = Initia equ BASEBOAR	the Module Identify function. (default) te the Module Identify on the Attention LED al to IdentifyPeriod. See <u>Table 128: Identify</u>	1 and repeat it for a period of time Function Period 1	6 7 8 9
	Read oper are not spo Identify fur	ations to the Assert_Identify facility ecified. The <u>Module Identify</u> facility p action. (See <u>Section 13.4.3.1</u>).	v using Baseboard MADs provides the state of the 2	20 21 22
	IB-ML Aco	ess - Read	2	23 24
	Read oper ified. The <u>t</u> tion. (See	ations to the Assert_Identify facility <u>Module Identify</u> facility provides the <u>Section 13.4.3.1</u>).	using IB-ML are not spec- 2 state of the Identify func- 2 2 2	25 26 27 28
			2	29
	Table	128 Identify Function Period	3	30 21
Term	Period	Comments	3	32

Term	Period	Comments
IdentifyPeriod	8s +/- 25%	Once <u>Assert Identify</u> facility been invoked, initiate the Mod- ule Identify on the Attention LED and repeat it for this amount of time.

13.4.3.3 MME_MODULE_ATTENTION

MME_Module_Attention is a bit facility that the MME controls to assert38the Attention LED if the LEDs are enabled with LED Enable (See Section3913.4.3.8 on page 532).40

The **MME_Module_Attention** facility has the following definition:

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0b = No Attention condition present (default) 1 1b = Attention condition present 2 **INTERRUPT EFFECTS** 3 See 13.4.2.3 Removal Status Change on page 527 for implications this 4 bit has on the **IMxInt** L signal. 5 Although MME Registers may not be available if a Module's DC-DC con-6 verter is OFF, if V_{Aux} is available, the Module's Attention LED maintains 7 its state (ON or OFF). It reflects the state it had prior to Module's DC-DC 8 going OFF. For example, the Attention LED may reflect a DC-DC con-9 verter failure. 10 11 13.4.3.4 CME_MODULE_ATTENTION 12 CME_Module_Attention is a bit facility that the CME controls to assert 13 the Attention LED if the LEDs are enabled with LED Enable (See Section 14 13.4.3.8 on page 532). 15 The **CME_Module_Attention** facility has the following definition: 16 17 0b = No Attention condition present (default) 18 1b = Attention condition present 19 **INTERRUPT EFFECTS** 20 See <u>13.4.2.3 Removal Status Change on page 527</u> for implications this 21 bit has on the IMxInt_L signal. 22 23 13.4.3.5 SW MODULE ATTENTION 24 SW_Module_Attention is a bit facility that the Baseboard Manager con-25 trols to assert the Attention LED given LEDs are enabled with LED Enable (See Section 13.4.3.8 on page 532). 26 27 The SW_Module_Attention facility has the following definition: 28 29 0b = No Attention condition present (default) 1b = Attention condition present 30 **INTERRUPT EFFECTS** 31 See 13.4.2.3 Removal Status Change on page 527 for implications this 32

13.4.3.6	ATTENTION	LED	STATE
10111010	/		

 Attention_LED_State is a facility which reflects the current state of the
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 Attention LED.
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 The Attention LED.
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The **Attention_LED_State** facility has the following definition:

 00b = OFF (Neither CME, MME, nor the Baseboard Manager has indicated an attention event and CME_RTR_Trap_Timeout is 0b.)
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bit has on the **IMxInt_L** signal.

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	01b = ON (Either CME, MME, or the Baseboard Manager has in event OR <i>CME_RTR_Trap_Timeout is 1b</i> .) 10b = Blink (indicates Module Identify)	ndicated an attention 1
	11b = reserved	3
		4
13.4.3.7 MODULE_STATUS_LED	_Ѕтате	5
	Module_Status_LED_State is a facility which reflects the Module Status LED.	ne current state of 6 7
	The Module_Status_LED_State facility has the followi	ng definition: 9
	00b = OFF	1(
	01b = ON	11
	10b = BLINK 11b - reserved	14
		14
13.4.3.8 LED_ENABLE		15
	LED Enable is a bit facility indicating to the CME and t	o the Baseboard 10
	Manager whether the LEDs are enabled for operation. T	he CME has write 17
	access to this bit.	18
	The LED Enable facility has the following definition:	19
		2'
	0b = LEDs are always OFF. 1b - LEDs follow the states detailed in Section 13.3.2.6. "Modul	e Indicators (LEDs) " 22
	on page 508. (default)	<u>2</u>
		24
		25
13.4.3.9 LED_IEST		20
	LED_Test is a bit facility indicating the state of the func	tion defined in 21
	board Manager.	29
		30
	The LED_Test facility has the following definition:	31
	0b = LED Test function is not in progress.	32
	1b = LED Test function is in progress.	33
13.4.3.10 INITIATE_LED_TEST		34
	Initiate_LED_Test is a bit facility that either the Basebo	pard Manager or 36
	the CME controls to initiate or rearm the LED function of Section 13.3.2.6.6. "LED Test." on page 513	letined in 37
	<u>Section 13.3.2.0.0, LED rest, Or page 313</u> .	38
	The Initiate_LED_Test facility has the following definiti	on: 39
	0 = Write of 0b has no effect. Once the test starts, it goes to con	npletion.
	1 = Initiate the LED Test on both Green and Attention LEDs.	- 4' /
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BASEBOARD ACCESS - READ

Read operations to the **Initiate_LED_Test** facility using Baseboard MADs are not specified. The <u>LED_Test</u> facility provides the state of the **LED Test** function. (See <u>Section 13.4.3.9</u>).

IB-ML ACCESS - READ

Read operations to the **Initiate_LED_Test** facility using IB-ML are not architected. The <u>LED Test</u> facility provides the state of the **LED Test** function. (See <u>Section 13.4.3.9</u>).

13.4.4 INTERRUPT CONTROL/STATUS FACILITY DESCRIPTIONS

13.4.4.1 CME_RTR_TRAP_TIMEOUT

CME_RTR_Trap_Timeout is a bit facility that the CME controls to indicate that the CME has timed-out while waiting for the **SW_RTR** to be set in acknowledgement to a CME Request to Remove (**CME_RTR**) *BMTrap*.

The CME **may** choose to over-ride the Baseboard Manager using the **CME_Force_OKTR** facility (See <u>13.4.2.6 CME_Force_OKTR on page</u> <u>528</u>).

Implementation Note

This time-out is an indication that the Baseboard Manager responsible for receiving the BMTrap may not be operating correctly. This time-out does not mean that the interested software entities have taken too long to respond with a **SW_CTR** because the Baseboard Manager is supposed to acknowledge the **BMTrap** before it queries the other interested software entities for their "vote". See <u>Section 13.3.2.4, "Graceful Hot Removal," on page 503</u>.

Although not directly related to Module OK To Remove, this time-out indicates that the **SW_RTR** and the **SW_CTR** is not set, and therefore, the Module is not OK To Remove from the Software's point of view. See <u>Section 13.3.2.4, "Graceful Hot Removal," on page 503</u>.

The **CME_RTR_Trap_Timeout** facility has the following definition:

0b = No time-out present (default)
0b = No time-out present (default)

1b = Time condition present

13.4.4.2 POWER_CONVERTER_FAULT

Power_Converter_Fault is a bit facility that the Module controls to indicate that the Module has turned off its main power converter(s) due to a power fault condition -- not in response to VBxEn_L negation, and not in response to an IB Power Down Request.39404041414242

The following bits are included in the **Power_Converter_Fault** facility: 2 InterruptSource.Power_Converter_Fault 3 InterruptControl.Power Converter Fault • 4 InterruptClear/Status.Power Converter Fault 5 These bits are associated as part of the control and status function that 6 contributes to the backplane interrupt signal as defined in 7 Section 13.3.2.8, "IMxInt L," on page 515. 8 9 The InterruptSource.Power Converter Fault bit has the following def-10 inition: 11 12 0b = No fault condition exists (default) 1b = Module power converter(s) off due to a fault condition 13 14 **BASEBOARD ACCESS - READ** 15 16 Architectural Note 17 18 If the Module DC-DC converter is off, it is very likely that its IB port is 19 non-functional and thus renders the Baseboard MAD access as moot. 20 However, to facilitate redundant power designs or designs that may use 21 alternate power sources, this access is architecturally provided. 22 23 **13.4.4.3 ENVIRONMENTAL FAULT** 24 **Environmental Fault** is a facility that the Module controls to indicate that 25 an environmental condition other than voltage or cooling conditions has 26 occurred. 27

The following bits are included in the **Environmental_Fault** facility:

- InterruptSource.Environmental_Fault
- InterruptControl.Environmental_Fault
- InterruptClear/Status.Environmental_Fault

These bits are associated as part of the control and status function that contributes to the backplane interrupt signal as defined in Section 13.3.2.8, "IMxInt L," on page 515.

The InterruptSource.Environmental Fault bit has the following definition:

- 39 0b = Module is not in an environmental fault condition (default) 40 1b = Module has detected an environmental fault condition.

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BASEBOARD ACCESS - READ

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	Architectural Note	2 3
	If the Module DC-DC converter is off, it is very likely that its IB port is non-functional and thus renders the Baseboard MAD access as moot. However, to facilitate redundant power designs or designs that may use alternate power sources, this access is architecturally provided.	4 5 6 7
13 4 4 4 FUNCTIONAL FAULT		8
13.4.4.4 TONCHONAL_TAULT	Functional_Fault is a bit facility that the Module controls to indicate that a Module specific functional fault condition was detected. This bit includes state from the following facilities:	9 10 11 12
	Hard Fault	13
	Degraded Fault	14
	The following hits are associated with the Functional Fault facility:	15
	The following bits are associated with the Functional_Functionaly.	10
	InterruptSource.FUNCTIONAL_FAULT	18
	InterruptControl.FUNCTIONAL_FAULT	19
	InterruptClear/Status.FUNCTIONAL_FAULT	20
	These bits are associated as part of the control and status function that contributes to the backplane interrupt signal as defined in Section 13.3.2.8 "IMxInt 1." on page 515	21 22
		23
	The InterruptSource.Functional_Fault bit has the following definition:	24
	0b = Module is not in a functional fault condition (default)	26
	1b = Module has detected a functional fault condition.	27
13.4.4.5 HARD_FAULT		28
	HARD_FAULT is a bit facility that the Module controls to indicate that a	29
	Module specific functional fault condition that renders the Module inoper-	31
	able was delected.	32
	The HARD_FAULT bit has the following definition:	33
	Ob - Module is not in a hard functional fault condition (default)	34
	1b = Module has detected a hard functional fault condition.	35
13.4.4.6 DEGRADED_FAULT		36
	Degraded Fault is a bit facility that the Module controls to indicate that a	<i>১।</i> ३८
	Module specific functional fault condition was detected but the Module is	39
	capable to functioning with degrade capabilities.	40
	The Degraded Fault hit has the following definition:	41
	The begraded_r and bit has the following definition.	42

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Ob = Module is not in a degraded functional fault condition (default)

1b = Module has detected a degraded functional fault condition.

Architectural Note

The **Degraded Fault** bit is intended to indicate that degraded faults such as loss of cache memory due to excessive ECC error and loss of power converter redundancy had occurred. Other error examples are certainly possible.

13.4.4.7 PREDICTIVE FAULT

12 Predictive_Fault is a bit facility that the Module controls to indicate that a 13 non-critical functional event or condition has occurred that may eventually lead to a critical failure. 14

The following bits are associated with the **Predictive_Fault** facility:

16 InterruptSource.Predictive_Fault 17 18 InterruptControl.Predictive Fault 19 InterruptClear/Status.Predictive_Fault 20 These bits are associated as part of the control and status function that 21 contributes to the backplane interrupt signal as defined in 22 Section 13.3.2.8, "IMxInt L," on page 515. 23 24 The InterruptSource.Predictive Fault bit has the following definition: 25 Ob = Module is functioning optimally. (default) 26 1b = Module is in a degraded state. 27 28

BASEBOARD ACCESS - WRITE

The setting of the InterruptSource.Predictive Fault bit through Infini-Band link operations is Module specific.

13.4.4.8 COOLING NON CRIT

Cooling_Non_Crit is a bit facility that the Module controls to indicate a temperature sensor(s) on the Module has crossed its Module-specific warning temperature threshold but is still operating. 36

The following bits are associated with the **Cooling_Non_Crit** facility:

- InterruptSource.Cooling_Non_Crit 39
- InterruptControl.Cooling Non Crit
- InterruptClear/Status.Cooling_Non_Crit

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	These bits are associated as part of the control and sta contributes to the backplane interrupt signal as defined <u>Section 13.3.2.8, "IMxInt L," on page 515</u> .	tus function that 1 in 2				
	The InterruptSource.Cooling Non Crit bit has the fo	3 Ilowina definition: 4				
	Ob Module Temperature and Caeling Status are normal (data)					
	1b = Module Temperature has exceeded its warning threshold o	r Module cooling				
	apparatus is not running optimally	/ 8				
13.4.4.9 COOLING_CRIT		9				
	Cooling_Crit is a bit facility that the Module controls to a ature sensor(s) on the Module has crossed its Module-s temperature threshold and that the Module has turned o verter(s).	indicate a temper- 1 specific critical 1 off its Power Con- 1 1				
	The following bits are associated with the Cooling_Crit	t facility: 1				
	InterruptSource.Cooling_Crit	1				
	InterruptControl.Cooling_Crit	1				
	 InterruptClear/Status.Cooling_Crit 	1				
	These bits are associated as part of the control and sta contributes to the backplane interrupt signal as defined <u>Section 13.3.2.8</u> , "IMxInt L," on page 515.	tus function that 1 in 2				
	The InterruptSource.Cooling_Crit bit has the followin	2 g definition: 2				
	0b = Module Temperature and Cooling Status are not critical. (de 1b = Module Temperature has exceeded its critical threshold and verter is off.	efault) 2 d Module Power Con- 2 2				
	BASEBOARD ACCESS - READ					
	Architectural Note	23				
	As the Module DC-DC converter is off, it is very likely to non-functional and thus renders the Baseboard MAD a However, to facilitate potential design options that may power sources, this access is architecturally provided.	that its IB port is access as moot. y use alternate				
13.4.4.10 COOLING_NON_RECO	13.4.4.10 COOLING_NON_RECOVERABLE					
	Cooling_Non_Recoverable is a bit facility that the Moo dicate that the temperature on the Module has gone over cific non-recoverable temperature threshold and that the turned off its power converter(s). In addition, the Module anymore because of a potential damage due to excess Once the Module reaches this temperature, the status in	dule controls to in- er its Module-spe- e Module has ile is not reliable ive over-heating. dication of this fa-				

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	cility will be permanently asserted (even through pouse a Fuse.)	wer sequences). (e.g. 1
	The following bits are associated with the Cooling_ I cility:	Non_Recoverable fa- 3 4
	 InterruptSource.Cooling_Non_Recoverable 	5
	 InterruptControl.Cooling_Non_Recoverable 	6
	 InterruptClear/Status.Cooling_Non_Recove 	rable 8
	These bits are associated as part of the control and contributes to the backplane interrupt signal as defined as the section 13.3.2.8, "IMxInt L," on page 515.	d status function that 9 ined in 1
	The InterruptSource.Cooling_Non_Recoverable definition:	bit has the following 1 1
	0b = Module Temperature and Cooling Status are not non- 1b = Module Temperature has exceeded its Non-recoverab Power Converter is off, and this Module is not reliable	recoverable. (default) 1 ble threshold, Module 1 e anymore.
	BASEBOARD ACCESS - READ	1
	Architectural Note	2
	As the Module DC-DC converter is off, it is very lik non-functional and thus renders the Baseboard M	xely that its IB port isAD access as moot.
13.4.4.11 Voltage_Crit		2
	Voltage_Crit is a bit facility that the Module controls monitoring device on the Module has crossed its M voltage threshold and that the Module has turned o verter(s).	s to indicate a voltage 2 odule-specific critical 2 off its power con-2
	The following bits are associated with the Voltage_	Crit facility: 3
	InterruptSource.Voltage_Crit	3
	 InterruptControl.Voltage_Crit 	3
	 InterruptClear/Status.Voltage_Crit 	3
	These bits are associated as part of the control and contributes to the backplane interrupt signal as defined as the section 13.3.2.8, "IMxInt_L," on page 515.	d status function that 3 ined in 3
	The InterruptSource.Voltage_Crit bit has the follo	owing definition: 3
	0b = Module Voltage is within range. (default)	4
	1b = Module Voltage is out of range and the Module Power	r Converter is off.

BASEBOARD ACCESS - READ

Architectural Note

As the Module DC-DC converter is off, it is very likely that its IB port is non-functional and thus renders the Baseboard MAD access as moot. However, to facilitate potential design options that may use alternate power sources, this access is architecturally provided.

13.4.4.12 VOLTAGE_NON_RECOVERABLE

Voltage_Non_Recoverable is a bit facility that the Module controls to indicate that the voltage on the Module has gone over its Module-specific non-recoverable voltage threshold and that the Module has turned off its power converter(s). In addition, the Module is not reliable anymore because of a potential damage due to excessive voltage. Once the Module reaches this threshold, the status indication of this facility will be permanently asserted (even through power sequences). (e.g. use a Fuse.)

The following bits are associated with the **Voltage_Non_Recoverable** facility:

- InterruptSource.Voltage_Non_Recoverable
- InterruptControl.Voltage_Non_Recoverable
- InterruptClear/Status.Voltage_Non_Recoverable

These bits are associated as part of the control and status function that contributes to the backplane interrupt signal as defined in <u>Section 13.3.2.8, "IMxInt L," on page 515</u>.

The InterruptSource.Voltage_Non_Recoverable bit has the following definition:

- 0b = Module Voltage is not non-recoverable. (default)
- 1b = Module Voltage has exceeded its non-recoverable threshold, Module Power Converter is off, and this Module is not reliable anymore.

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BASEBOARD ACCESS - READ

Architectural Note

As the Module DC-DC converter is off, it is very likely that its IB port is non-functional and thus renders the Baseboard MAD access as moot.

13.4.4.13 MODULE_POWER_ON

Module_Power_On is a bit facility indicating whether one or more of the Module power converter(s) are enabled and providing output voltage and current within Module specific parameters.

The following bits are included in the Module_Power_On facility:

- InterruptSource.Module_Power_On
- InterruptControl.Module_Power_On
- InterruptClear/Status.Module_Power_On

These bits are associated as part of the control and status function that contributes to the backplane interrupt signal as defined in <u>Section 13.3.2.8, "IMxInt L," on page 515</u>.

The InterruptSource.Module_Power_On bit has the following definition:

0b = All Module DC-DC Converters are Off

1b = At least one DC-DC Converter is On and providing Module specified power

Architecture Note

If only one power converter is present, the bit represents that state of that converter; if more than one converter is present in a redundant arrangement, this bit conveys if any of the converters are ON.
BASEBOARD ACCESS - READ

	Architectural Note	3
	If the Module DC-DC converter is off, it is very likely that its IB port is non-functional and thus renders the Baseboard MAD access as moot. However, to facilitate redundant power designs or designs that may use alternate power sources, this access is architecturally provided.	4 5 6 7
13.4.5 MODULE CONTROL/STAT	US FACILITY DESCRIPTIONS	8 0
13.4.5.1 Pwr_Conv_Redundance	CY	10
	Pwr_Conv_Redundancy is a facility controlled by the Module to indicate the redundancy state of its power converter function.	11 12
	The Pwr_Conv_Redundancy facility has the following definition:	13 14
	00b = non-redundant converter	15
	01b = redundant converter is operating fully redundant	16
	10b = redundant converter is operating with degraded redundancy	17
	11b = redundant converter is operating non-redundant	18
13.4.5.2 WAREONIB		19
	WakeOnIB is a bit facility controlled by the Module to indicate that the last	20
	wake-up was caused by a wakeOnib event. (Beacon delected.)	21
	The WakeOnIB facility has the following definition:	22
		23
	0b = Last wake-up was not due to WakeOnIB (default)	24
	1b = Last wake-up was due to WakeOnIB	25
		26
13.4.5.3 WAKEONWRE		27
	WakeOnWRE is a bit facility controlled by the Module to indicate that the	28
	last wake-up was caused by a wake-Request-Event.	29
	The WakeOnWRE facility has the following definition:	30
		31 22
	0b = Last wake-up was not due to WRE (default)	3Z
	1b = Last wake-up was due to WRE	24
		34
13.4.5.4 IWIXINI_L_STATE		36
	IMxInt_L_State is a bit facility controlled by the Module to indicate the cur-	37
	rent state of the INIXINT_L pin.	38
	The IMxInt L State facility has the following definition:	30
		40
	0b = IMxInt_L signal is not asserted; it is at a high voltage.	41
	1b = IMxInt_L signal is asserted; it is at a low voltage.	42

13.4.5.5 WAKEONIB_ENABLE		1
	WakeOnIB_Enable is a bit facility controlled by the CME to control and indicate whether the power controller on the Module will allow wake-up based on a WakeOnIB event. (Beacon detected.)	2 3 4 5
	The WakeOnIB_Enable facility has the following definition:	6
	0b = wake-up due to WakeOnIB is Disabled 1b = wake-up due to WakeOnIB is Enabled (default)	7 8 9 10
	Implementation Note	11 12
	Use of this facility is not recommended and is subject to removal in future versions of the specification.	13 14
	If it is used to disable the detection of beaconing events while the module is the M _{Standby} state (which was established by in-band Power Management operations), the awakening anticipated by the in-band Power Manager through beaconing will not occur. Depending on the system design, this may result in service replacement of the module as being faulty that would otherwise not be warranted.	15 16 17 18 19 20
13.4.5.6 IMXINT L ENABLE		21
	IMxInt_L_Enable is a bit facility controlled by the CME to control and in- dicate whether the Module will assert IMxInt_L based on <i>InterruptStatus</i> and <i>InterruptControl</i> registers.	23 24 25
	The IMxInt_L_Enable facility has the following definition:	26 27
	0b = Will not assert IMxInt_L (default) 1b = Will assert IMxInt_L based on <i>InterruptControl</i> and <i>InterruptStatus</i> registers	28 29 30
13.4.5.7 WRE_ENABLE		31
	WRE_Enable (Wake Request Event Enable) is a bit facility controlling whether an IOC is enabled to generate a Wake Request Event defined in <u>Section 14.2.5.1, "Wake Request Event," on page 635</u> .	32 33 34
	This bit is "sticky" and is not to be affected by resets (power-on or IMx-PRst) or other power state transitions; thus, the default state of this facility is undefined. Power Management software must explicitly establish the initial state through Baseboard commands. With the sticky nature defined, this facility is considered to be run on auxiliary power.	35 36 37 38 39
	If a Module supports Power Management (<i>ModulePowerInfo.ModulePM-Capability.IsPowerManagementSupported</i> = 1b) and additionally sup-	40 41 42

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	ports WRE generation as indicated in its IOCPMInf (any of WREisIDozeSupported, WREisINapSuppor Supported, WREisIStandbySupported = 1b), it sha WRE_Enable facility.	o.IOCPmCapability rted, WREisISleep- II provide the 3
	The WRE_Enable facility has the following definition	on: 5
	0b = WREs Not Enabled	6 7
13 / 5 8 WPE STATUS	ID = WRES Enabled	8
13.4.3.0 WILL_STATUS		1
	WRE_Status (Wake Request Event Status) is a bit whether an IOC has generated a Wake Request Event Section 14.2.5.1, "Wake Request Event," on page 6 setting of <u>WRE_Enable</u> (See <u>Section 13.4.5.7</u>).	facility indicating vent defined in <u>35</u> independent of the 1
	This bit is "sticky" and is not to be affected by reset PRst) or other power state transitions; thus, the defa is undefined. Power Management software must ex- initial state through Baseboard commands. With the this facility is considered to be run on auxiliary pow	s (power-on or IMx- ault state of this facility cplicitly establish the sticky nature defined, er.
	If a Module supports Power Management (Module Capability.IsPowerManagementSupported = 1b) an ports WRE generation as indicated in its IOCPMInf (any of WREisIDozeSupported, WREisINapSuppor Supported, WREisIStandbySupported = 1b), it sha WRE_Status facility.	PowerInfo.ModulePM- 2 ad additionally sup- 2 o.IOCPmCapability 2 rted, WREisISleep- 2 II provide the 2
	The WRE_Status facility has the following definition	n: 2
		2
	0b = WRE not present	2
	ID = WRE present	2
13.5 CHASSIS FEATURES		3
		3
13.5.1 CHASSIS FEATURE REC	UIREMENTS	3
	This section defines the required and optional feature of Chassis which will accept InfiniBand Modules. The quired ensure interoperability between such a Chas fined by this specification.	ires for various types 3 hose indicated as re-3 ssis and Modules de-3 3
	The column cells of Table 129 shall have the follow	ving definition: 3
	 Req - A Chassis shall implement the facility "Requirement" column. 	v labeled Req in the 4 4 4

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	 Rec - The Chassis the "Requirement" of provided. If the feat provisions of the feat 	may implement column. It is reco ure is provided, t ature description	the features la mmended tha he Chassis s section.	abeled Rec in at the feature be hall follow the
	 Opt - The Chassis r "Requirement" colu shall follow the pro 	nay implement th mn. If the feature visions of the fea	ne features la e is provided, iture descripti	beled Opt in the the Chassis on section.
	 N/A - The feature is dressed. 	s not applicable to	o the Chassis	being ad-
	C13-28: Removed since it	is a null set.		
	C13-29: An InfiniBand defir ment Entity which accepts a vides an IB-ML to it shall p facilities labeled as " Req " in <u>129</u> .	ned Chassis not o at least one Infinil rovide those fea n the "Passively	containing a C Band defined tures and the Managed" co	hassis Manage- Module and pro- dependent lumn of <u>Table</u>
	C13-30: An InfiniBand defi ment Entity which accepts a vides an IB-ML to it shall p facilities labeled as " Req " in	ned Chassis con at least one Infinil provide those fea n the "Actively Ma	taining a Cha Band defined tures and the anaged" colui	ssis Manage- Module and pro- dependent mn of <u>Table 129</u> .
	Table 129 Cl	nassis Feature	Requireme	ents
	Register	Unmanaged	Passively Managed	Actively Managed
	IB-ML	N/A	Req	Req
	IB-ML Slave Support	N/A	Req	Req
	CME	N/A	N/A	Req
	Module Power Control	N/A	N/A	Opt

Register	Unmanaged	Passively Managed	Actively Managed
IB-ML	N/A	Req	Req
IB-ML Slave Support	N/A	Req	Req
CME	N/A	N/A	Req
Module Power Control	N/A	N/A	Opt
Module Removal Control	N/A	N/A	Opt
IB-ML Selector Proxy	N/A	Opt	Opt
ChassisInfo Device	N/A	Req	Req

13.5.2 CHASSIS FEATURE DESCRIPTIONS 13.5.2.1 IB-ML

IB-ML is a multi-drop, multi-master, two-wire serial bus which uses signaling and arbitration protocols similar to that of SMBus 1.1 bus [24]. It primarily allows for access to defined facilities on the Module from the

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Chassis, but it also allows for certain defined operations to be sourced from the Module to the Chassis.

Architectural Note

IB-ML is architecturally considered "point-point" in that the address space from one IB-ML port is not shared with the address space of any other port. This allows for the same device address assignments to be used on each Module without having to resort to dynamic address assignment techniques.

An IB-ML is made up of 2 Backplane Connector defined signals: **IMxClk** and **IMxDat**. See <u>Section 11.5.1</u>, "IMxClk, IMxDat," on page 448 and <u>Annex A2: IB-ML Design Guidelines</u> for the electrical details of the IB-ML signals.

C13-31: A managed Chassis **shall** implement an IB-ML on at least the Primary Backplane Connector (Port 1) of all Slots (See <u>Section 12.5,</u> <u>"Chassis Power Rules," on page 470</u>). It **may** implement IB-MLs on other available Backplane Connectors; if so, it **shall** keep the multiple IB-MLs electrically isolated from each other.

See <u>Section 11.5, "System Management Group," on page 448</u> and <u>Annex</u> <u>A2: IB-ML Design Guidelines</u> for the details of the IB-ML signals.

13.5.2.2 IB-ML SLAVE SUPPORT

Logical slave devices on the IB-ML provide access to the ChassisInfo Device (See <u>Section 13.5.2.7, "ChassisInfo Device," on page 548</u> and, optionally, to a CME (See <u>Section 13.5.2.3, "CME," on page 546</u>).

C13-32: A Passively Managed or an Actively Managed Chassis **shall** respond as IB-ML slaves for Read and Write access to the device addresses labeled as "**Req**" in the "Access" column of <u>Table 130</u>.

C13-33: A Passively Managed or an Actively Managed Chassis **shall not** respond as IB-ML slaves for Read and Write access to the device addresses labeled as Not Permitted "**NP**" in the "Access" column of <u>Table 130</u>.

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A Passively Managed or an Actively Managed Chassis **may** respond as IB-ML slaves for Read and Write access to the following device addresses labeled as "Opt" in the "Access" column of <u>Table 130</u>.

Function	Device A	Address ^a	A	Deference
Function	Hex	Binary	Access	Reference
ModuleInfo Device	A0h	1010_000b	NP	Section 13.3.2.10 on page 517
Reserved for future IB definition	A2h	1010_001b	NP	
Reserved for future IB definition	A4h	1010_010b	NP	
Module Specific Use	A6h	1010_011b	NP	
Module Specific Use	ACh	1010_110b	NP	
Module Specific Use	AEh	1010_111b	NP	
Module Specific Use	40h-46h 50h-5Eh 90h-9Eh BCh-BEh C2h DCh-DEh		NP	Section 13.3.2.2 on page 495
ChassisInfo Device	A8h	1010_100b	Req	Section 13.5.2.7 on page 548
Chassis Specific Use	AAh	1010_101b	Opt	
CME Slave	E8h	1110_100b	Req ^b	Section 13.5.2.3.1 on page 547
MME Function	E0h	1110_000b	NP	Section 13.6.5 on page 581
MME lbML2lb	E2h	1110_001b	NP	Section 13.6.5 on page 581
MME Command	E4h	1110_010b	NP	Section 13.3.2.3.3 on page 498

a. This 7-bit Binary notation for IB-ML slave addresses leaves out the Write/Read direction bit which is encoded as the least significant bit on the IB-ML bus during the address phase. The accompanied Hex notation follows this Binary notation by left justifying the 7-bit IB-ML address to fit into an 8-bit wide byte and setting the list significant bit to 0. b. Not required for Passively Managed Chassis.

13.5.2.3 CME

C13-34: A system with an actively managed Chassis **shall** include a Chassis Management Entity (CME).

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	The CME has point-to-point connections via the IB ML) to each Module it supports. The CME may opti Switches within the Chassis. The CME and the Bas these links to move management data and comman Modules and Switches.	Management Link (IB- ionally have access to seboard Manager use nds between the CME,	1 2 3 4
	The CME may have access to all Backplane Conn VBxEn_L, IMxPReq_L, IMxInt_L, and IMxPRst.	ector signals such as	5 6 7
	C13-35: The CME in an Actively Managed Chassis CMEInfo Record and its fields that are labeled " Re (Section Table 158 on page 627). The CME shall re quired fields in response to a <u>ReadVPD</u> CME comp dicated by the CMEAccess field of the SlotInfo.	s shall implement the q " in <u>CMEInfo Record</u> eturn data for these re- nand from the ports in-	8 9 10 11 12
13.5.2.3.1 CME SLAVE			13
	As an IB-ML slave, the CME responds to CME Sla Table 130 Chassis IB-ML Slave Addresses on page	ve address listed in <u>e 546</u> .	14 15 16
13.5.2.4 MODULE POWER CONTR	ROL		17
	The Chassis Management Entity (CME) may contribute VBxEn_L pin as part of Chassis specific powertions. See <u>Section 11.3.4</u> , "VBxEn_L," on page 437 Section 13.6.12.7, "OutBandModuleCtl," on page 5	ol a Module power via r sequencing opera- <u>7</u> and <u>596</u>) rs) sub-ordinate to	18 19 20 21 22
	TCAs are outside of the scope of InfiniBand specifi	ication.	23 24
13.5.2.5 MODULE REMOVAL CON	ITROL		25
	An Actively Managed Chassis may choose to implivided mechanism to hold a Module in place tempo Using the CME_CTR , the Chassis may block the a Remove" indication.	ement a Chassis-pro- rarily or permanently. ssertion of the "OK To	20 27 28 29
	o13-7: If Module Removal Control feature is implem set the CME_CTR facility in the MME to 1b when t remove from the Chassis point of view. The CME m	nented, the CME shall he Module is clear to nay set the CME_CTR	30 31 32 33
			34 35 36 37
			39 40 41
			42

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bit to 0b when the Chassis wishes to indicate that the Module is not OK to remove, whether for physical or logical reasons.

Implementation Note

For example, the CME and the Management Software can be enabled to control an Electro-Mechanical Lock which can hold a Module in place. The CME may release the lock in response to a locally generated Request to Remove (e.g. via a Chassis mounted Request to Remove push-button, Chassis front panel keypad, etc.) or remotely in response to **SW_CTR** being asserted from management software. Proprietary IB messages and out-of-band interfaces may also be used to control the lock.

If it is known that the Chassis implements a mechanical lock, and that the mechanical lock condition is the only one that would cause the Chassis to deassert **CME_CTR**, then the state of the **CME_CTR** bit could be used to infer the state of the lock."

13.5.2.6 IB-ML SELECTOR PROXY

A CME can act as a proxy to "route" IB-ML operations to a specified slot's IB-ML using a selector field in an applicable command. (<u>Section 13.6.12</u>, <u>"CME Commands," on page 592</u>). A proxy of this type is necessary for managing non-protocol-aware Modules (i.e. Repeater Modules).

ChassisInfo.CMEAccess provides an indication as to whether this feature is present (See <u>Section 13.5.2.7. "ChassisInfo Device." on page 548</u>).

13.5.2.7 CHASSISINFO DEVICE

The ChassisInfo Device holds data that provide Vital Product Data (VPD) and other capability information such as **ChassisGUID** that are necessary to allow for the Hardware Management of a Chassis as it pertains to InfiniBand. ChassisInfo includes readable and write-protect areas. The ChassisInfo Device consists of one base VPD device and zero or more extension VPD devices. The base VPD device always resides at the ChassisInfo Device address specified in <u>Table 130: Chassis IB-ML Slave Addresses</u>.

These areas are readable and writable via IB-ML and IB.

C13-36: For every IB-ML-connected Slot, Managed Chassis **shall** implement at least 64 bytes of non-volatile writable area in ChassisInfo out of which the first 32 bytes are reserved for the Module and the second 32 bytes are reserved for the Baseboard Manager. It is recommended that the Chassis implement an additional 64 non-volatile writable bytes for OEM-software. The Chassis **may** implement this writable area in the base VPD device or in an extension VPD device

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	C13-37: In a ChassisInfo Device, a Managed Chass the ChassisInfo Record and its fields that are labeled <u>ChassisInfo Record - Record Format Version=2 on p</u> sisInfo Record shall immediately follow the Device H	sis shall implement d " Req " in <u>Table 153</u> bage 613. The Chas- eader. 4	
13.5.2.7.1 SLOTINFO		5	,
	C13-38: A Managed Chassis shall implement this field specific information. This element consists of SlotNu cess . See <u>ChassisInfo Record - Record Format Versited 153 on page 613</u>) for the details.	eld to provide slot mber and CMEAc- on=2 (Section Table 1	; ;)
13.6 MANAGEMENT COMMAND	S	1	1
	This section provides an outline for a transport mecha Band (IB) to the InfiniBand Management Link (IB-ML	anism from the Infini- 1 .) and vice-versa. 1 1	3 4 5
13.6.1 IB-то-MME (BASEBOA	RD MAD) COMMANDS	1	6
13.6.1.1 GENERIC MANAGEMENT	REQUESTS AND RESPONSES	1	7
	InfiniBand Architecture Specification, Volume 1, Chavices", Section "Baseboard Management", Subsection fines the primary fields that are used for a baseboard request MAD (Management Datagram) packets trans via the InfiniBand media.	pter "General Ser- on "MAD Fields" de- d management mitted and received 2 2	9 20 21 22
	Baseboard Management requests and responses are BMSend method described in <i>InfiniBand Architecture</i> <i>Volume 1</i> , Chapter "General Services", Section "BM baseboard management traps are delivered using th BMTraps may be suppressed by the receipt of a MAD pRepress method (See <i>InfiniBand Architecture Spee</i> Chapter "Management Model", Section "Traps").	e delivered using the e Specification, Methods". Similarly, e <i>BMTrap</i> method. D having the BMTra - cification, Volume 1, 2 3	24 25 26 27 28 29 30
	Typically, remote software will issue a BMSend with a data parameters that select a particular request (com cuted on the managed entity's MME. This will norma matching BMSend containing a response with a <i>con</i> that indicates whether the request was accepted. The hold additional parameter data based on the type of sued.	n attribute value and 3 mand) to be exe- lly be followed by a <i>npletion status</i> code e response may also request that was is- 3	12 13 13 13 13 13 13 13 13 13 13 13 13 13
	The BMSend method is also used for delivering requan IB -to- IB-ML message to the MME. The CME can sponding BMTrap message for the response and retuusing an IB-ML -to- IB mechanism. (See Section 13.6. on page 588)	uests to the CME via 3 then format a corre- irn it to the requester <u>9.1, "SendBMTrap,"</u> 4	8 9 0 1

Figure 166 depicts the structure of the a Baseboard Management MAD as defined in InfiniBand Architecture Specification, Volume 1, Chapter "General Services", Section "Baseboard Management". The Common Header portion is defined in InfiniBand Architecture Specification, Volume 1, Chapter "Management Model", Section "Management Datagrams" and is repeated as Figure 167 for convenience⁴.

Figure 166 Baseboard Management MAD Format

Offset	Byte 0	Byte 1	Byte 2	Byte 3	
0		Common N	IAD Header		
20					
24		B_I	Кеу		
28					
32		Rese	erved		
60					
64		Baseboard Ma	nagement Data		
252					

Figure 167 Common MAD Header Format

bytes					
0	BaseVersion	MgmtClass	ClassVersion	R	Method
4	Sta	tus	ClassSpecific		
8	TransactionID				
12					
16	AttributeID Reserved				
20		Attribute	Modifier		

4. InfiniBand Architecture Specification, Volume 1 shall take precedence over Figure 167 should differences exist.

Table 131 outlines the baseboard management MAD usage of the common MAD fields. Refer to InfiniBand Architecture Specification, Volume 1, Chapter "Data Packet Format and Chapter "Management Model", Section "Management Datagrams" for additional information on packet format and field offsets.

Table 131 Common MAD Field usage for Baseboard Management

Field Name	Length (bits)	Description
BaseVersion	8	Version of MAD base format. Set to 1.
MgmtClass	8	Designates Baseboard Management class. Value is defined in <i>InfiniBand Architecture Specification, Volume 1</i> , Chapter "General Services", Section "Management Datagrams".
ClassVersion	8	Version of MAD class-specific format. Set to 1 for this version of the specification.
R	1	This field is used in combination with Method to differentiate "Send" methods from "Response" methods. 0 indicates a request, 1 a response. Baseboard Management Commands are only transported using "datagram" send methods BMSend and BMTrap ; these meth- ods only produce "requests" as represented by this bit. Other methods supported by the Baseboard Management Class do produce "responses" (i.e. BMGet, BMSet, etc.). The Baseboard Management commands utilize the Attribute Modifier to commu- nicate command level request / response indications.
Method	7	Baseboard management commands use the BMSend Method. Traps use the BMTrap Method. The other valid methods are defined in <i>InfiniBand Architecture Specification, Volume 1</i> , Chapter "General Services", Section "Baseboard Management".
Status	16	This field is only valid for Methods with the R bit set. Thus, this is always 0000_0000h for BMSend and BMTrap Methods.
ClassSpecific	16	Reserved for this version of the specification.

Field Name (bits		Description			
ransactionID	64	For baseboard management commands from software, the Transaction ID is incremented indicate a new instance of a request at the IB packet level. For retried requests, the Transac- tion ID is not incremented, but instead Transaction ID from the initial request is repeated.			
		The MME maintains its own Transaction ID counter for outgoing requests that it generates, including messages generated using the IbML2BM (IB-ML -to Baseboard Manager) functionality. This counter is also incremented for each new request, and repeated for retried requests. The MME is allowed to restart its outgoing Transaction ID value from 0 whenever the communication on the Module's InfiniBand interface is activated. It is recommended that the MME keep the outgoing Transaction ID on standby power if possible in order to reduce this occurrence.			
		BMSend and BMTrap Methods are unacknowledged data- grams. The actual matching of Baseboard MAD requests and responses occurs at the Baseboard Management command level, using the BMSequenceNumber that is part of the Base- board Management Data field in BMSend and BMTrap requests.			
AttributeID	16	This field holds a value that identifies the baseboard manage- ment "command" to be performed. <u>Table 136: Baseboard MAD</u> <u>Commands</u> provides an overview list of the commands and their associated request and response parameters. The BM Attributes defined in <i>InfiniBand Architecture Specification, Vol-</i> <i>ume 1,</i> Chapter "General Services", section "BM Attributes" pro- vides the attribute ID values assigned to the individual commands.			
Reserved	16				
AttributeModi- ïer	32	 [31:1] Reserved. 0000_0000_0000_000h. [0] Response/Request or BMTrap 0b = Attribute is for a Baseboard Management Command request. 1b = Attribute is for a Baseboard Management Command response or BMTrap 			

Table 131 Common MAD Field usage for Baseboard Management

Field Name	Length (bits)	Description
s_Key	64	A 64-bit (8-byte) key that is used to protect Baseboard Manage- ment operations.
		This specification allows more than one B_Key in a partition.
		The Baseboard Manager sets Nodes' B_Keys using BMSet(BKeyInfo). A Node shall include its B_Key in every Baseboard Management MAD that it emits.
		The Method and the Attribute Modifier determine how the B_Key is handled. If the message is a <i>request</i> , it shall only be accepted if its B_Key matches the B_Key set earlier by the Baseboard Manager via a BMSet(BKeyInfo). If the message is a <i>response</i> or a BMTrap, by default, the receiver shall ignore the B_Key.
		An implementation may include a vendor-specific option to check the B_Key in responses. This is a provision to allow an MME associated with a Baseboard Manager or a system software to check B_Keys on responses, if desired.
		See InfiniBand Architecture Specification, Volume 1, Chapter "General Services", section "B_Key General Use" and section "BKeyInfo". Also see <u>Section 13.6.1.1, "Generic Management</u> <u>Requests and Responses," on page 549</u> for more information.

Table 132 B_Key Field usage for Baseboard Management

42

Field Name Description BMSequence 16 This value is used to track requests and responses at the Base board MAD Command level. The value is incremented (with wrap-around to 0000h at FFFFh) for new BMTraps and BMSend requests, and repeated for retried traps and requests. For responses, the value that was passed in the request is returned in the response. The MME maintains its own BMSequence number that is used to tag requests that it generates (typically as the result of generating an IB-ML -to- Baseboard Management Command request or response. The MME and CME 7-bit slave addresses in bits [7:1] of this field By convention, bit 0 is always 0b. 00h = Source is unspecified. 00h = Source is unspecified.
BMSequence 16 This value is used to track requests and responses at the Base board MAD Command level. The value is incremented (with wrap-around to 0000h at FFFFh) for new BMTraps and BMSend requests, and repeated for retried traps and requests. For responses, the value that was passed in the request is returned in the response. The MME maintains its own BMSequence number that is used to tag requests that it generates (typically as the result of generating an IB-ML -to- Baseboard Manager transaction). BMSourceDe-vice 8 Identifies the source of the Baseboard Management Command request or response. The MME and CME values are based on the MME and CME 7-bit slave addresses in bits [7:1] of this field By convention, bit 0 is always 0b. 00h = Source is unspecified. E0h = source is the MME
BMSourceDe- 8 Identifies the source of the Baseboard Management Command request or response. The MME and CME values are based on the MME and CME 7-bit slave addresses in bits [7:1] of this field By convention, bit 0 is always 0b. 00h = Source is unspecified.
BMSourceDe- vice Identifies the source of the Baseboard Management Command request or response. The MME and CME values are based on the MME and CME 7-bit slave addresses in bits [7:1] of this field By convention, bit 0 is always 0b. 00h = Source is unspecified. E0h = source is the MME
00h = Source is unspecified.
E(h - source is the MME
E9h - source is the CME (Lead when CME concretes
Baseboard Management request or responses.
FEh = source is Baseboard Manager.
BMParmCount 8 Indicates the number of parameter bytes in the BMParameters field. 1-based. 0 means no additional command parameter data follows.
BMParameters 0 to 40*8 Baseboard MAD Command request and response parameters for the given Attribute ID. Refer to <u>Table 136</u> : <u>Baseboard MAD</u> <u>Commands</u> for the parameter definition and offsets of the bytes used within this field, and for command-specific completion sta tus values. Refer to <u>Table 135</u> : <u>Completion Status Values</u> for completion status values that can be used with any Baseboard MAD Command response.
Background: The 40 byte maximum specified is for a 32 byte data write using the command with the largest command header / trailer information per <u>Table 136: Baseboard MAD Commands</u> (WriteVPD).
40B = 1B (Device Selector) + 2B (# of bytes to write (NBW + 2B (Offset) + 1B (CMD) + 1B (Length) + 32B (Data) + 1E (PEC)
Reserved var Fill to produce the required 192 byte MAD Data Field. Content is unspecified.
Number of bits equal 1504 - BMParameters field size (in bits).
Background: 1504 = 1536 (192B*8) - 32 (BMSequence

Table 133 Baseboard Management Data Field

13.6.1.2 DELIVERING REQUEST MESSAGES TO THE MME

2 The **BMSend** request message is used for both delivering requests to the MME from IB, and responses from the MME to IB. (The request/response 3 formats are actually symmetric, so it would also be possible for the MME 4 to generate a request to IB, and receive a response from IB). 5 6 As an example, Table 136 Baseboard MAD Commands on page 570 de-7 fines a GetModuleStatus attribute that allows Baseboard Manager soft-8 ware to get information such as whether an Attention indication is being 9 asserted by the Module, or whether a fault condition exists. For this example, assume that software will be using the command to retrieve the 10 present state of the Module LEDs. The following outlines the steps that 11 are used for sending this command and getting the corresponding re-12 sponse. 13 14 C13-38.1.1: A Protocol Aware module shall perform the actions to be per-15 formed by either the MME or Node in Section 13.6.1.2. 16 17 1) Baseboard Management software formats up the request by filling in 18 the appropriate fields of the request message: 19 The Baseboard Management Software shall populate the source 20 and destination queue-pair addressing and Q Key information for 21 the channel that routes the request from the Baseboard Manager 22 to the Module. 23 The Baseboard Management Software shall set the Method field 24 to the value for BMSend (see InfiniBand Architecture Specifica-25 tion, Volume 1, Chapter "General Services", Section "BM Meth-26 ods"). 27 The IB packet communication function associated with the Base-28 board Management Software shall set the Transaction ID field. 29 This function shall increment the transaction ID field for each new request, and shall leave it the same for retried requests. 30 31 The Baseboard Management Software shall set the Attribute ID • 32 field to identify which baseboard management command it is per-33 forming. 34 For this example, the Attribute ID field will be set to the value for 35 the GetModuleStatus attribute (see InfiniBand Architecture Speci-36 fication, Volume 1, Chapter "General Services", Section "BM At-37 tributes"). Table 136 Baseboard MAD Commands on page 570 lists the parameters and bit-fields associated with the baseboard 38 management attributes. Table 136 is followed by command de-39 scriptions for each Attribute ID. The actual values for the Attribute 40 IDs are specified in the "BM Attributes" section in the Management 41 Chapter of the InfiniBand[™] Architecture Specification, Volume 1. 42

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	• The Baseboard Management Software shall cant bit of the Attribute Modifier field to 0b f	set the least signifi- or a <i>request</i> .
	 The Baseboard Management Software shall to the required value obtained from the Confi (CFM) or other entity managing the B_Keys. 	set the B_Key value 3 guration Manager 4
	 The Baseboard Management Software shall quence and BMSourceDevice sub-fields wi Management Data field. (The Baseboard Ma shall set the BMSourceDevice sub-field to I message is from the Baseboard Manager.) 	set the BMSe - thin the Baseboard anagement Software FEh to indicate the 9
	 The Baseboard Management Software shall Count and BMParm sub-fields within the Base ment Data field as specified in <u>Table 133</u>: Base Management Data Field and according to the umn for the specific command in <u>Table 136 E</u> <u>Commands on page 570</u>. 	set the BMParm- seboard Manage- aseboard 11 2 2 2 2 3 3 3 3 3 3 3 3 3 3 3 3 3
	In this example, BMParmCount is set to zer tional parameters are required for the <i>GetMo</i> mand.	o because no addi- 16 17 18
2)	The remaining header fields and data integrity cl filled in according to the packet format specificat finiBand Architecture Specification, Volume 1.	neck fields shall be 19 ions defined in <i>In-</i> 20 21
3)	The message is delivered via the fabric to the m	anaged IB Module. 22
4)	The Node in the IB Module receives the packet, Baseboard Management Agent (BMA) function. identifies Baseboard Management class message valid, the BMA passes the necessary message f The MME shall be delivered the Attribute Modi finiBand packet fields that are necessary to format to the requester. (The Transaction ID is not require the MME.) The B_Key gets checked if bit 0 of the is 0b (a <i>request</i> message and not a BMTrap). Se <u>Common MAD Field usage for Baseboard Manage</u> and <u>Table 132 B Key Field usage for Baseboard</u> page 553.	and passes it to the The BMA function23The BMA function24es. If the message is ields to the MME.25fier and all In- at the response back ired to be passed to e Attribute Modifier28at the response back ields 131 gement on page 551311 Management on33
5)	The MME processes the <i>request</i> by examining the tribute , the Attribute Modifier , and baseboard in fields. The MME may ignore unsolicited <i>response</i>	ne values of the At- 34 management data 35 es. 36
6)	If the requested action is valid and accepted, the <i>response</i> message with a completion status of 0 erwise, the MME shall return a non-zero completion din <u>Completion Status Values</u> (Section Table The response will typically be delivered after the cuted; however, in some cases, such as for <u>SetM</u>	MME shall format a370h = "OK". Oth-38ition status as de-39135 on page 565).40command is exe-41ModulePMControl42

InfiniBand ^{1 M} Architecture Release 1.2 VOLUME 2 - PHYSICAL SPECIFICATIONS		Hardware Management	October, 2004 FINAL
		command, the execution of a command may pr from being delivered. In these cases, the MME sponse before acting on the requested comma	event the response shall return the re- nd.
	7)	The MME passes the following fields to allow th BMSend message with the following content:	ne BMA to format a
		 The MME shall set the InfiniBand addressin destination as defined in InfiniBand Archited Volume 1. 	ng information for the cture Specification,
		For this example, the addressing informatio of the <i>request</i> .	n is for the originator
		 The MME shall set the Method field to the (see InfiniBand Architecture Specification, N "General Services", Section "BM Methods") 	value for BMSend /olume 1, Chapter
		• The MME shall set the R bit to 0b.	
		 The MME shall set the Transaction ID field MME's Transaction ID counter. 	d to the value from
		 The MME shall set the Attribute ID field to cific command attribute to which it is response. 	the value for the spe- nding.
		For this example: the value for the <i>GetModu</i> InfiniBand Architecture Specification, Volum Services", Section "BM Attributes").	<i>leStatus</i> attribute (see e 1, Chapter "General
		 The MME shall set Bit 0 of the Attribute M cate a response. See <u>Table 131 Common N</u> <u>Baseboard Management on page 551</u>. 	odifier to1b to indi- IAD Field usage for
		 The MME shall set the BMSequence sub-f board Management Data field to the BMSe was passed in the request. 	field within the Base- equence value that
		• The MME shall set the BMSourceDevice s dicate the message is coming directly from	sub-field to E0h to in- the MME functionality.
		 The MME shall set the BMParmCount and fields in the Baseboard Management Data f the Response Data column for the GetModu Table 136 Baseboard MAD Commands on 	BMParameter sub- ield as specified by <i>IleStatus</i> command in page 570.
		For this example, there are six bytes of para cluding the completion status, so the BMPa 06h and the BMParameter Field will hold th	ameters returned, in- rmCount field will be e six response data

state information.

message to the IB fabric.

bytes for the GetModuleStatus command. According to Table 136:

Baseboard MAD Commands, byte six contains the desired LED

8) The Node shall add its B_Key and complete the formatting of the

message using the **BMSend** Method and deliver the formatted

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	 The response is then delivered to the originat process is completed. 	ing software and the 1	>
13.6.1.3 IB-TO-IB-ML Access		3	}
	C13-38.1.2: Protocol aware modules shall provid defined in <u>13.6.1.3 IB-to-IB-ML Access on page 5</u>	de IB2IBML operations 5 558. 6	5
	The Management Commands support "low-level" IB-ML. This is accomplished using the <i>Ib2IbML</i> co can be used for the following three types of IB-M	access to devices on an 7 ommand. The command 8 L transactions: 9	, ; ; ;
Atomic Write	Atomic write to an IB-ML device. This is a write o IB-ML device at the specified slave (device) addre tion. No data is returned from the device. Devices typically use this type of transaction when being w	f N-bytes of data to the 1 ess, as a single transac- 1 s such as SEEPROMs 1 written. 1	1 2 3 4
Atomic Read	Atomic Read from an IB-ML device. This is a real the IB-ML device at the specified slave (device) a transaction. In this transaction, no parametric dat prior to the read. Because of this, this transaction with devices such as simple latches that do not n other write to select the data to be returned.	d of M-bytes data from address, as a single a is written to device n is typically only used eed an "index" value or 2	6 7 8 9 20
Atomic Write-Read	Atomic Write-Read to an IB-ML device. This is a followed by a read of M-bytes of data to/from the slave (device) address. The write and read transa with a "repeated start" to form a single, atomic tra Devices such as SEEPROMs use this type of tra random reads, where the write data are used to se SEEPROM from which the read data are to be re	write of N-bytes of data device at the specified actions are tied together ansaction on the IB-ML. nsaction for supporting at an offset value into the sturned.	22 23 24 25 26 27 28
	The <i>Ib2IbML</i> command includes parameters for t write to and the number of bytes to read from the three IB-ML transactions are selected according t for the write and read counts. If a non-zero write- read count is set to zero an Atomic Write is perfo is set to zero and a non-zero number used for the Read is performed. Lastly, if both values are non- Read transaction is performed.	he number of bytes to specified device. The to what values are used count is used and the rmed. If the write count e read count an Atomic -zero an Atomic Write-	29 20 20 20 20 20 20 20 20 20 20 20 20 20
	Figure 168: IB-to-IB-ML Access illustrates how the eters passed in the <i>Ib2IbML</i> command, creates the ML, and generates the corresponding response. bytes at offset 5Ah from a 24C02-style SEEPROP ample. This requires a write-read transaction whe written to the device and then the data read out.	e MME takes the param- ne transaction on the IB- A random read of three M is shown as the ex- ere the offset to read is	;7 ;8 ;9 ;0 ;1



The thick arrow lines identify field data that the MME essentially copies from the request to the response. The thin arrow lines identify data that are transferred to and from the IB-ML.

Transactions and arbitration on IB-ML **shall** follow the SMBus 1.1 specification.

29 A transaction is begun with a master (the IB-ML Agent in the MME in this 30 case) arbitrating for the bus and then issuing a START condition followed by the 7-bit slave address of the device it wishes to access. The least sig-31 nificant bit of the slave address byte indicates whether the transfer is a 32 write (0) or a read (1). All bytes transferred are followed by an ACK bit in-33 terval. For master writes to a slave, the slave device is responsible for 34 ACK'ing any bytes written to it, including its slave address. If the slave 35 NACKs one of the written bytes, the transaction is terminated by the 36 master and the MME returns an error value for the completion status. 37 Conversely for bytes read by a master from a slave, the master is responsible for ACK'ing the bytes, with the exception of the last read byte which 38 the master NACKs.

The transaction is concluded by the master driving a STOP condition onto the bus. SMBus write and read transactions can be concatenated by is-

23

24

25 26

27

sui Th Ato Iov by	ng another START condition and slave address instead of a STOP. s is referred to as a "repeated START". The IB-ML only specifies an omic Write-Read transaction, which is a single write transaction fol- ved by a single read transaction concatenated to the write transaction a repeated START.	1 2 3 4
Re VP ha	ferring to Figure 168, the following steps outline how SEEPROMs (e.g. D Devices) are accessed on the IB-ML. Note that for simplicity, the ndling of the ACK bit intervals is left out.	5 6 7 8
1)	The BMA receives the message via the TCA and passes the request data to the MME (See <u>Section 13.6.1.2</u> , " <u>Delivering Request Messages to the MME</u> ," on page 555).	9 10 11
2)	The MME interprets the Attribute field and finds an <i>Ib2IbML</i> request.	12
3)	MME checks the write and read byte counts. If the number of bytes to write and the number of bytes to read are both zero, the request is invalid and the MME shall return an error value for the completion status as defined in <u>Completion Status Values (Section Table 135 on page 565)</u> .	13 14 15 16 17
4)	MME gets IB-ML Agent to arbitrate for the IB-ML.	18 19
	If the MME cannot win arbitration, times out waiting for a bus free con- dition, or a bus error occurs during the transaction, it shall return a re- sponse with an appropriate error value for the completion status as defined in <u>Completion Status Values (Section Table 135 on page 565)</u> .	20 21 22 23
		24
Ir	nplementation Note	25 26 27
T A th a th	he MME is not allowed to arbitrate until detecting a bus free condition. In MME implementation can elect to automatically retry arbitrating for e IB-ML on the next bus free condition instead of giving up on the first tempt. This type of implementation is recommended, since it reduces e possibility that software will need to retry the IB request.	28 29 30 31
5)	MME formats the Write data for the IB-ML based on the number of bytes to write.	33 34
	If Write Count is not zero, the MME shall issue an IB-ML START condition, write the device slave address with LSB=Wr (0), and then write the indicated number of data bytes to IB-ML. If the Write Count is zero, the MME skips to the following step.	35 36 37 38
	In this example, just one data byte, 5Ah, is written.	39
6)	If the Read Count is not zero, the MME shall issue an IB-ML START condition, write the device slave address with LSB=R (1), and clock	40 41 42

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	in data bytes based on read count. If the Read Count is zero, the MME shall skip the following step.
	In this example, three bytes are read from the specified IB-ML device.
	7) MME shall fill in appropriate completion status, address, and R fields as defined in <u>Section 13.6.1.2</u> , " <u>Delivering Request Messages to the</u> <u>MME.</u> " on page 555) and forwards the response message data to the BMA for transmission to IB.
	 The BMA waits for an IB transmit opportunity and sends the re- sponse.
13.6.1.4 IB-ML SPLIT-TRANSAC	DN MESSAGING
	The CME is accessed using a split-transaction messaging mechanism on IB-ML. The messaging is defined symmetrically; the CME can generate both requests and responses, and a party can send both requests and responses to the CME. An MME may also be accessed using a split-transaction messaging mechanism on IB-ML. See <u>MME Commands (Section 13.3.2.3.3 on page 498)</u> .
	Messages to the CME can be delivered from Baseboard Management MADs by using a BMSend method with the Ib2CME attribute. The Ib2CME command is similar to the Ib2IbML command, except that it only supports writing data to the CME on IB-ML. (The CME's device address is implicit in the command). The data contains the message for the CME.
	This specification also defines how the MME would be accessed with the same messaging approach. In this case, the <i>Ib2MME</i> attribute is used to deliver messages to an MME.
	When the <i>Ib2CME</i> attribute is used to send messages to the CME via the MME, the MME does not check the semantics of the CME message data, (although it can check that the message data meets the maximum IB-ML transaction specifications, see <u>13.6.1.11</u> : <u>Maximum Transaction / Message Lengths</u>) it simply transfers the data to the IB-ML.
	Because of this, and because messaging communication with the CME uses a split-transaction, the immediate response to the <i>Ib2CME</i> request only indicates that the message data was forwarded to IB-ML and the CME. (If the message data could not be delivered, perhaps because of an IB-ML bus error, or a busy CME, the MME will return an error value for the completion status.)
	If the message data held a request for the CME, sometime later, the CME will asynchronously format and send a Baseboard Management MAD using the <i>SendBMTrap</i> message. See <u>Section 13.6.9, "MME IbML2Ib</u> Register Descriptions," on page 588.

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Messages from IB to the MME are directly handled by the MME, however, the same split-transaction rules apply. The response to the *Ib2MME* command indicates that the request was simply transferred to the MME, *not* whether the MME has actually processed the request. A separate response message will be sent from the MME once it has processed the *Ib2MME* command.

13.6.1.5 IB-ML SPLIT-TRANSACTION MESSAGE FORMAT

Figure 170 shows the generic format used for requests and responses on IB-ML. For simplicity, the ACK interval is not shown. The most visible difference between requests and response formats is that responses include a completion status field and have the "Rs" bit set to 1. The individual fields are described below.

Request

S	Destination Device ID (e.g. CME address)	0	CMD Set	Length	Source Device ID (e.g. MME address)	Rs (0)	Seq	Data	PEC	Ρ	
---	---	---	------------	--------	--	-----------	-----	------	-----	---	--

Response

S	Destination Device ID (e.g. MME address)	0	CMD Set	Length	Source Device ID (e.g. CME address)	Rs (1)	Seq	Data	PEC	Ρ
---	---	---	------------	--------	--	-----------	-----	------	-----	---

S = START condition, P = STOP condition. ACK bits not shown.

Figure 169 Generic IB-ML Split-Transaction Format

The positions of Seq and CMD Set fields in the above formats allow all IB-ML "split transaction" messages, regardless of CMD Set, to have a common header. The Seq field in the CME message serves a purpose similar to that for the Transaction ID field in the baseboard management MAD. The Seq field provides a way to differentiate new instances of a request from retried requests, and provide a mechanism for matching up requests with responses at the CME messaging level.

13.6.1.6 GENERIC IB-ML SPLIT-TRANSACTION MESSAGE PARAMETERS

C13-39: An entity that supports IB-ML Split-transaction messages to a CME or MME **shall** have the fields as indicated by <u>Figure 170</u> and defined in this section.

Destination Device ID 7-bit ID of device/function on IB-ML that is to receive the message. This directly maps to an IB-ML slave address. Typically, this will be either the CME or MME address. The 7-bits of the Destination occupy the most significant bits of the first byte of the message. The least significant bit of the byte is always 0. Hardware Management

Source Device ID	7-bit ID of device/function on IB-ML that is sending the message. This will also typically be the slave address of the CME or MME. For request mes- sages, this field is used to tell where a corresponding response message should be sent. For responses, this identifies the device that originated the response. The 7-bits of the Source Device ID occupy the most signif- icant bits of the second byte of the message. The least significant bit of the byte is the Rs bit, described below.	1 2 3 4 5 6
Rs	1-bit field that differentiates request messages from response message. A 1 indicates a response, 0 indicates a request.	7 8 9
CMD Set	Identifies the command set from which the command is defined. Com- mand sets are:	10 11

Command	Description
00h	IB-ML, InfiniBand Hardware Management.
01h:1Fh	reserved
20h	IPMI Hardware Management
21h	DMTF Pre-OS Working Group (ASF)
23h	OEM - controller specific. The commands are specified relative to the OEM that has specified the functionality of the device that receives the message. The device must respond to a command that retrieves the OEM ID from the device itself, or if not present, the OEM ID from the Chassis info is used.
24h	OEM/Std. Other Standard body. These commands are required to have an OEM ID as the first 3 bytes of the data field in the request, and as the first three bytes of data in the response. The OEM ID can specify a manufacturer or standardization body.
25h	PCI (placeholder)
26h	Compact PCI (placeholder)

Table 134 IB-ML Command Sets

Length

Seq#

Data

as

1-byte field indicating the number of bytes following the length byte, but excluding the PEC. A length of 1 indicates there is one byte following the length byte.

Used to identify different instances of a particular command. Can be used by the requester to match up responses with particular requests. Can be used by destination device to discriminate retries from new requests. The value 00h is used to indicate a request that should never be interpreted as a retry. The Seq field is tracked per Source Device ID.

Data parameters specific to given CMD Set/CMD, or OEM ID if CMD Set 40 = OEM/Std. 41

41 42

32

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PEC	Packet Error Code. This is an 8-bit CRC on all the preceding mess bytes, including the initial slave address and read/write bit. The pol mial for the CRC is: $C(x) = x^8 + x^2 + x^1 + 1$ and shall be calculated order of the bits as received. The PEC algorithm starts off with an i value of 00h.						
	o13-8: The PEC field is optional unless otherwise state mand set. If it is present, it shall be the first byte after t cated by the length field.	ed for a giv the last by	'en com te indi-	ו- 6 7 8			
13.6.1.7 IB-ML CMD SET SPECI	FIC FIELDS			9			
	C13-40: An entity that supports CMD Set = IB-ML as de shall provide the additional fields defined in <u>Section 13</u>	efined in <u>Ta</u> <u>3.6.1.7</u> .	<u>able 134</u>	10 11 12			
CMD	Command. Identifies the requested function under the set. (See <u>Table 140 MME Function Registers on page MME IbML2Ib Registers on page 588</u> , <u>Table 123 MME page 499</u> , and <u>Table 143 CME Commands on page 593</u> first data byte of both requests and responses.	IB-ML con <u>584, Table</u> Commane <u>3</u>). The CM	nmand <u>) 141</u> <u>ds on</u> 1D is the	13 14 15 0 16 17			
Completion Status	This is the second byte of the data field of responses with CMD Set = IB-ML. The field indicates whether the request was successfully processed or not. Completion Status values are specified for the individual commands. In addition, there is a set of generic completion status values that can be used. See Table 135 Completion Status Values on page 565.						
PEC	Packet Error Code. See <u>Section 13.6.1.6, "Generic IB-</u> tion Message Parameters." on page 562. C13-41: The PEC field shall be present for all CMD Se sages.	<u>ML Split-tr</u> et = IB-ML	<u>ansac-</u> . mes-	23 24 25 26 27 28 20			
	Request			30			
	S Destination Device ID (e.g. CME address) 0 Set = IB-ML Length IB-ML Source Device ID (e.g. MME (0) address) Seq CME	D Data PEC	Ρ	32 33			
	Response			35			
	S Destination Device ID (e.g. MME address) 0 CMD Set = IB-ML Length Source Device ID (e.g. CME address) Rs (1) Seq CMD Com St	npletion tatus Data	PEC P	36 37 38			
	S = START condition, P = STOP condition. ACK bits not shown. Figure 170 IB-ML Message Form	mats		39 40 41			

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13.6.1.7.1 GENERIC SPLIT-TRANSACTION COMPLETION STATUS VALUES

Table 135: Completion Status Values,
can be used with any CMD Set = IB-ML or CMD Set = OEM Controller-
specific split-transaction response. In addition, Table 135 contains the list
of common completion status values that can be returned in Baseboard
MAD responses shown in Table 136 and the lists of common completion
status values that a CME may return in response to CME commands in
Table 143.2111112311131111141111115111111611111171111117111111711111171111117111111711111171111117111111711111171111117111111711111171111117111111711111</

Value	Definition
00h-3Fh	generic completion status
00h	ОК
01h	Unspecified error
02h	CME busy
03h	MME busy
04h	command not supported
05h	illegal request parameter
06h-3Fh	reserved for generic completion status
40h-BFh	command-specific completion status
40h	Write protected
41h	NACK'd
42h	Bus error
43h	Busy (arb loss)
44h	Invalid VPD device selector
45h	Illegal offset
46h	Illegal byte count
C0h-FFh	Vendor-specific Error (defined by vendor identified by the Vendor ID field in the Module info)

Table 135 Completion Status Values

13.6.1.8 IPMI/DMTF PRE-OS WORKING GROUP CMD SET FIELDS

o13-9: An entity that supports CMD Sets = IPMI and ASF as defined in Table 134 shall have the fields as indicated by Figure 171 on page 566 and defined in Section 13.6.1.8.

Note that the IB-ML defined Completion Status field is not a standard part of these response messages, although equivalent fields may be specified.

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Data	Additional data parameters, as specified by the IPMI or DMTF Pre-OS Working Group specifications.							
PEC	Packet Error Code.							
	o13-10: The PEC field may be present for all CMD Set = IPMI and ASF messages. If present, it shall be as specified in <u>Section 13.6.1.6</u> , "Generic <u>IB-ML Split-transaction Message Parameters," on page 562</u> .							
	Request	9 10						
	S Destination Device ID (e.g. CME address) 0 CMD Set = IPMI or ASF Length Source Device ID (e.g. MME address) Rs (0) Seq Data PEC P	11 12 13						
	Response	14 15						
	Destination Device ID (e.g. MME address) 0 CMD Set = IPMI or ASF Length Source Device ID (e.g. CME address) Rs (1) Seq Data PEC P	16 17 18						
	Figure 171 IPMI/ASF Message Formats	19 20						
13.6.1.9 OEM CONTROLLER-SPE	ECIFIC CMD SET FIELDS	21 22						
	o13-11: An entity that supports CMD Sets = OEM as defined in <u>Table 134</u> shall have the fields as indicated by <u>Figure 172 OEM Controller-specific</u> <u>Message Formats on page 567</u> and defined in <u>Section 13.6.1.9</u> .	23 24 25						
	These commands are formatted like CMD Set = IB-ML messages, except the CMD Set = OEM. The meaning of the CMD field is specified by the OEM associated with the controller that accepts the request.	26 27 28						
CMD	Command. Identifies the requested function under the OEM command set. The CMD values and semantics are specified by the vendor / organi- zation identified by the ID returned by the GetVendorID CME Command. The CMD is the first data byte of both requests and responses.							
Data	Additional data parameters, as specified by OEM.	34 35						
Completion Status	This is the second byte of the data field of responses with CMD Set = 36 OEM. Command-specific completion status codes are specified by the 37 OEM. In addition, there is a set of generic completion status values that can be used. See <u>Table 135 Completion Status Values on page 565</u> . 39							
PEC	Packet Error Code. See <u>Section 13.6.1.6, "Generic IB-ML Split-transac-</u> tion Message Parameters," on page 562	40 41 42						

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1

o13-12: The PEC field shall be present for all CMD Set = OEM messanes

	Sages.						
	Request						
	Destination Device ID (e.g. CME address) 0 CMD Set = OEM Length Source Device ID (e.g. MME address) Rs (0) Seq CMD Data PEC P						
	Response						
	Destination Device ID (e.g. MME address) 0 CMD Set = OEM Length Source Device ID (e.g. CME address) Rs (1) Seq CMD Completion Status Data PEC	Р					
	Figure 172 OEM Controller-specific Message Formats						
.6.1.10 OEM/STD	ID SET SPECIFIC FIELDS						
	o13-13: An entity that supports CMD Sets = OEM/Std as defined in	<u>Table</u>					
	<u>134</u> shall have the fields as indicated by <u>Figure 173 OEM/Std Mess</u>	<u>sage</u>					
	Formats on page 568 and defined in Section 13.6.1.10.						
	Note that the Completion Status field is not a standard part of these	e re-					
	sponse messages.						
	Three byte OEM ID. Same format as OEM/Mfr. ID used in GUID. Fields						
	dards body identified by the OEM ID.						
ta	Additional data parameters, as specified by OEM/Mfr or standards b	body					
	identified by the OEM ID.						
ic.	Packet Error Code						
	o13-14: The PEC field may be present for all CMD Set = OEM/Std	mes-					
	sages. If present, it shall be as specified in Section 13.6.1.6, "Gener	<u>ric IB-</u>					
	ML Split-transaction Message Parameters," on page 562.						

39 40

41 42

Re	equest											
s	Destination Device ID (e.g. CME address)	0	CMD Set = OEM/Std	Length	Source Device ID (e.g. MME address)	Rs (0)	Seq	OE IE (3 by	M) rtes)	Data	PEC	Р
Re	esponse											
s	Destination Device ID (e.g. MME	0	CMD Set = OEM/Std	Length	Source Device ID (e.g. CME	Rs (1)	Seq	CMD	0 (3 t	EM D	Data	PEC

Figure 173 OEM/Std Message Formats

13.6.1.11 MAXIMUM TRANSACTION / MESSAGE LENGTHS

C13-42: An entity that implements IB-ML operations **shall** adhere to the requirements of <u>Section 13.6.1.11</u>

All IB-ML transactions are limited to an overall write transaction length of 36 bytes and an overall read transaction length of 36 bytes. That is to say, there are no more than 36 bytes from START condition to STOP or Repeated Start to STOP.

Architectural Note

Because there is varying overhead required for address bytes, length fields, CMD Set fields, PEC, etc., the maximum amount of data payload will vary. Factors such as proxy accesses and using IB-to-IBML commands also introduce variations in the number of data bytes that can be carried based on the access mechanism.

For the command in (CMD set == IBML), the 36-byte limit allows sufficient number of bytes of data field payload to be carried to the final targeted IB-ML device across all interfaces. The software does not need to adjust payload size based on the path (Ib2IBML, CME proxy, a peer on IBML) it takes to deliver the transaction.

- 1) All MME's **shall** accept at least 42-bytes of Baseboard Management Data from the BMA. Note that IB addressing fields, Transaction ID, etc. are not part of the Baseboard Management Data field.
- 2) All MME's shall accept a 36-byte (slave address through PEC) IB-ML 3
 write for accessing the IbML2Ib register. All other MME write transactions shall support at least the number bytes in registers specified in Table 140 MME Function Registers on page 584 and Table 141 MME IbML2Ib Registers on page 588.

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	3)	An MME is allowed to accept write transactions gre bytes. Until the next STOP condition, an MME shal ceived byte of a write-transaction once the MME's in	ater than 36 I NACK every re- nput buffer is full.
	4)	All CME's shall accept at least 36-bytes written to it ML.	t as a slave on IB-
	5)	All MME's that implement MME Command shall ac bytes written to it as a slave on IB-ML.	cept at least 36-
	6)	A CME is allowed to accept write transactions great A CME shall NACK the first byte of a write-transact its buffer size. Until the next STOP condition, a CMI every received byte of a write-transaction once the buffer is full.	ter than 36 bytes. tion that exceeds E shall NACK CME's input
	7)	The writable IB-ML VPD devices shall accept write least 8 data bytes. The writable IB-ML VPD devices write transactions that cause writes to go beyond th boundary.	transactions of at can NACK the e device
	8)	IB-ML VPD devices shall accept read transactions bytes, excluding read transactions that would cause the storage limit of the device.	of at least 36 e reads beyond
	9)	All other "proprietary" or unspecified devices on IB-M define their own limits, but designers should be awa "proxy" access and IB-to-IBML transactions will limi IB-ML transactions that can be driven through a CM	ML are allowed to are that the CME t the size of any IE or MME.
	h	nplementation Note	
	/ d d	Applications should be aware that proxy operations, u ata between interfaces, will introduce additional over uce the data payload that can be transferred.	used to transfer head that will re-

13.6.2 BASEBOARD MAD COMMANDS (BM MAD ATTRIBUTES)

Table 136lists the named attributes and bitfields that constitute the "commands" used for managing the Module via the Baseboard Management23344

Table 136 Baseboard MAD Commands

Command (Description Section)	Request data	Response data	Facility 7 Reference 8
<u>lb2lbML</u> (<u>13.6.3.1</u>)	(3+NBW)x8 bits <u>byte 1:</u> device selector <u>byte 2:</u> # bytes to write (NBW) <u>byte 3 to NBW+2:</u> write data bytes (if NBW is 0, this byte is absent) <u>byte NBW+3:</u> # bytes to read (NBR)	(1+NBR)x8 bits <u>byte 1:</u> completion status ^a <u>bytes 2+:</u> read data bytes (if any)	1 1 1 1 1
<u>lb2CME</u> (<u>13.6.3.2</u>)	(1+NBW)x8 bits <u>byte 1:</u> # bytes to write <u>byte 2+:</u> write data bytes (see text)	(1+NBR)x8 bits <u>byte 1:</u> completion status ^a <u>bytes 2+:</u> read data bytes (if any)	1
<u>Ib2MME</u> (<u>13.6.3.3</u>)	(1+NBW)x8 bits <u>byte 1:</u> #bytes to write <u>byte 2+:</u> write data bytes (see text)	(1+NBR)x8 bits <u>byte 1:</u> completion status ^a <u>bytes 2+:</u> read data bytes (if any)	1 1 2
<u>OEM</u> (<u>13.6.3.4</u>)	3x8 + vendor-specific number of bits bytes 1:3: vendor ID bytes 4+: vendor-specific data	 4x8 + vendor-specific number of bits <u>byte 1:</u> completion status^a (vendor defined) <u>bytes 2:4:</u> vendor ID <u>bytes 5+:</u> vendor-specific response data 	2 2 2 2 2
<u>WriteVPD</u> (<u>13.6.3.5</u>)	(5+NBW)x8 bits <u>byte 1:</u> VPD device selector (address) <u>bytes 2:3</u> # bytes to write (NBW: 2 bytes, 1-based. 0 allowed) <u>bytes 4:5</u> VPD offset to write (2 bytes, 0-based) <u>byte 6+:</u> write data bytes (NBW bytes)	8 bits <u>byte 1:</u> completion status ^a	2 2 2 3 3 3 3 3
<u>ReadVPD</u> (<u>13.6.3.6</u>)	5x8 bits <u>byte 1:</u> VPD device selector (address) <u>bytes 2:3</u> VPD number of bytes to read (NBR: 2 bytes. 1-based. 0 allowed) <u>bytes 4:5</u> VPD offset to read (2 bytes)	(1+NBR)x8 bits <u>byte 1:</u> completion status ^a <u>bytes 2+:</u> read data bytes (if any)	3 3 3 3 3 3 4 4

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Command (Description Section)	Request data	Response data	Facility Reference
<u>GetModuleStatus</u>	none	6x8 bits	
(<u>13.6.3.16</u>)		byte 1: completion status ^a	
		<u>byte 2:</u> Removal status	
		7 - <u>Module_OKTR</u>	<u>13.4.2.1</u>
		6 - <u>MME_RTR</u>	<u>13.4.2.4</u>
		5 - <u>MME_CTR</u>	<u>13.4.2.5</u>
		4 - <u>CME_Force_OKTR</u>	<u>13.4.2.6</u>
		3 - <u>CME_RTR</u>	<u>13.4.2.7</u>
		2 - <u>CME_CTR</u>	<u>13.4.2.8</u>
		1 - <u>SW_CTR</u>	<u>13.4.2.9</u>
		0 - <u>SW_RTR</u>	<u>13.4.2.10</u>
		byte 3: Module Attention	
		7:4 - reserved	
		3 - Module Identify	13.4.3.1
		2 - MME Module Attention	13.4.3.3
		1 - CME Module Attention	<u>13.4.3.4</u>
		0 - SW Module Attention	<u>13.4.3.5</u>
		byte 4: Attention source	
		7:6 - reserved	
		5 - CME RTR Trap Timeout	13.4.4.1
		4 -Power Converter Fault	13.4.4.2
		3 -Environmental_Fault	13.4.4.3
		2 - Reserved	
		1 - <u>Functional Fault</u>	<u>13.4.4.4</u>
		0- Predictive Fault	<u>13.4.4.7</u>
		byte 5: Power/environmental status	
		7 - Cooling Non Crit	13.4.4.8
		6 - <u>Cooling Crit</u>	<u>13.4.4.9</u>
		5 - Cooling Non Recoverable	<u>13.4.4.10</u>
		4 - <u>Voltage Crit</u>	<u>13.4.4.11</u>
		3 - Voltage Non Recoverable	<u>13.4.4.12</u>
		2 - <u>Module_Power_On</u>	<u>13.4.4.13</u>
		1:0 - Pwr Conv Redundancy	<u>13.4.5.1</u>
		byte 6: LED Status	
		7 - reserved. Return as 0b	13.436
		6:5 - Attention LED State	<u></u>
		4:3 - Module Status LED State	13.4.3.7
		2 - Module Identify	13.4.3.1
		1 - LED Enable	13.4.3.8
		0 - LED_Test	13.4.3.9

Table 136 Baseboard MAD Commands

Command (Description Section)	Request data	Response data	Facility Reference
<u>ResetIbML</u> (<u>13.6.3.7</u>)	none	8 bits <u>byte 1: c</u> ompletion status ^a 01h = could not clear bus	
SetModuleState (13.6.3.14)	8 bits <u>byte 1:</u> Removal Control 7:2 - reserved 1 - <u>SW_CTR</u> 0 - <u>SW_RTR</u>	8 bits <u>byte 1: c</u> ompletion status ^a	<u>13.4.2.9</u> <u>13.4.2.10</u>
SetModuleAttention (13.6.3.15)	8 bits <u>byte 1:</u> Module Attention 7:4 - reserved 3 - <u>Assert_Identify</u> 2 - reserved 1 - <u>Initiate_LED_Test</u> 0 - <u>SW_Module_Attention</u>	8 bits <u>byte 1: c</u> ompletion status ^a	<u>13.4.3.1</u> <u>13.4.3.10</u> <u>13.4.3.5</u>
Power Control ^b			
SetModulePMControl (13.6.3.8)	8 bits <u>byte 1:</u> control $00h = M_{On}$ $05h = M_{Standby}$ Others = reserved	8 bits <u>byte 1:</u> completion status ^{c a}	<u>14.4</u>
GetModulePMControl (13.6.3.9)	none	2x8 bits <u>byte 1:</u> completion status ^a <u>byte 2:</u> Module Power State ^d 00h = M _{On} 05h = M _{Standby} 06h = M _{NoWake} Others = reserved	14.4
SetUnitPMControl (13.6.3.10)	8 bits <u>byte 1:</u> control 00h =U $_{On}$ 04h =U $_{Sleep}$ 05h =U $_{Standby}$ Others = reserved	8 bits <u>byte 1:</u> completion status ^a	<u>14.5</u>

Table 136 Baseboard MAD Commands

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Command (Description Section)	Request data	Response data	Facility Reference
GetUnitPMControl (13.6.3.11)	none	2x8 bits <u>byte 1:</u> completion status ^a <u>byte 2: Unit P</u> ower State $00h = U_{On}$ $04h = U_{Sleep}$ $05h = U_{Standby}$ Others = reserved	<u>14.5</u>
<u>SetIOCPMControl</u> (<u>13.6.3.12</u>)	2x8 bits byte 1: OC Selector byte 2: control 7 - WRE Status 6 - WRE Enable 5:4 - Reserved 3:0 - <u>IOC Power States</u> $Oh = I_{Operational}$ $1h = I_{Uninit}$ $2h = I_{Doze}$ $3h = I_{Nap}$ $4h = I_{Sleep}$ $5h = I_{Standby}$ 6h-Fh = reserved	8 bits byte 1: completion status ^a	<u>13.4.5.8</u> <u>13.4.5.7</u> <u>14.6</u>
<u>GetIOCPMControl</u> (<u>13.6.3.13</u>)	8 bits byte 1: IOC Selector	2x8 bits <u>byte 1:</u> completion status ^a <u>byte 2:</u> control 7 - <u>WRE_Status</u> 6 - <u>WRE_Enable</u> 5:4 - Reserved 3:0 - <u>IOC Power States</u> Oh = I <i>Operational</i> 1h = I <i>Uninit</i> 2h = I <i>Doze</i> 3h = I <i>Nap</i> 4h = I <i>Sleep</i> 5h = I <i>Standby</i> 6h-Fh = reserved	<u>13.4.5.8</u> <u>13.4.5.7</u> <u>14.6</u>

Table 136 Baseboard MAD Commands

a. The completion status field uses the values defined in <u>Table 135</u>. Additional completion status values that may pertain to a given command are enumerated.

- 37 38
- 39 40
- 10
- 41 42

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14

b. Power state value assignments used in this table are:

- 0h = Operational or On
- 1h = Uninit 2h = Doze

3h = Nap

4h = Sleep

5h = Standby

6h = NoWake

c. The Module **shall** return the *response* to the BM MAD before attempting to perform the requested command. See <u>Section 13.6.1.2, "Delivering Request Messages to the MME," on page 555</u>.

d. The Module is not expected to respond to BM MADs when it is not in Mon power state.

13.6.3 BASEBOARD MAD COMMAND DESCRIPTIONS

13.6.3.1 IB2IBML

	The <i>Ib2IbML</i> command provides the facility for driving a low-level IB-ML transaction via a Baseboard Management MAD. There are three types of transaction supported: An Atomic Write, Atomic Read, and Atomic Write-Read. If the transaction is successful, the response to this command will return an "OK" completion status value and the requested IB-ML data (if any). If the MME cannot complete the transaction because of an IB-ML bus error, the corresponding non-zero completion status will be returned in the response. See <u>Section 13.6.1</u> , "IB-to-MME (Baseboard MAD) Commands," on page 549 for more information.	 15 16 17 18 19 20 21 22
	A <i>request</i> for an Atomic Write-Read operation specifies the Selector for the targeted Device, the number of data bytes to write (NBW: # bytes to write), NBW bytes of Write data, and the number of data bytes to Read (NBR: # bytes to read). It delivers (3+NBW)x8 bits.	23 24 25 26 27
	The <i>response</i> to an Atomic Write-Read operation returns a <i>completion status</i> and NBR bytes of Read data. It returns (1+NBR)x8 bits.	28 29
13.6.3.2 Ів2СМЕ		30 31
	The <i>Ib2CME</i> command provides the facility for delivering a split-transac- tion request or response message to the CME via IB-ML using a Base- board Management MAD. The MME takes the parameters of this command and creates the corresponding CME IB-ML message. If MME is able to successfully transmit the message to the CME, the response will contain an "OK" completion status. If the MME cannot perform the transfer because of an IB-ML bus error, the corresponding non-zero completion status will be returned in the response. Note that the response to this com- mand only indicates that the message was successfully transferred to the CME. It does not indicate whether the CME was able to process the mes- sage. See <u>Section 13.6.1.4</u> , "IB-ML Split-transaction Messaging," on page 561 for more information.	32 33 34 35 36 37 38 39 40 41 42

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	All protocol-aware Modules provides the Ib2CME mented physical IB-MLs. Non-Module forms of p abstract IB-ML and perform Ib2CME function. So <u>MAD Command Requirements on page 580</u> .	command to their imple- ackaging may choose to ee <u>Table 137 Baseboard</u> 2 3	
13.6.3.3 Ів2ММЕ		5	
	The <i>Ib2MME</i> command provides the facility for a tion request or response message to the MME u agement MAD. The transaction is formatted the se delivered to a device on IB-ML, although there is be physically implemented that way. If MME accessonse will contain an "OK" completion status. Of sponding non-zero completion status will be returned to the MME. It does not indicate whether the message. See <u>Section 13.6.1.4, "IB-ML Splitton page 561</u> for more information.	delivering a split-transac- using a baseboard man- same way as if it is being s no requirement for it to epts the message, the re- otherwise, the corre- urned. Note that the was successfully trans- the MME has processed -transaction Messaging."	0 1 2 3 4 5 6
13.6.3.4 OEM		1	7
	The OEM optional command provides a mechan board management MADs to a vendor-specific f The request parameters include the id of the ver remaining data parameters in the request. If this a the MME shall provide a response with a compl tribute not supported". If the command is suppor vendor ID, an "Illegal request parameter" complet turned.	nism for sending base- function within an MME. 11 ndor that has defined the attribute is not supported, 2 letion status value of "At- ted, but not for the given etion status shall be re-	8 9 1 2 3 4 5
13.6.3.5 WRITEVPD		2	6
	The <i>WriteVPD</i> command provides the mechanis VPD devices, including the ModuleInfo and the of selector parameter in the request holds the "slave vice to be accessed. For Chassis VPD devices, quest parameters and formats a physical IB-ML tr VPD using a 24C02 SEEPROM style access. Fi format of such a SEEPROM write transaction or this type of access is also shown in Figure 168 I page 559.	sm for writing to different ChassisInfo. The device e address" of the VPD de- the MME takes the re- ransaction to the Chassis <u>gure 174</u> shows the n IB-ML. An example of <u>B-to-IB-ML Access on</u> 33	, 8 9 0 1 2 3 4 5
	As long as the baseboard management MAD is ware does not care whether Module VPD is imp SEEPROM on IB-ML, or not. Thus, Module VPD as a physical SEEPROM device on the IB-ML, in would format the same type of IB-ML transaction access. While a different implementation may imp using proprietary hardware, in which case the MM	handled correctly, soft- lemented as a physical could be implemented n which case the MME as used for Chassis VPD plement the Module VPD ME would be responsible	6 7 8 9 0 1 2

for translating the command and performing whatever steps necessary to perform an equivalent write to the Module VPD.

If the write transaction is performed successfully, The MME **shall** return a response with an "OK" completion status value. Otherwise, the MME **shall** return an appropriate non-zero completion status value.

IB-ML 'SEEPROM Write'



IB-ML 'SEEPROM Read'

s	Device Address (e.g. 1010_100_b for Chassis VPD)	A	offset into SEEPROM	A	S	Device Address (e.g. 1010_000_b for Module VPD)	1	A	read data byte 1	A	read data byte 2	A		read data byte N	Ā	Ρ	
---	--	---	------------------------	---	---	---	---	---	------------------------	---	------------------------	---	--	------------------------	---	---	--

Figure 174 IB-ML SEEPROM Access Formats

Architectural Note

The *WriteVPD* Number of Bytes to Write (NBW) field is defined to be 2 bytes so as to 1) allow for larger data abstraction implementations that may not use physical IB-ML devices that are limited to 256B of address ability and 2) to accommodate emerging physical devices that allow for 16KB of addressablity.

13.6.3.6 READVPD

The **ReadVPD** command is similar to the **WriteVPD** command, except that if the access is successful the response will include the requested VPD data in addition to with the completion status value. See Figure 174 for the IB-ML format of a SEEPROM read.

Architectural Note

The *ReadVPD* Number of Bytes to Read (NBR) field is defined to be 2 bytes so as to 1) allow for larger data abstraction implementations that may not use physical IB-ML devices that are limited to 256B of address ability and 2) to accommodate emerging physical devices that allow for 16KB of addressablity.
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13.6.3.7 RESETIBML

The **ResetIbML** command directs the MME to reset its IB-ML Agent function. If the command is successful, the response **shall** return an "OK" completion status value. Otherwise, the MME shall return an appropriate non-zero (error) completion status value.

Implementation Note

Optionally, the MME can attempt to restore a "hung" IB-ML bus state by clocking "1" data bits onto the bus until it sees the data line go high, at which time it can issue a STOP condition. For this operation to be successful, the hung bus condition must not render the IB-ML Agent's master function un-operational.

13.6.3.8 SETMODULEPMCONTROL

If ModulePowerInfo.ModulePMCapability.IsPowerManagedSupported=1b, the SETMODULEPMCONTROL command shall allow access to the current Power Management state for the Module as defined in Section 14.4, "Module Power States," on page 643.

If ModulePowerInfo.ModulePMCapability.IsPowerManagedSupported=0b, the SETMODULEPMCONTROL command shall not cause any updates, not produce any side effects, and return a non-zero completion status value in the response that accompanies this command.

Valid states are indicated through ModuleInfo.PmCapablity facility (see Section 13.3.2.10, "ModuleInfo Device," on page 517).

Issuing this command with an unsupported state value shall not result in any update to the state.

13.6.3.9 GETMODULEPMCONTROL

If ModulePowerInfo.ModulePMCapability.IsPowerManagedSupported=1b, the GETMODULEPMCONTROL command shall allow access to the current Power Management state for the Module as defined in Section 14.4, "Module Power States," on page 643.

If ModulePowerInfo.ModulePMCapability.IsPowerManagedSupported=0b, the GETMODULEPMCONTROL command shall always produce 00h as the state. 36

Valid states are indicated through ModuleInfo.PmCapablity facility (See Section 13.3.2.10, "ModuleInfo Device," on page 517).

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13.6.3.10 SETUNITPMCONTROL

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	If ModulePowerInfo.ModulePMCapability.IsPowerManagedSup- ported=1b, the SETUNITPMCONTROL command shall allow access to the current I/O Unit Power Management state as defined in <u>Section 14.5, "I/O</u>	1 2 3
	Unit Power States," on page 646 for the addressed IOC.	4 5
	If ModulePowerInfo.ModulePMCapability.IsPowerManagedSup-	6
	dates, not produce any side effects, and return a non-zero completion status value in the response that accompanies this command.	7 8 0
	Valid states are indicated through <i>ModuleInfo.UnitPmInfo</i> facility (see <u>Section 13.3.2.10, "ModuleInfo Device," on page 517</u>).	10 11
	Issuing this command with an unsupported state value shall not result in any update to the state.	12 13
		15
IS.0.3.11 GETUNITPWICONTROL	If Madula Bowarlata Madula BMC anability la Bowar Managad Sun	16
	ported=1b, the GetUnitPMControl command shall allow access to the	17
	Power Management state for the I/O Unit as defined in Section 14.5, "I/O	18
	Unit Power States," on page 646.	20
	If ModulePowerInfo.ModulePMCapability.IsPowerManagedSup-	21
	<i>ported</i> =0b, the <i>GETUNITPMCONTROL</i> command shall always produce 00h as the state.	22 23
	Valid states are indicated through <i>ModuleInfo.UnitPmInfo</i> facility (see Section 13.3.2.10, "ModuleInfo Device," on page 517).	24 25
	,	26
13.6.3.12 SETIOCPMCONTROL		27
	If ModulePowerInto.ModulePMCapability.IsPowerManagedSup-	20 29
	current IOC Power Management state as defined in <u>Section 14.6. "IOC</u>	30
	Power States," on page 648 for the addressed IOC.	31
		32
	It ModulePowerInto.ModulePMCapability.IsPowerManagedSup- ported=0b the SETIOCPMCONTROL command shall not cause any up-	33
	dates, not produce any side effects, and return a non-zero completion	35
	status value in the response that accompanies this command.	36
	Valid states are indicated through Madulalate 1000 - late to slite the	37
	Section 13.3.2.10, "ModuleInfo Device," on page 517).	38 39
	Issuing this command with an unsupported state value shall not result in any update to the state.	40 41
		42

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13.6.3.13 GETIOCPMCONTROL		4
	If ModulePowerInfo.ModulePMCapability.IsPowerManag ported=1b, the GETIOCPMControl command shall allo Power Management state for the IOC as defined in <u>Sect</u> <u>Power States," on page 648</u> .	vedSup- 2 w access to the 3 ion 14.6, "IOC 4 5
	If ModulePowerInfo.ModulePMCapability.IsPowerManag ported=0b, the GETIOCPMControl command shall alwa as the state.	edSup-6 ays produce 00h 8 9
	Valid states are indicated through <i>ModuleInfo.IOCPmInfo</i> <u>Section 13.3.2.10, "ModuleInfo Device," on page 517</u>).	o facility (see 10
13.6.3.14 SETMODULESTATE		12
	The SetModuLeState command provides update access SW_CTR and SW_RTR facilities in support of Module Gr See also <u>Section 13.3.2.4</u> , "Graceful Hot Removal," on p	es to the 14 aceful Removal. 15 age 503. 16
13.6.3.15 SETMODULEATTENTIO	Ν	18
	The SETMODULEATTENTION command provides control a tention LED and to initiate the Identify function. See also Section 13.3.2.6.4, "Attention (Amber) LED," on page 51 Section 13.3.2.6.7, "Module Identify," on page 513.	ccess to the At- 19 20 20 2 and 21 22 22
13.6.3.16 GETMODULESTATUS		23
	The GetModuleStatus command provides access to the cilities on a Module. The facilities accessible by this com cated by the Facility Reference column for <u>GetModuleState</u>	e state of the fa- mand are indi- tus in <u>Table 136</u> . 27 28
13.6.4 BASEBOARD MAD COM	IMAND REQUIREMENTS	29
	This section defines the required and optional command types of InfiniBand devices and physical packages.	s for various 30 31 32
	The column cells of Table 137 shall have the following d	efinition: 33
	 Req - A Module shall implement the command lat "Requirement" column. 	beled Req in the 35 36
	 Rec - A Module may implement the command lat "Requirement" column. It is recommended that the provided. If the command is provided, the Module provisions of the command description section. If not provided, the Module shall silently drop the M the command. 	beled Rec in the 37 be command be 38 shall follow the 39 the command is 40 AD containing 41

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	• Opt - The Module may implement the facility command is provided, the Module shall do s the provisions of the command description s mand is not provided, the MAD containing the ly dropped.	y if so labeled. If the so in accordance with section. If the com- ne command is silent-	1 2 3 4
	 N/A - The command is not applicable to the dressed. The MAD containing the command 	package being ad- l is silently dropped.	5 6
	C13-43: An InfiniBand defined Module containing at aware device shall provide those facilities labeled a tocol-aware Module" column of <u>Table 137</u> .	n InfiniBand protocol- as " Req " in the "Pro-	7 8 9
	C13-44: An InfiniBand defined Module not containing tocol-aware device shall provide those facilities labe "Non-Protocol-aware Module" column of <u>Table 137</u> .	ng an InfiniBand pro- eled as " Req " in the	10 11 12 13
	C13-45: An InfiniBand Channel Adapter device mou other than an InfiniBand Module shall provide those " Req " in the "Non-Module xCA" column of <u>Table 137</u>	unted on a package e facilities labeled as <u>7</u> .	14 15 16
	C13-46: An InfiniBand Switch device mounted on a an InfiniBand Module shall provide those facilities la "Non-Module Switch" column of <u>Table 137</u> .	package other than beled as " Req " in the	17 18 19 20
	C13-47: An entity that implements Baseboard MAD here to <u>Section 13.6.1, "IB-to-MME (Baseboard MAD page 549, Section 13.6.2, "Baseboard MAD Comma tributes)." on page 570, and <u>Section 13.6.3, "Baseboard Descriptions," on page 574</u>.</u>	Commands shall ad- <u>D) Commands," on</u> ands (BM MAD At- oard MAD Command	21 22 23 24 25
	C13-48: An entity that implements IB-ML operations requirements of <u>Section 13.6.1.11</u> , "Maximum Trans Lengths," on page 568.	s shall adhere to the saction / Message	26 27 28
	Table 137 Baseboard MAD Command Requ	uirements	29 30

Register	Protocol- aware Module	Non-Protocol- aware Module	Non-Module xCA ^a	Non-Module Switch ^a
Ib2IbML	Req	N/A	Opt	Opt
Ib2CME	Req	N/A	Opt ^b	Rec ^b
Ib2MME	Opt	N/A	Opt	Opt
<u>OEM</u>	Opt	N/A	Opt	Opt
<u>WriteVPD</u>	Req	N/A	Req	Req
ReadVPD	Req	N/A	Req	Req
	I	I	1	1

Table 137 Baseboard MAD Command Requirements

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Register	Protocol- aware Module	Non-Protocol- aware Module	Non-Module xCA ^a	Non-Module Switch ^a
<u>ResetIbML</u>	Req	N/A	Opt	Opt
SetModulePMControl	Opt	N/A	Opt	Opt
GetModulePMControl	Opt	N/A	Opt	Opt
SetUnitPMControl	Opt	N/A	Opt	Opt
GetUnitPMControl	Opt	N/A	Opt	Opt
SetIOCPMControl	Opt	N/A	Opt	Opt
GetIOCPMControl	Opt	N/A	Opt	Opt
SetModuleState	Req	N/A	Opt	Opt
SetModuleAttention	Req	N/A	Opt	Opt
GetModuleStatus	Req	N/A	Opt	Opt

Table 137 Baseboard MAD Command Requirements

a. (See Section 13.3.2.1, "BMA," on page 495 and Table 120 Module Feature Requirements on page 494) All protocol-aware InfiniBand devices shall support ReadVPD and WriteVPD.
b. The IB2CME command is required to perform the <u>IB-ML Selector Proxy</u> function (See <u>13.5.2.6 on page 548</u>).

13.6.5 MME FUNCTION REGISTERS

IB-ML access to the MME is accomplished by reading and writing to "registers" within a device address that operate on facilities on the Module. Another device address provides for IB-ML to IB messaging whereby message data are provided to the MME which, in turn, forwards correspondingly formatted data to the BMA for delivery to the InfiniBand media via the channel adapter.

<u>Table 138</u> and <u>Table 139</u> illustrate the format of the IB-ML atomic Write-Read transactions used to access MME Registers.

Table 138 MME Register Write from IB-ML^a

IB-ML	data direction
START condition	
MME Slave Address 0	into MME
Register Selector	into MME
# bytes to read from register = 00h	into MME
data to write to register (N bytes)	into MME
PEC	into MME

Table 138 MME Register Write from IB-ML^a

IB-ML	data direction
START condition	
MME Slave Address 1	into MME
Register Selector	out from MME
completion status: 00h = OK 01h = PEC error in write ^b 02h = illegal register selector 03h = illegal write length 04h = illegal read count	out from MME
PEC	out from MME
STOP condition	

a. The rows in this table correspond to successive operations on IB-ML.

b. The MME ACKs the PEC byte in the write-portion of the transaction, even if the PEC is in error. This is done in order to allow it to return an explicit completion status indicating the PEC error was detected.

Table 139 MME Register Read from IB-ML^a

IB-ML	data direction
START condition	
MME Slave Address 0	into MME
Register Selector	into MME
# bytes to read from register = N	into MME
PEC	into MME
START condition	
MME Slave Address 1	into MME

Table 139 MME Register Read from IB-ML^a

IB-ML	data direction
Register Selector	out from MME
completion status:	out from MME
00h = OK	
01h = PEC error in write ^b	
02h = illegal register selector	
03h = illegal write length	
04h = illegal read count	
ead data from register (N bytes)	out from MME
PEC	out from MME
STOP condition	
The rows in this table correspond to suc	ccessive operations on IB-
. The MME ACKs the PEC byte in the wr	ite-portion of the
ansaction, even if the PEC is in error. This	is is done in order to allow
to return an explicit completion status ind	icating the PEC endr was

13.6.6 MME FUNCTION REGISTER SUMMARY

<u>Table 140</u> lists the named registers, their selector indication, and the fields that are used for managing a Module using the IB-ML Device Address for "MME Function" defined in <u>Table 121 Module IB-ML Slave Addresses on page 496</u>.

Deviator	Write Data		Read Data	
(Selector)	Description	Facility Refer	Description	Facility Refer
Interrupt- ClearStatus (00h)	Writing a "0" clears the correspond- ing interrupt capture flag. Writing a "1" causes no change. <u>byte 1:</u> 7:6 - reserved. Write as 11b. 5 - <u>Attention Status Change</u> 4 - <u>Removal Status Change</u> 3 - <u>Power Converter Fault</u> 2 - <u>Environmental Fault</u> 1 - <u>Functional Fault</u> 0 - <u>Predictive Fault</u>	<u>13.4.2.2</u> <u>13.4.2.3</u> <u>13.4.4.2</u> <u>13.4.4.3</u> <u>13.4.4.4</u> <u>13.4.4.4</u>	 "1" indicates which source has had a state change captured. If enabled, that change will be contributing to the interrupt signal. byte 1: 7:6 - reserved. Return as 00b. 5 - Attention Status Change 4 - Removal Status Change 3 - Power Converter Fault 2 - Environmental Fault 1 - Functional Fault 0 - Predictive Fault 	<u>13.4.2.2</u> <u>13.4.2.3</u> <u>13.4.4.2</u> <u>13.4.4.3</u> <u>13.4.4.4</u> 13.4.4.7
	byte 2: 7 - Cooling Non Crit 6 - Cooling Crit 5 - Cooling Non Recoverable 4 - Voltage Crit 3 - Voltage Non Recoverable 2 - Module Power On 1 - WakeOnIB 0 - WakeOnWRE	13.4.4.8 13.4.4.9 13.4.4.10 13.4.4.11 13.4.4.12 13.4.4.13 13.4.5.2 13.4.5.3	byte 2: 7 - <u>Cooling Non Crit</u> 6 - <u>Cooling Crit</u> 5 - <u>Cooling Non Recoverable</u> 4 - <u>Voltage Crit</u> 3 - <u>Voltage Non Recoverable</u> 2 - <u>Module Power On</u> 1 - <u>WakeOnIB</u> 0 - <u>WakeOnWRE</u>	13.4.4.8 13.4.4.9 13.4.4.10 13.4.4.11 13.4.4.12 13.4.4.13 13.4.5.2 13.4.5.3
InterruptSource (01h)	not writable		Presents the present state of the interrupt source. "1" indicates that the corresponding condition is presently asserted, "0" indicates it is presently deasserted. <u>byte 1:</u> 7:6 - reserved. Return as 00b. 5 - Attention Status Change 4 - Removal Status Change 3 - Power Converter Fault 2 - Environmental Fault 1 - Functional Fault 0 - Predictive Fault <u>byte 2:</u> 7 - Cooling Non Crit 6 - Cooling Crit 5 - Cooling Non Recoverable 4 - Voltage Crit 3 - Voltage Non Recoverable 2 - Module Power On	$\begin{array}{r} 13.4.2.2\\ 13.4.2.3\\ 13.4.4.2\\ 13.4.4.3\\ 13.4.4.4\\ 13.4.4.7\\ 13.4.4.8\\ 13.4.4.9\\ 13.4.4.10\\ 13.4.4.12\\ 13.4.4.13\end{array}$
			1 - <u>WakeOnIB</u> 0 - <u>WakeOnWRE</u>	<u>13.4.5.3</u>

Table 140 MME Function Registers

Pagistor	Write Data		Read Data	
(Selector)	Description	Facility Refer	Description	Facility Refer
InterruptControl	Writing a "1" enables the correspond-		"1" indicates which interrupt capture	
(02h)	ing interrupt capture flag to contribute		flags are enabled.	
	to the interrupt signal.		buto 1	
	7:6 reserved Write as 11b		Zie received Beturn as 00b	
	5 Attention Status Change		5 Attention Status Change	13.4.2.2
	4 - Removal Status Change	<u>13.4.2.2</u>	4 - Removal Status Change	13.4.2.3
	3- Power Converter Fault	<u>13.4.2.3</u>	3 - Power Converter Fault	13.4.4.2
	2 - Environmental Fault	<u>13.4.4.2</u>	2 - Environmental Fault	13.4.4.3
	1 - Eunctional Fault	13.4.4.3	1 - Eunctional Fault	13.4.4.4
	0 - Predictive Fault	13.4.4.4	0 - Predictive Fault	13.4.4.7
	byte 2:	<u>13.4.4.7</u>	byte 2:	
	7 - Cooling Non Crit	13//8	7 - Cooling Non Crit	13.4.4.8
	6 - Cooling Crit	13/10	6 - Cooling Crit	<u>13.4.4.9</u>
	5 - Cooling Non Recoverable	<u>13,4,4,5</u> 13,4,4,10	5 - Cooling Non Recoverable	<u>13.4.4.10</u>
	4 - Voltage Crit	<u>134411</u>	4 - Voltage Crit	<u>13.4.4.11</u>
	3 - Voltage_Non_Recoverable	13 4 4 12	3 - Voltage_Non_Recoverable	<u>13.4.4.12</u>
	2 - Module Power On	13.4.4.13	2 - Module Power On	<u>13.4.4.13</u>
	1 - WakeOnIB	13.4.5.2	1 - WakeOnIB	<u>13.4.5.2</u>
	0 - <u>WakeOnWRE</u>	13.4.5.3	0 - <u>WakeOnWRE</u>	<u>13.4.5.3</u>
LEDTestStatus	byte 1:		byte 1:	
(03h)	7:3 - reserved. Write as 000000b		7 - reserved. Return as 0b	
			6:5 - Attention LED State	13.4.3.6
			4:3 - Module Status LED State	13.4.3.7
	2 - Assert Identify	13.4.3.2	2 - Module Identify	<u>13.4.3.1</u>
	1 - <u>LED_Enable</u>	13.4.3.8	1 - <u>LED_Enable</u>	<u>13.4.3.8</u>
	0 - Initiate LED Test	<u>13.4.3.10</u>	0 - <u>LED_Test</u>	<u>13.4.3.9</u>
	byte 2: Module Attention control		byte 2: Module Attention status	
	7:2 - reserved		7:6 - reserved	
			5 - <u>Hard Fault</u>	<u>13.4.4.5</u>
			4 - <u>Degraded Fault</u>	<u>13.4.4.6</u>
			3 - reserved	<u>13.4.3.1</u>
	1 - <u>CME Module Attention</u>		2 - MME Module Attention	<u>13.4.3.3</u>
	0 - reserved	<u>13.4.3.4</u>	1 - <u>CME Module Attention</u>	<u>13.4.3.4</u>
			0 - <u>SW_Module_Attention</u>	<u>13.4.3.5</u>
ModuleControl-	byte 1:		byte 1:	
<u>Status</u>	7 - CME RTR Trap Timeout	<u>13.4.4.1</u>	7 - CME RTR Trap Timeout	<u>13.4.4.1</u>
(04h)	6:3 - reserved. Write as 00000b		6 - <u>WakeOnIB</u>	<u>13.4.5.2</u>
			5 - <u>WakeOnWRE</u>	<u>13.4.5.3</u>
			4 - <u>IMxInt L State</u>	<u>13.4.5.4</u>
			3 - <u>WRE_Enable</u>	<u>13.4.5.7</u>
	2 - WakeOnIB_Enable	<u>13.4.5.5</u>	2 - <u>WakeOnIB_Enable</u>	<u>13.4.5.5</u>
		1	1 M/DE Status	13458
	1 - reserved		I - WILL Status	10.4.0.0

Table 140 MME Function Registers

Deviator	Write Data		Read Data	
(Selector)	Description	Facility Refer	Description	Facility Refer
<u>IodulePower</u>	byte 1:		byte 1:	
05h)	7:0 - reserved. Write as 0000000b		7:3 - 00000b	
			2 - M _{On}	
			1 - MStandby	
			byte 2	
	byte 2:		7:2 - 000000b	
	7.0 - Teserved. While as 00000000		1:0 - <u>Pwr Conv Redundancy</u>	<u>13.4.5.1</u>
emovalControl-	byte 1: Removal status		byte 1: Removal status	
<u>atus</u>	7:5 - reserved. Write as 000b		7 - <u>Module_OKTR</u>	<u>13.4.2.1</u>
6h)			6 - <u>MME_RTR</u>	<u>13.4.2.4</u>
			5 - <u>MME_CTR</u>	<u>13.4.2.5</u>
	4 - <u>CME_Force_OKTR</u>	<u>13.4.2.6</u>	4 - <u>CME_Force_OKTR</u>	<u>13.4.2.6</u>
	3 - <u>CME_RTR</u>	<u>13.4.2.7</u> 12.4.2.9	3 - <u>CME_RTR</u>	<u>13.4.2.7</u>
	2 - <u>CME CTR</u> 1:0 - reserved Write as 000b	13.4.2.0	1 - SW CTR	<u>13.4.2.0</u> 13.4.2.0
			0 - <u>SW_RTR</u>	<u>13.4.2.10</u>
Reserved for IB				
7Fh:07h)				
DEM				
(FFh:80h)				

Table 140 MME Function Registers

13.6.7 MME FUNCTION REGISTER DESCRIPTIONS

13.6.7.1 INTERRUPTCLEARSTATUS

The *INTERRUPTCLEARSTATUS* register provides a CME access to the facilities listed for <u>InterruptClearStatus</u> in <u>Table 140</u> to perform the "Clear" function upon a "write" and provide state change "Status" upon a "read" as defined in <u>Section 13.3.2.8, "IMxInt L." on page 515</u>.

13.6.7.2 INTERRUPTSOURCE

The *INTERRUPTSOURCE* register provides a CME access to the facilities listed for <u>InterruptSource</u> in <u>Table 140</u> to get current interrupt source status upon a "read" as defined in <u>Section 13.3.2.8, "IMxInt L," on page 515</u>.

13.6.7.3 INTERRUPTCONTROL

The *INTERRUPTCONTROL* register provides a CME access to the facilities listed for <u>InterruptSource</u> in <u>Table 140</u> to control the **IMxInt_L** contribution enabling as defined in <u>Section 13.3.2.8</u>, "IMxInt_L," on page 515.

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13.6.7.4 LEDTESTSTATUS		1
	The <i>LEDTESTSTATUS</i> register provides a CME access to defined in <u>Section 13.3.2.6</u> , "Module Indicators (LEDs), using the facilities listed for <u>LEDTestStatus</u> in <u>Table 140</u>	the Module LEDs 2 <u>" on page 508</u> 3 <u>.</u> 4
13.6.7.5 MODULECONTROLSTATE	JS	5
	The <i>MODULECONTROLSTATUS</i> register provides a CME a of the facilities listed for <u>ModuleControlStatus</u> in <u>Table 1</u>	ccess to the state 6 40. 7
13.6.7.6 MODULEPOWER		9
	The <i>MODULEPOWER</i> register provides a CME access to Module Power Management state defined in <u>Section 14.</u> <u>States," on page 643</u> .	the current 10 4, "Module Power 11 12
	rue	13
13.0.7.7 NEMOVALGONTROLOTA	The <i>REMOVALCONTROLSTATUS</i> register provides a CME cilities listed for <u>RemovalControlStatus</u> in <u>Table 140</u> for the functions described in <u>Section 13.3.2.4</u> , " <u>Graceful H page 503</u> .	access to the fa- use in supporting lot Removal," on
13.6.8 MMF IbMI 2lb REGIST		18
	Table 141 lists the named registers, their selector indicat	ion and the fields 20
	that are used for managing a Module using the IB-ML De	evice Address for 21
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"MME IbML2Ib" defined in Table 121 Module IB-ML Slave Addresses on page 496.

Pogistor	Write Data		Read Data	
(Selector)	Description	Facility Refer	Description	Facility Refer
SendBMTrap (00h)	byte 1: BMTrapDataLength - number of BMTrapData bytes to include in trap byte 2: BMTrapType 00h = Generic MME 01h = OEM MME 02h = CME_RTR 03h = WRE 04h = Generic CME 05h = OEM CME All others - reserved bytes 3:5 - BMTrapTypeModifier varies based on trap type: holds 3-byte OEM ID if Trap Type is OEM MME or OEM CME. holds SlotSelector, 00h, 00h if trap type is CME_RTR holds 00h,00h,00h (reserved) if Trap Type is Generic MME, WRE, or Generic CME byte 6 + - BMTrapData =data bytes for Trap Type of OEM MME or OEM CME		byte 1: completion status 01h = IB buffer not available (busy) 02h = IB media not ready 03h = Invalid length	
SendlbML2BM (02h)	byte 1: BMDataLength - number of data bytes to include in the Base- board Management data field of the BM MAD starting after the BMSe- quence Field byte 2+ - BMData - data for BM MAD		<u>byte 1:</u> completion status 01h = IB buffer not available (busy) 02h = IB media not ready 03h = Invalid length	

MME IbMI 21b Pogistors Table 444

13.6.9 MME IBML2IB REGISTER DESCRIPTIONS

13.6.9.1 SENDBMTRAP

The SENDBMTRAP register allows the CME to send a "BMTrap" method message to the Baseboard Management LID. The Module uses the components of the **BM.ClassPortInfo** and the "BMTrapType" and "BMTrap-Data" bytes (See SendBMTrap in Table 141) for the "Baseboard Management Data" field to form the datagram message as defined in InfiniBand Architecture Specification, Volume 1, Chapter "General Services", Section "Baseboard Management". The value indicated in the BMTrapDataLength byte (See <u>SendBMTrap</u> in <u>Table 141</u>) must not ex-

ceed the "Baseboard Management Data" field length specified in *Infini-Band Architecture Specification, Volume 1.*

Architecture Note

This register is intended to be used by a CME to communicate with the Baseboard Manager and should be used in lieu of the *SendIBML2BM* register. A node running the Baseboard Manager can use the method in the Baseboard class MAD (BMTrap) to direct the MAD to the Baseboard Manager versus the node's BMA as a BMA is only to act upon BMSend methods with the R bit being 0 (requests). See <u>Table 131</u> Common MAD Field usage for Baseboard Management on page 551.

13.6.9.2 SENDIBML2BM

The SENDIBML2BM register allows the CME to send a "BMSend" method message to the Baseboard Management LID. The Module uses the components of the **BM.ClassPortInfo** and the "IBData" bytes for the "Baseboard Management Data" field to form the datagram message as defined in *InfiniBand Architecture Specification, Volume 1*, Chapter "General Services", Section "Baseboard Management". The value indicated in the IBLength byte (See <u>SendIbML2BM</u> in <u>Table 141</u>) must not exceed the "Baseboard Management Data" field length specified in *InfiniBand Architecture Specification*, Volume 1.

This register is not recommended for use and is subject to removal in future versions of the specification. A CME should use the <u>SendB-MTrap</u> register with "OEM CME" BMTrapType to communicate with the Baseboard Manager. BMTrapType of "Generic CME" is defined as a placeholder for potential future definition of IB2CME.

13.6.10 MME REGISTER REQUIREMENTS

This section defines the required and optional registers for various types of InfiniBand devices and physical packages.

The "Requirement" column cells of <u>Table 142</u> **shall** have the following definition:

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commands at address E4h. An implementation is allowed to make registers available via both the physical and MME command interfaces.

- 4 Rec - A Module may implement the command labeled Rec in the "Requirement" column. It is recommended that the command be provided. If the register is provided, the Module shall follow the 7 provisions of the register description section. If the register is not provided, the Module shall provide the default values for read accesses that are specified for the facility bit(s); write accesses shall not cause updates to occur from the default value for the facilities within the register.
- Opt The Module may implement the facility if so labeled in the 13 "Requirement" column. If the register is provided, the Module 14 shall do so in accordance with the provisions of the register de-15 scription section. If the register is not provided, the Module shall 16 provide the default values for read accesses that are specified for 17 the facility bit(s); write accesses shall not cause updates to occur 18 from the default value for the facilities within the register. 19
- N/A The register is not applicable to the package being addressed. Reads from the register shall return all 0s for the bits designated; writes to the register shall not have any effect.

C13-49: This compliance statement is obsolete and has been replaced by C13-49.1.1:.

C13-49.1.1: An InfiniBand defined Module containing an InfiniBand protocol-aware device shall provide those facilities labeled as "Reg" in the "Protocol-aware Module" column of Table 142.

C13-50: An InfiniBand defined Module not containing an InfiniBand protocol-aware device shall provide those facilities labeled as "Reg" in the "Non-Protocol-aware Module" column of Table 142.

C13-51: An InfiniBand protocol-aware device mounted on a package other than an InfiniBand Module shall provide those facilities labeled as "Reg" in the "Non-Module Device" column of Table 142.

o13-15: An InfiniBand defined Module that implements the facilities labeled as "Rec" or "Opt" in Table 142 shall follow the described specification in Section 13.6.7, "MME Function Register Descriptions," on

page 586 and <u>13.6.11 MME Facilities in Power Management States on</u> page 591.

Register	Protocol- aware Module	Non-Protocol- aware Module	Non-Module Device	
InterruptClearStatus	Req	Req	Opt	
InterruptSource	Req	Req	Opt	
InterruptControl	Req	Req	Opt	
LEDTestStatus	Req	Req	Opt	
ModuleControlStatus	Req	Req	Opt	
ModulePower	Req	Req	Opt	
RemovalControlStatus	Req	Req	Opt	
SendBMTrap	Req	N/A	Opt	
SendlbML2BM	Opt	N/A	Opt	

Table 142 MME Function Register Requirements

13.6.11 MME FACILITIES IN POWER MANAGEMENT STATES

o13-51.1.1: A Module that sets its *ModulePowerInfo.ModulePMCapability.IsPowerManagedSupported to 1b* **shall** provide the following facilities in power management states:

- If MME commands are implemented via IB-ML (at E4h), the <u>GetCMDSetVersion</u> command **shall** be available from IB-ML in all power-managed states.
- If the <u>MME Function Registers</u> are accessible using MME commands via IB-ML, the <u>ReadMMERegister</u> and <u>WriteMMERegister</u> commands **shall** be available from IB-ML in all power-managed states. In this case, the commands **shall** accept the selectors for the <u>LEDTestStatus</u>, <u>ModulePower</u>, and <u>RemovalControlStatus</u> registers.
- The module shall return an 'illegal request parameter' completion status if other IB-specified register selectors are used in the <u>Re-</u> <u>adMMERegister</u> and <u>WriteMMERegister</u> commands, but the register is unavailable due to the power state.
- Similarly, if <u>MME Function Registers</u> are accessible via E0h, an 'illegal request parameter' completion status **shall** be returned for register selectors where the register is not available in a given power state.

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	 For both E0h and E4h accesses, if register a given power state, all facilities for the self functional as specified in Section <u>13.6.6: N</u> <u>Summary</u>. 	r access is provided in ected register shall be <u>1ME Function Register</u> 3
13.6.12 CME COMMANDS		4
	CME commands are split-transaction IB-ML request actions, as described in section <u>13.6.1.4 IB-ML Sp</u> <u>saging on page 561</u> . CME commands are part of th Management command set (<u>Section 13.6.1.7, "IB- Fields," on page 564</u>). The CME performs the request mats a response using the sequence number that quest.	est and response trans- blit-transaction Mes- blit-transaction Mes
	For the standard CME commands (commands oth messages), the Source Device ID in the request of CME delivers the response to the commands. A re- the MME's IbML2Ib function is assumed to have of board Manager. If the Source ID in the request mate- slave address (<u>Table 130: Chassis IB-ML Slave A</u> shall send the response back to the Baseboard M <i>SendIBML2BM</i> MME register or via the SendIbML depending on which is available. Otherwise, the re- as an IB-ML split-transaction response to the slave the Source Device ID in the request.	1 her than OEM CMD letermines where the equest that comes from the Base- ches the MME IbML2Ib ddresses), the CME lanager using the _2BM MME command, esponse shall be sent e address specified by 2
	OEM CME commands are allowed to include parameters of turning the response to the Baseboard Manager are turn the response via other mechanisms.	meters that override re- nd direct the CME to re- 2
	C13-52: Actively Managed Chassis shall implementation tures described in <u>Table 143</u> .	ent a CME with the fea- 2 2
	C13-52.1.1: Actively Managed Chassis shall impl features described in <u>13.2.6 Chassis Managemen</u>	ement a CME with the ² t on page 489.
	Table 143 defines the split-transaction commands sent to the CME Slave Address. See Section 13.6	for CMD Set = IB-ML 3 5.1.7, "IB-ML CMD Set 3
		3 3 3 3 3 3 3 3
		4 4 4

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Specific Fields." on page 564 for CMD field placement in the split-transaction message.

Table 143 CME Commands

Command	CMD	Request data	Response data
GetCMDSetVersion (13.6.12.1)	00h	none	byte 1: completion status ^a byte 2: Version of CME command set (CMD Set = IB-ML) that this controller supports. BCD encoded. Initial value = 10h for CMD Set version 1.0
<u>GetVendorID</u> (<u>13.6.12.2</u>)	01h	none	byte 1: completion status ^a bytes 2+ - A series of one or more 3-byte IDs for each vendor or organization that have defined controller-specific (OEM) com- mands implemented by this CME. FFFFFFh if no controller-specific commands. 3-byte ID uses same format as the vendor ID field in ChassisGUID.
ProxyWriteRead (13.6.12.3)	02h	byte 1: SlotSelector ^b , 1-based byte 2: device selector byte 3: # bytes to write byte 4: write data (if any) byte 5: # bytes to read	byte 1: completion status ^a
<u>ReadVPD</u> (<u>13.6.12.4</u>)	03h	<u>byte 1:</u> SlotSelector ^b , 1-based 00h = No s. Device is directly associated with the CME. <u>byte 2:</u> VPD device selector (address) <u>byte 3</u> VPD number of bytes to read (1 byte. 1-based. 0 count is allowed) <u>bytes 4:5</u> VPD offset to read (2 bytes)	<u>byte 1:</u> completion status ^a <u>byte 2+</u> - read data bytes (if any)
<u>WriteVPD</u> (<u>13.6.12.5</u>)	04h	<u>byte 1:</u> SlotSelector ^b , 1-based. 00h =No proxy. Device is directly associ- ated with the CME. <u>byte 2:</u> VPD device selector (address) <u>byte 3</u> number of bytes to write (1-bytes, 1- based. 0 count is allowed) <u>bytes 4:5</u> VPD offset to write (2-bytes, 0- based) <u>byte 6+:</u> data (N bytes)	<u>byte 1:</u> completion status ^a
<u>OEM</u> (<u>13.6.12.6</u>)	05h	<u>bytes 1-3:</u> vendor ID <u>byte 4+:</u> vendor-specific data	byte 1: completion status ^a bytes 2-4: vendor ID byte 5+: vendor-specific response data

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Table 143	CME	Commands
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Command	CMD	Request data	Response data
OutBandModuleCtl (13.6.12.7)	06h	byte 1: SlotSelector ^b , 1-based. ResetIbML, Reset, or VBxEn_L for the specified slot. byte 2: IB-ML Reset and Module Reset and Power Control bit 7:3 - reserved bit 3 - DisableBulkPower 0 = Do not Disable bulk power via VBxEn_L 1 = Disable bulk power via VBxEn_L bit 2 - reserved bit 1 - ResetModule 0 = Negate IMxPRst 1 = Reset Module via IMxPRst bit 0 - ResetIBML 0 = Do not reset IB-ML 1 = Reset IB-ML	<u>byte 1:</u> completion status ^a 51h = could not clear IB-ML 52h = Module Reset not supported 53h = Module Power Control not supported
ReadModuleCtlStatus (<u>13.6.12.8</u>)	07h	byte 1: SlotSelector ^b , 1-based. Data associ- ated with <u>OutBandModuleCtl</u> for specified slot. byte 2: IB-ML Reset, Module Reset, Module Present and Bulk Power Control Status bit 7:4 - reserved bit 3 - BulkPowerDisabled 0 = Bulk Power is not Disabled via VBxEn_L. 1 = Bulk Power is Disabled via VBxEn_L bit 2:1 - Module IMxPRst 00 = CME is not asserting IMxPRst. 01 = CME is asserting IMxPRst 10 = CME samples IMxPRst as Mod- ule not present. 11 = CME samples IMxPRst as Mod- ule present. bit 0 - ResetIBML 0 = IB-ML is not in reset. 1 = IB-ML is in reset.	byte 1: completion status ^a

a. The completion status field uses the values defined in <u>Table 135</u>. Additional completion status values that may pertain to a given 35 command are enumerated.

b. A non-zero SlotSelector refers to the designating number of an InfiniBand Slot in the Chassis. SlotSelector 0 refers to the CME function which relates to the Chassis itself.

13.6.12.1 GETCMDSETVERSION

GETCMDSETVERSION is an IB-ML split-transaction command that returns 40 the version of the IB-ML command set (CMD Set = IB-ML) implemented 41

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	by the CME. The version information is stored in BCD imal) format, where the most-significant nibble holds in number and the least-significant nibble holds the mine For example, a value of 09h corresponds to IB-ML co 0.9.) (binary coded dec- the major version or version number. mmand set version	1 2 3 4 5
13.6.12.2 GETVENDORID			6
	GetVendorID is an IB-ML split-transaction command for the vendor that has defined controller-specific (CM sages for the CME. The vendor ID format is the same ChassisGUID. If no CMD Set = OEM messages are of 00_00_00h shall be returned in the response. Note the more than one set of vendor-specific commands to be CME.	that returns the ID D Set = OEM) mes- as that used in the defined, a value of nat it is possible for e implemented on a	7 8 9 10 11 12 13
13.6.12.3 PROXYWRITEREAD			14
	ProxyWriteRead, an IB-ML split-transaction command perform a Write-Read transaction to the IB-ML for the CME will perform the requested transaction.	, directs the CME to specified slot. The	15 16 17
13.6.12.4 READVPD			10
	ReadVPD, an IB-ML split-transaction command, allow VPD data from the IB-ML associated with the slot spe <i>lector</i> parameter. A slot selector value of 00h indicates is directly associated with the CME rather than a given command can be used for getting VPD information fro other than the one used to deliver the command to the the CME to act as a "proxy" to access VPD from Mod peater Modules, that lack direct support for providing V the ReadVPD Baseboard Management MAD.	s the CME to return cified by the <i>slot se-</i> s a VPD device that slot. The ReadVPD om a slot (IB-ML) e CME. This allows ules, such as Re- /PD information via	20 21 22 23 24 25 26 27 28
	A CME implementation that receives a ReadVPD CM one IB-ML to read VPD from a slot's IB-ML will typica ters from the request to format an atomic Write-Read I read the VPD SEEPROM on the specified slot's IB-M CME will then take the data read from this transaction a ReadVPD response with a 00h "OK" completion stat countered errors while attempting to access the IB-M appropriate non-zero completion status.	E command from Ily use the parame- B-ML transaction to L. If successful, the and use it to format atus. If the CME en- L, it shall return an	20 29 30 31 32 33 34 35
13.6.12.5 WRITEVPD			36
	WriteVPD, an IB-ML split-transaction command, allow to the VPD device for the slot specified by the slot set slot selector value of 00h indicates a VPD device that ated with the CME rather than a given slot. It can be the able VPD devices of Modules, such as Repeater Modu	vs the CME to write lector parameter. A t is directly associ- for writing into writ- ules, that lack direct	37 38 39 40 41 42

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	support for providing VPD write access via the WriteVP Management MAD. The operation of the WriteVPD CME of the ReadVPD command, except that data from the rea the specified device, and the response does not contain the completion status value.	PD Baseboard E is similar to that quest is written to n data other than	1 2 3 4 5
13.6.12.6 OEM			6
	This IB-ML split-transaction message allows a vendor of define additional CME functions. The message includes that helps ensure that data parameter values specified organization do not interfere or need to be reconciled w lected by another vendor or organization. All other data fied by the vendor or organization identified by the vendor	or organization to a vendor-ID field by one vendor or <i>v</i> ith the values se- fields are speci- dor-ID field.	7 8 9 10 11 12
	The OEM CME command specified here is within the IE Set (<u>Table 143: CME Commands</u>) and shall utilize the s fields (Destination Device ID, Source Device ID, Rs, CM etc.) as the other standard CME commands specified in	B-ML Command same message MD Set, Length, n this section.	13 14 15 16 17
13.6.12.7 OUTBANDMODULECTL			18
	The OUTBANDMODULECTL split-transaction command d control a specific IB-ML, Module bulk power (via VBxEr reset (via IMxPRst).	irects the CME to n_L), and Module	19 20 21 22
	The slot selector value selects the IB-ML and the Modul	e for this function.	23 24
	If the command is supported and successful, the response "OK" completion status value; otherwise, the CME shal priate non-zero (error) completion status value.	se shall return an Il return an appro-	25 26 27
13.6.12.8 READMODULECTLSTA	TUS		28
	The READMODULECTLSTATUS split-transaction command to provide information about IB-ML, Module bulk power and Module reset and presence status (via IMxPRst) for	d directs the CME (via VBxEn_L), or a specific slot.	30 31 32
	The slot selector value selects the IB-ML and the Modul	e for this function.	33 34
	If the command is supported, the response shall return tion status value; otherwise, the CME shall return an ap zero (error) completion status value.	an "OK" comple- ppropriate non-	35 36 37
13.6.13 IB-ML TIMEOUT PARA	METERS		38 39
	C13-53: All Modules shall conform to the parameters lies <u>IB-ML Timeout Parameters on page 597</u> .	sted in <u>Table 144</u>	40 41 42

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o13-16: All non-Modules that implement IB-ML **shall** conform to the parameters listed in <u>Table 144 IB-ML Timeout Parameters on page 597</u>.

C13-54: All Managed Chassis **shall** conform to the parameters listed in <u>Table 144 IB-ML Timeout Parameters on page 597</u>.

13.6.13.1 IB-ML SLAVE TIMEOUT

A slave device always times out when any clock is held low longer than t_{TIMEOUT} maximum. See <u>Figure 175 on page 598</u>.

13.6.13.2 IB-ML MASTER TIMEOUT

 $t_{LOW:SEXT}$ is defined as the cumulative time a master device is allowed to extend its clock cycles within one byte in a message as measured from: 12 13 14

start to ack	15
	16
ack to ack	17
ack to stop	18

See <u>Figure 175 on page 598</u> for a timing diagram depicting this parameter.

Table 144 IB-ML Timeout Parameters

Symbol	Parameter	Minimum	Maximum	Units	Comments
t _{TIMEOUT}	Clock low time-out	25	35	ms	See note ^a
t _{LOW:SEXT}	Cumulative clock low extend time (slave device)		25	ms	See note ^b
t _{LOW:MEXT}	Cumulative clock low extend time (master device)		10	ms	See note ^c
t _{BMTrapRetryPeriod}	BMTrap Retry Period	200	300	ms	See note ^d
t _{BMTrapTimeout}	BMTrap Timeout Period	4	6	s	See note ^d
t _{Module} :CmdTOut	BM Command Timeout		20	ms	See note ^e
t _{CME:NoPrxCmdTOut}	CME Command Timeout while not using a Proxy Command		20	ms	See note ^f
t _{CME:PrxCmdTOut}	CME Command Timeout when using a Proxy Command		50	ms	See note ^f
t _{CME:OEMCmdTOut}	CME Command Timeout for an OEM Command	-	-		Not specified ^f
t _{lbML2lbDelay}	IB-ML to IB message delay		20	ms	See note ^g

a. Devices participating in a transfer will timeout when any clock low exceeds the value of $t_{TIMEOUT}MIN$). Devices that have detected a timeout condition must reset the communication no later than $t_{TIMEOUT}MAX$). The maximum value specified must be adhered to by both a master and a slave as it incorporates the cumulative stretch limit for both a master ($t_{LOW: MEXT}$) and a slave ($t_{LOW: SEXT}$).

b. t_{LOW: SEXT} is the cumulative time a slave device is allowed to extend the clock cycles in one message from the initial start to the stop. If a slave device exceeds this time, it is expected to release both its clock and data lines and reset itself.

c. $t_{LOW: MEXT}$ is the cumulative time a master device is allowed to extend its clock cycles within each byte of a message as defined from start-to-ack, ack-to-ack, or ack-to-stop. A master device **shall not** violate $t_{LOW: MEXT}$ except while forcing a slave device timeout.

d. While awaiting **SW_RTR** bit to be set to 1b, the CME **shall** retry the **BMTrap** message once every t_{BMTrapRetryPeriod} for t_{BMTrapTimeout} Period of time.

e. From the time the IB device receives the entire BM MAD, the amount of time it takes for a Module to respond to a BM command before the Baseboard Manager will have to retry the message

f. Amount of time it takes for a CME to respond to a CME Command from the time the CME receives a CME Command g. The amount of time it takes for a Module to respond to an IbML2Ib register access (IBML -to- IB delay) (form the time the Module receives the IbML2Ib message into the MME's register to the time the Module sends the IB message on the IB) See <u>Section 13.6.8 on page 587</u>.

Figure 175 shows the cycle-to-cycle timeout parameters that are mentioned in <u>Table 144</u>.



Figure 175 IMxDat, IMxClk t_{TIMEOUT} Measurement Intervals

13.7 XINFO FORMAT

The following section describes the format of xInfo such as ChassisInfo, ModuleInfo, FRUInfo, PortConnectionInfo, ModulePowerInfo, CMEInfo, BuddyInfo, and OEM Record used in InfiniBand Chassis and Modules. InfiniBand devices on non InfiniBand-specified form factors may also adopt this format.

13.7.1 OVERVIEW

ModuleInfo and ChassisInfo include Vital Product Data (VPD). VPD, also referred to as Field Replaceable Unit information or FRU data, includes

information for identifying the type and version information of a replaceable unit or an entire system. This often includes elements such as serial numbers and part numbers.

In addition to VPD, ChassisInfo and ModuleInfo include elements that report about the configuration such as the number of slots a Chassis supports, whether a slot provides CME access, power management capabilities for a Module, GUIDs, etc.

The ChassisInfo and ModuleInfo data are stored as a series of typed records. Each record has a record header that indicates the type, version, and size of the data in that record. Following the header is a data area consisting of a number of fixed length and/or variable length fields.

A single device that emulates 24C02 SEEPROM style non-volatile memory may contain several xInfo Records; conversely, an xInfo may be large enough to require extension devices. See <u>Section 13.7.3, "Device Header," on page 603</u>.

There are non-volatile writable regions in xInfo devices into which the CME, the Module, or the Baseboard Manager may write. The data in these specified writable areas follow the OEM Record format. See <u>Table</u> <u>159 OEM Record on page 628</u>.) The Device Header of each device identifies the write-protected regions of that device.

13.7.1.1 NOTATION

Table 145identifies the notations used in the xInfo format tables and de-2scriptions.3

Abbreviation	Description
PA_Module	Protocol-aware InfiniBand Module
IPA_Module	non-Protocol-aware InfiniBand Module
I_ModuleXCA	Non-Module xCA. An xCA that is not on an InfiniBand Module
_ModuleSw	Non-Module Switch. A Switch that is not on an InfiniBand Module
eq_UNA	Required Unspecified Not Allowed (if the Record is present, the field is required to be present and populated with valid data other than the "unspecified" value.)
Peq_UA	Required Unspecified Allowed (if the Record is present, the field is required to be present and populated with valid data.)
eq	Required (if the Record is present, the field is required to be present and populated with valid data. The "unspecified" value is not defined for this field.)
ot	Optional The presence of the field in the Record is optional. If present, the field shall be popu- lated with valid data.

Table 145 Notations used in xInfo Field Descriptions

13.7.2 COMPLIANCE

C13-55: All xInfo devices that a Module implements **shall** be non-volatile memory devices and **shall** conform to the Header and Record definitions in this section. The Module **shall** provide IB-ML access to its xInfo devices when **V**_{Aux} is available on **VA_In**. (See Section 11.4, "Auxiliary Power Group," on page 446.)

C13-56: All xInfo devices that a Chassis implements **shall** be non-volatile memory devices and **shall** conform to the Header and Record definitions in this section.

C13-57: All xInfo devices that a non-Module implements **shall** be non-vol- 3 atile memory devices and **shall** conform to the Header and Record definitions in this section.

C13-58: This statement has been made obsolete by <u>C13-58.1.1:</u>.

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C13-58.1.1: A Protoco Records and their field "Req_UA" in the PA_M uleInfo Record, Section	bl-aware InfiniBand Module shall implement the ds that are labeled " Req ", " Req_UNA ", and Module column of the tables in <u>Section 13.7.6, Mod-</u> on 13.7.8, FRUInfo Record, and Section 13.7.9.	1 2 3
PortConnectionInfo R	ecord. Section 13.7.14. BuddvInfo Record.	4
Section 13.7.10. Mod	ulePowerInfo Record, and Section 13.7.15. As-	5
setTag Record.		5
		0
C13-59: This stateme	nt has been made obsolete by <u>C13-59.1.1:</u> .	/ 8
C13-59.1.1: .A non-Pl the Records and their "Req_UA" in the NPA	rotocol-aware InfiniBand Module shall implement fields that are labeled " Req ", " Req_UNA ", and _ Module column of the tables in <u>Section 13.7.6,</u>	9 10 11 12
ModuleInto Record, S	ection 13.7.8, FRUINTO Record, Section 13.7.9,	13
PortConnectionInto R	ecord, Section 13.7.14, BuddyInto Record,	1/
Section 13.7.10, Mode	ulePowerinto Record, and Section 13.7.15, As-	15
<u>settag Record</u> .		10
		16
o13-17: This stateme	nt has been made obsolete by <u>013-59.1.1:</u> .	17
		18
o13-59.1.1 : A Module	that optionally implements, ChassisInfo Record,	19
<u>CMEInfo Record</u> , or <u>C</u>	DEM Record shall follow the format of the appro-	20
priate sections Section	n 13.7.7, ChassisInfo Record, Section 13.7.12,	21
<u>CMEInfo Record</u> , and	Section 13.7.13, OEM Record respectively.	22
		23
o13-18: A non-Module	e xCA_NID or non-Module Switch_NID that option-	24
ally implements Modu	leInfo Record, ChassisInfo Record, PortConnec-	25
<u>tionInfo Record, Modu</u>	IlePowerInfo Record, IOCPMInfo Record, CMEInfo	20
Record, OEM Record	, FRUInfo Record, BuddyInfo Record or AssetTag	20
Record shall follow th	e format of the appropriate sections Section 13.7.6.	27
<u>ModuleInfo Record, S</u>	ection 13.7.7, ChassisInfo Record, Section 13.7.9,	28
PortConnectionInfo R	ecord, Section 13.7.10, ModulePowerInfo Record,	29
Section 13.7.11. IOCF	² MInto Record, Section 13.7.12, CMEInto Record,	30
Section 13.7.13, OEN	Record, Section 13.7.8, FRUInto Record,	31
Section 13.7.14, Budd	dyinto Record, and Section 13.7.15, Asset lag	32
<u>Record</u> respectively.		33
o13-19: A non-Module	e xCA_ID or non-Module Switch_ID that optionally	34
implements PortConn	ectionInfo Record, ModulePowerInfo Record, IO-	35
<u>CPMInfo Record, CM</u>	EInfo Record, OEM Record, FRUInfo Record, Bud-	36
dyInfo Record or Asse	etTag Record shall follow the format of the	37
appropriate sections	Section 13.7.9, PortConnectionInfo Record,	38
Section 13.7.10, Mod	ulePowerInfo Record, Section 13.7.11, IOCPMInfo	39
Record, Section 13.7.	12. CMEInfo Record, Section 13.7.13. OEM	40
Record, Section 13.7.	8, FRUInfo Record, Section 13.7.14, BuddyInfo	Δ1
Record, and Section	13.7.15, AssetTag Record respectively.	10
		42

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2 3 4
5 6
7 8 9 0
2 3
4 5 6 7 8 9
0 1 2 3 4 5
6 7 8 9 0 1

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	ChassisInfo Device Hea	Record, the ChassisInfo Record shall imr der.	nediately follow the	1
	C13-65: An Record, Por Minfo Record Info Record sections Sec Record, Sec ModulePow Section 13.7	entity that implements <u>ModuleInfo Record</u> <u>tConnectionInfo Record</u> , <u>ModulePowerInf</u> rd, <u>CMEInfo Record</u> , <u>OEM Record</u> , <u>FRUIr</u> or <u>AssetTag Record</u> shall follow the forma <u>ction 13.7.6</u> , <u>ModuleInfo Record</u> , <u>Section</u> <u>ction 13.7.9</u> , <u>PortConnectionInfo Record</u> , <u>Section</u> <u>ction 13.7.9</u> , <u>PortConnectionInfo Record</u> , <u>Section</u> <u>ction 13.7.11</u> , <u>IOCPMInfo</u> <u>7.12</u> , <u>CMEInfo Record</u> , <u>Section 13.7.13</u> , <u>C</u>	d, ChassisInfo fo Record, IOCP- nfo Record, Buddy- at of the appropriate 13.7.7, ChassisInfo Section 13.7.10, fo Record, DEM Record, dyInfo Record, and	3 4 5 6 7 8 9 10
13.7.3 DEVICE HEADER	Section 13.7	7.15. Asset lag Record respectively.		11 12 13
	The Device provides a v matches this device in a o beginning of follow the D	Header identifies the writable regions with ersion number indicating the format of the s specification as well as the device addres chain of xInfo devices. The Device Heade f all xInfo devices (VPD devices). xInfo Re evice Header.	nin a device. It also Device Header that ss for the next xInfo r is present at the ecords immediately	14 15 16 17 18 19
	xInfo Device of the xInfo	<u>e Header (Section Table 146 on page 603)</u> Device Header.	outlines the format	2(2
		Table 146 xInfo Device Heade	r	22 23
	Byte Offset	Field		24 25
	0	VPD_FormatVersion in BCD. [7:4] - MSN = major revision [3:0] - LSN = minor revision		26 21 21

Byte	Field	24
Offset		25
0	VPD_FormatVersion in BCD.	26
	[7:4] - MSN = major revision	27
	[3:0] - LSN = minor revision	28
	11h for this specification (format version 1.1)	29
1	[7:1] - ExtensionDeviceSlaveAddress	30
	0000_000 = no extension device.	31
	[0] - reserved (set to 0b)	32
2:5	byte 2: LSB of offset to first byte of write-protected area	33
	byte 3: MSB of offset to first byte of write-protected area	34
	byte 4: LSB of offset to last byte of write-protected area	35
	byte 5: MSB of offset to last byte of write-protected area	36
	FFFF_0000h if no write-protected area.	37
6	Header Checksum	38
		39

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13.7.3.1 VPD_FORMATVERSION			4
	The version informat where the most-signi least-significant nibb	ion is stored in BCD (binary coded ficant nibble holds the major version le holds the minor version number.	decimal) format, n number and the 4
13.7.3.2 EXTENSIONDEVICESLAV	EADDRESS		5
	ExtensionDeviceSlav is the next extension IB view, this address Management comma will either be a physi SEEPROM write-rea using a WriteVPD or the same access me cess the present dev	veAddress is the address of the dev to the device containing this device is the address that is used in a Read and to the MME. From the IB-ML vi cal IB-ML device address accessed d transaction or a logical IB-ML de ReadVPD command. Software sho thod for the Extension device that ice, and if that fails try the alternate	ice on IB-ML that header. From the dVPD Baseboard ew, this address d using an IB-ML vice accessed build first try to use was used to ac- e implementation.
13.7.3.3 OFFSETFORMAT			15
	OFFSETFORMAT define which are offsets to t	es the offset format to use in the su he first and the last bytes of a write	bsequent bytes 16 e-protected area. 17
	If both start and end write protected. The as the ending offset	offset are the same value, it indica value of FFFFh as the starting offs indicates that NO write-protected b	tes that 1 byte is et and the 0000h ytes are present.
13.7.4 Record Header			22
	The Record Header tional records that wi Header has the follo	contains offset information needed Il sequentially follow in a list manne wing format.	to find any addi- er. The Record 22 25
		Table 147 Record Header	26
	Field Size (in Bytes)	Field	28

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Record Type ID

See Table 151 Record Type IDs on page 609

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Field Size (in Bytes)	Field
1	Record Parameters
	[7] - LastRecord
	0b = more records follow
	1b = last record in this read-only or writable area. To
	find all Records, Software shall check both read-
	tifies the read-only and writable areas.) Other
	Records may exist in the extension device(s).
	[6] - Length Multiplier
	0b = record length given in bytes
	1b = record length given in multiples of 8 bytes. This does not imply that the record data starts on an 8-
	byte boundary. The record data always immedi- ately follows the record header.
	[5] - Read Only
	0b = The record contents are not Write Protected
	1b = S/W shall not attempt to write to any field in the
	record; it is recommended that the h/w device
	physically write-protect the record.
	[4] - reserved
	[3:0] - Record Format Version (=1n for this specification, unless otherwise specified.)
1	Record Length, bits 7:0 (zero based)

Table 147 Record Header

Any data associated with the Record will follow the last field of the header.

13.7.4.1 CHECKSUM

13.7.4.1.1 CHECKSUM CALCULATION

Record and field checksums are calculated as 256-([sum(bytes)+bytecount] mod 256). This is equivalent to taking an 8-bit sum of the bytes plus the bytecount and then performing an 8-bit 2's complement of the result.

Example:

Assume that we have three data bytes, AAh, 87h, and 32h. The bytecount 35 is then 3. The 8-bit sum of the bytes plus the bytecount is AAh+87h+32h+03h = 66h. 66h is 01100110b. The two's complement of 01100110b is equal to 10011001b+1b = 10011010b or 9Ah.

13.7.4.1.2 VERIFYING THE CHECKSUM

40 If the checksum is added to the preceding data bytes plus the bytecount, 41 the sum modulo 256 should be 00h. 42

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Example:

Assume that we have three data bytes, AAh, 87h, and 32h. Per the pre-3 ceding examples, the checksum is 9Ah. If we add AAh, 87h, 32h, 03h, and 9Ah we get 200h. 200h modulo 256 = 00h. 4

13.7.4.2 ENCODING/LENGTH BYTE

Records can be a combination of fixed-length and variable length fields. The Encoding/Length byte serves several purposes for variable length fields: It holds the length value for the field. It allows 'string' fields to be encoded in a way that is more efficient based on whether the string can be encoded as BCD (two characters per byte), ASCII (one character per byte), or UNICODE v3.0 (two bytes per character).

Architectural Note

The character encoding is done in a way that helps utility software present data, even if it doesn't know the semantics of the field. For example, it can display BCD, ASCII, or UNICODE strings without knowing their exact definition and can display binary encoded fields as 'hex'. Lastly, it provides a mechanism to tag OEM-defined fields.

The checksum is always the last byte in a Record. The Record Header specifies the length of the Record; therefore, the checksum is always at a known location regardless of the number of PADded bytes.

Table 148 presents the specification of the encoding/length byte.

Table 148 Encoding/Length Byte

bits	Sub-field	Description
[7:6]	EncodingType	Identifies the type of encoding used for the subsequent data bytes.
		00b - Binary or unspecified. Binary data bytes are stored least-significant
		62 bytes, maximum.
		01b - BCD plus (see below). BCD values are stored most-significant byte
		first. E.g. the BCD bytes for 1234h are stored as: byte $0 = 12h$, byte $1=34h$. This is done because it is expected that most BCD encoded
		fields will be treated as strings rather than converted to binary val-
		ues.
		10b - UNICODE v3.0 string, or OEM Field prefix.
		11b - 8-bit ASCII + Latin 1. "ASCII+LATIN1" is derived from the first 256 characters of Unicode 3.0. The first 256 codes of Unicode follow ISO
		646 (ASCII) and ISO 8859/1 (Latin 1). The Unicode "C0 Controls
		and Basic Latin" set defines the first 128 8-bit characters (00h-7Fh)
		128 (80h-FFh).

Table 148 Encoding/Length Byte

bits	Sub-field	Description
[5:0]	CharacterCount	Number of characters (number of bytes for a binary-encoded field). A character count of 00_0000b has special meaning in combination with the Encoding Type field. In addition, a count of 11_1111b is reserved when used with Encoding Type = 00b (binary). See <u>Table 149 Special Encoding/Length</u> Field Values

13.7.4.2.1 SPECIAL ENCODING/LENGTH FIELD VALUES

The values in Table 149 for an Encoding/Length field have special meanings.

value	name	meaning
00 h	reserved	Reserved. This value shall not be used where an Encoding/Length byte is expected.
3F h	reserved	Reserved. This value shall not be used where an Encoding/Length byte is expected.
40 h	Null Field	Empty (null) field. This value is used to identify a field that is present but unpopulated. This value must be used for null fields even when the normal encoding for this field wher populated is not ASCII.
80 h	OEM Prefix	80h = OEM Prefix field. The field indicates the start of a set of vendor-specific fields within a standard InfiniBand record. All following fields in the record, up to the next OEM Prefix field if any, are assumed to be specified by the vendor or organization identified by the OEM ID. The value FFh, FFh, FFh for a EUI-64 Company ID is reserved for Infini- Band specification defined records. OEM Fields are only allowed to follow the InfiniBand specification defined fields in a record.
C0 h	Last Field	Last variable length field in record. This value is used when a record has a variable num ber of Encoding/Length encoded fields and padding follows the last field. A record is allowed to end immediately with the checksum byte. I.e. a C0h does not need to follow the last field unless there are additional characters (PAD) between the last field and the checksum.

Table 149 Special Encoding/Length Field Values

13.7.4.2.2 OEM PREFIX FIELD

The OEM Prefix field is specified as follows. Note that the length of the field is implied by having an Encoding/Length value of 80h and is fixed at five bytes.

Table 150 OEM Prefix Field

field size (in bytes)	field
1	OEM Prefix Encoding/Length = 80h (OEM ID Field)
1	 [7:4] ID Type 1h = Company ID per EUI-64 / 48 (3 bytes) FFh, FFh, FFh = InfiniBand specified fields 2h = IANA Enterprise Number-based ID (3 bytes). FFh, FFh, FFh = reserved all others = reserved [3:0] ID Length - # of OEM ID data Bytes following
3	OEM ID data bytes least-significant byte first

13.7.4.3 USING OEM RECORDS AND DATA FIELDS

The VPD format supports both OEM-unique records, and OEM-unique data field extensions within InfiniBand specification defined 'standard' records. The following outlines the usage rules for OEM records and OEM fields within standard records.

- 1) OEM Records
 - With the exception of the ending checksum byte, the format of data fields within OEM-unique Records is not specified.
- 2) OEM Fields in Standard Records
 - One or more groups of OEM-unique data fields can be included in a standard record.
 - Each *group* of OEM-unique data fields for a given vendor or organization is required to be prefixed by a special 'OEM ID Field' that contains a 3-byte ID for the OEM.
 - Each individual field within the group is required to be formatted as a variable length field that starts with an Encoding /Length byte.
 - OEM-unique fields in a standard record can only follow the last standard field defined for the record. They are not allowed to be inserted between standard fields, even if the standard field starts with an Encoding/Length byte.

13.7.4.4 USE OF OPTIONAL FIELDS

Unless otherwise specified, Optional Fields must be present, but can be null or filled with the appropriate value indicating the field contents are 'unspecified'. Software identifies fields based on their order in the record.

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Since individual fields are not tagged according to type (to save space) all fields must be present to maintain ordering.

13.7.4.5 Use with Non-Module VPD Devices

All Record Types are allowed to be used on non-Module VPD devices, al-though some records only have meaning in the context of an InfiniBand Module. A non-Module device can optionally return records, such as ChassisInfo Records, at the ModuleInfo VPD device address. This implies that software should always check the ModuleInfo VPD device address first as the root device for VPD discovery. The ModuleInfo Record will in-dicate whether there is additional CME or ChassisInfo that can be obtained from other device addresses.

13.7.5 RECORD TYPES

Table 151 Record Type IDs on page 609 lists the different VPD record types and the associated Record Type ID values that are used in the Record Header.

Table 151 Record Type IDs			
Record Type	Record Type ID		
ModuleInfo	00h		
ChassisInfo	01h		
FRUInfo	02h		
ModulePowerInfo	03h		
PortConnectionInfo	04h		
CMEInfo	05h		
OEM	06h		
BuddyInfo	07h		
AssetTag	08h		
IOCPMINFO	09h		

13.7.6 MODULEINFO RECORD

The ModuleInfo Record is typically included on an InfiniBand Module to describe the Module class and the number of InfiniBand and IB-ML links

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exiting the Module. Non-Modules can also utilize this record to describe their link and IB-ML connection support.

field size (bytes)	field	Read/Write	PA_Module	NPA_Module	N_ModuleXCA	N_ModuleSw
8	ModuleGUID - EUI-64 ID assigned for this Module	RO	Req	Req	Req	Req
1	 [7:5] IBModuleType 000b = Module is not an InfiniBand Module 001b = Module is an InfiniBand Module All others = reserved [4:0] ModuleClass 0x00 - TCA 0x01 - HCA 0x02 - Switch 0x03 - Router 0x04 - 1x Repeater (port connection info record indicates whether repeater is Copper or Optical) 0x05 - 4x Repeater 0x06 - 12x Repeater All others - Reserved 	RO	Req	Req	Req	Req
1	NodeCount - Number of InfiniBand Nodes on this Module with unique NodeGUIDs. A value of FFh represents more than FEh.	RO	Req	Req ^a	Req ^a	Req ^a
1	PortCount - Number of InfiniBand port on this Module with unique Port- GUIDs (i.e. NodeGUID plus Port Number) A value of FFh represents more than FEh.	RO	Req	Req	Req ^a	Req ^a
1	 BackplaneLinkCount - Number of InfiniBand Links exiting this Module through its Backplane Connectors. Defines the number of Backplane Connection fields present in the associated PortConnectionInfo record. For modules that are not InfiniBand Modules, this count is the number of InfiniBand links that exit the module. 	RO	Req	Req	Req ^a	Req ^a
1	IBMLCount - Number of IB-ML interfaces on this Module	RO	Req	Req	Req ^a	Req ^a
1	BackplaneIBMLCount -Number of IB-MLs exiting this Module through its Backplane Connectors. For modules that are not InfiniBand Modules, this count is the number of IB-MLs that exit the module.	RO	Req	Req	Req ^a	Req ^a

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Table 152 ModuleInfo Record - Record Format Version=2 2 ModuleXCA ModuleSw NPA_Module field 3 Module Read/Write field size 4 (bytes) 5 Ł z z 6 1 or 6 or ModuleSize -Volumetric information for standard form factors in millime-RO Rea Rea Req Rea 7 8 ters. For InfiniBand Modules, the origin is defined as the 0,0,0 datum UA UA UA UA 8 used in the mechanical specifications for the Module. For non-standard 9 modules, this is the dimension of the overall envelope of the module. 10 Format (stored least significant byte first) Field size is 1-byte if 'null', 8-bytes if DimensionType = 1b, 6-bytes if 11 DimensionType=0b. 12 For DimensionType = 1b (standard from origin) 7-bytes: 13 Six 8-bit bitfields to describe 6 offsets from the origin: 14 [63:57] - Reserved. 15 56] - Extension (reserved. Write as 0b) ſ [55:48] - Right. Positive X direction from origin in right-hand coordi-16 nate system. 17 [47:40] - Left. Negative X direction from origin in right-hand coordi-18 nate system. 19 [39:32] - Up. Positive Y direction from origin in right-hand 20 [31:24] - Down. Negative Y direction from origin in right-hand coordinate system. 21 [23:16] - Front. Distance from origin to front (faceplate) of Module. 22 Positive Z direction from origin in right-hand coordinate sys-23 tem. [15:08] - Rear. Distance from origin to rear or backplane connection 24 of Module. Negative Z direction from origin. 25 For DimensionType = 0b (envelope) 26 [47:44] - Reserved. 27 [43:32] - Module Width in mm 12-bits. 28 [31:20] - Module Height in mm 12-bits. 29 [19:08] - Module Depth in mm 12-bits. For DimensionTypes 0b and 1b 30 [07:02] - Reserved 31 [1] - DimensionType 32 1b = offsets specified relative to standardized Module origin. 33 0b = size of envelope specified. 34 0] - FieldPopulated ſ 35 1b = bits [63:0] are populated. 0b = field is unspecified: only bits [7:0] are present. (bits 7:1 36 should be 000_000b) 37

field size bytes)	field	Read/Write	PA_Module	NPA_Module	N_ModuleXCA	N_ModuleSw
1	 FormFactor 00h = unspecified 01h = non-removable (integrated, embedded, or non- user -service-able) 02h = Standard IB Module 03h = Standard Wide IB Module 04h = Tall IB Module 05h = Tall Wide IB Module 13h = PCI 14h = low-profile PCI 15h = Compact PCI 16h = VME 17h = Internal Mezzanine Board 18h = Card Edge Board 19h = Device Bay 1Ah = Other Removable All others reserved 	RO	Req_ UNA	Req_ UNA	Req_ UA	Req_ UA
var	OEM fields . A group of one or more OEM fields must be preceded with an OEM Prefix field.	-	Opt	Opt	Opt	Opt
1	C0h (Encoding/Length byte encoded to indicate no more info fields). [Only required when space exists between the end of the last field and the Checksum]	-	Opt	Opt	Opt	Opt
var	PAD [0 to N bytes]. An implementation is allowed to pad records with FFh values.	-	Opt	Opt	Opt	Opt
1	Checksum	-	Req	Req	Req	Req

a. Zero is a valid number for this count.

13.7.7 CHASSISINFO RECORD

This record returns information about an InfiniBand Chassis and slotspecific information for Chassis VPD accessed from an InfiniBand Mod-

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ule or a CME.

field size bytes)	field	Read/Write	Requiremen
8	ChassisGUID - EUI-64 ID that identifies this Chassis.	RO	Req
1	SlotCount - Total number of IB Module slots available in this Chassis. (1-based)	RO	Req
/ar	SlotNumbers - HighestSlotNumber ^a / 3 (rounded up) 8-bit bitfields indicating which slot numbers are valid for the Chassis. This field allows slot numbers to be non-sequential. Slot numbers must be in the range 1-254. 0 is assigned to the CME and the Chassis containing the CME.	RO	Req
	1b = There is at least one other SlotNumbers field byte following this one.		
	0b = This is the last byte of the SlotNumbers field in this record.		
	[6]-reserved		
	[5:0] - Each bit-pair represents one of three corresponding slot numbers, with bits[1:0] of the first SlotNumbers field corresponding to slot number 1.		
	00b = Chassis does not implement this slot number		
	01b = Chassis provides one Backplane Connector to this Standard Slot		
	10b = Chassis provides one Backplane Connector to this Tall Slot		
	11b = Chassis provides two Backplane Connectors to this Tall Slot		
var	CMEAccess - HighestSlotNumber ^a / 7 (rounded up) contiguous, 8-bit, bitfields indicating which InfiniBand Module slots in this Chassis provide CME Access via their Primary Port (1). If this record is for the CME itself (Slot number = 0) then this indicates the number of IB-MLs connected to the CME.	RO	Req
	[7] - extension.		
	1b = There is at least one other CMEAccess field byte following this one.		
	0b = This is the last byte of the CMEAccess field in this record.		
	[6:0] - Each bit represents one of seven corresponding slot numbers, with bit 1 of the first CMEAccess field corresponding to the first implemented slot as defined in <u>Section 9.1.3.1, "Slot Designations," on page 360</u> . (bit 0 of the first CMEAc- cess field indicates whether a CME is present at all. 0b = no CME, 1b = CME exists.)		
	0b = slot does not provide CME access.		
	1b = slot provides CME access.		
otInfo			
1	SlotNumber- Chassis-assigned slot number for the slot through which this Chassis-	RO	Req
	Info device is being accessed by the Module. 1-based.		UNA
	Slot numbers must be in the range 1-254. 0 is assigned to the CME and the Chassis containing the CME. FFh means 'unspecified' and is used to support non-Module applications of this record.		

Table 153 ChassisInfo Record - Record Format Version=2

Table 153 ChassisInfo Record - Record Format Version=2

eld ize ⁄tes)	field	Read/Write	Requiremen
1	 SlotDetails - One byte field giving details on the slot through which this ChassisInfo device is being accessed [7:6] CMEAccess 00b = unspecified (used to support non-Module applications of this record) 01b = A CME is accessible via the Primary Port (1) for this slot. If this info is for a non-Module, this bit indicates that a CME is accessible by BM MADs to the port used to access this VPD Device. 10b = A CME is not accessible from this slot / port. 11b = reserved [5] ProxyAccess 0b = There is no CME proxy access to other slots via the slot or port used to access this VPD Device. 1b = This slot or port provides access to a CME that provides proxy access to other slots. [4] reserved. [3:2] LockDrivesCTR - Indicates whether the lock (if present) keeps CME_CTR deasserted (0) until the lock is released. 00b = unspecified (used to support non-Module applications of this record) 01b = CME_CTR will not be asserted unless lock is released, but CME has other criteria that can also cause CME_CTR to be kept deasserted. 11b = reserved [1:0] MechanicalLockPresent - Indicates whether there is a mechanical lock associated with this slot. A mechanical lock physically prevents removal of the Module is for the slot. The implementation of the lock can be a purely mechanical (e.g. a mechanical key lock) or electro-mechanical (e.g. a solenoid). 00b = unspecified (used to support non-Module applications of this record) 01b = CME_CTR will not be asserted unless lock is released, but CME has other criteria that can also cause CME_CTR to be kept deasserted. 11b = reserved 	RO	Req_ UNA
	NodeCount - Number of InfiniBand Nodes on this Chassis with unique Node- GUIDs. A value of FFh represents more than FEh.	RO	Req_ UNA
	OEM fields . A group of one or more OEM fields must be preceded with an OEM Pre- fix field.	-	Opt
	C0h (Encoding/Length byte encoded to indicate no more info fields). [Only required when space exists between the end of the last field and the Checksum]	-	Opt
ır	PAD [0 to N bytes]. An implementation is allowed to pad records with FFh values.	-	Opt
1	Checksum	-	Req

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13.7.8 FRUINFO RECORD

FRU stands for "Field Replaceable Unit". The FRUInfo Record provides information that can potentially help a user identify and inventory the field replaceable units that make up a given Module, system, or sub-system. The record can be used for many types of InfiniBand specification defined and non-InfiniBand specification defined FRUs.

C13-66: All InfiniBand Modules shall implement a FRUInfo Record in an xInfo device. They shall also follow the FRUInfo Record, the Device Header, and the Record Header specifications.

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o13-23: All entities that implement a FRUInfo Record shall follow the FRUInfo Record, the Device Header, and the Record Header specifications.

Implementation Note

There can be more than one FRUInfo Record within a VPD device. A typical example of this is a low-cost system design where a single VPD device is used to hold both FRUInfo for the chassis as a replaceable unit, and FRUInfo for the overall product. Similarly, a system where there is a single VPD device on the main system board could hold three FRUInfo Records. One for the system as an overall product, one for the main system board itself as a replaceable unit, and one for the Chassis as a replaceable unit.

Table 154 FRUInfo Record

field size (bytes)	field	Read/Write	PA_Module	NPA_Module	N_ModuleXCA	N_ModuleSw	15 16 17 18 19
1	FRUType	RO	Req_	Req_	Req_	Req_	- 20
	00h = unspecified		UNA	UNA	UA	UA	21
	01h = InfiniBand Module						22
	02h = InfiniBand Module Backplane						23
	03h = InfiniBand Switch module ^a						24
	04h = Main Chassis. This is FRUInfo for the Chassis itself as a replaceable unit.						25
	05h = Platform/System Product. This identifies a separate FRU						26
	record used to hold information about the overall platform (sys-						27
	a Main Chassis FRU record.						28
	06h = Product. This identifies a FRU that is a standalone product, but						29
	does not fit the definition of an InfiniBand Platform or other pre- defined FRU types.						30 31
	07h = Board or Card. This FRU holds info about a board or card that						32
	08b = Power Converter / Supply modulea						33
	00h = 0 ther module ^a (assembly)						34
	0Ah = Cooling modulea (assembly) (e.g. FAN)						35
	0Bh = Sub-Chassis						36
	0Ch = Processor module ^a (or field replaceable chip)						27
	0Dh = Memory module ^a						37
	0Eh = Memory Card						36
	0Fh-DFh = reserved for future InfiniBand specifications						39
	E0h-FFh = OEM specified per manufacturer / company identified by						40
	ManufacturerID field, below.						41
	1	1	1	1	I	I	42

Table 154 FRUInfo Record

field size (bytes)	field	Read/Write	PA_Module	NPA_Module	N_ModuleXCA	N_ModuleSw
1	FRU_Handle The FRU_Handle identifies Records that are associated with the same FRU. The scope of the value for the FRU_Handle is the xInfo device and its extension devices. Different FRUs shall be represented by different FRU_Handles.	RO	Req	Req	Req	Req
1	 FRUGUID All FRUGUID data bytes are encoded as binary, least-significant byte first, unless otherwise specified. 00h = none specified (0 data bytes follow) 01h = EUI-64 (8 data bytes follow) 02h = EUI-48 (6 data bytes follow) 03h = SMBIOS/IPMI/OSF/ Wired for Management/Microsoft GUID/UUID (16 data bytes follow) 04h = SMBus 2.0 UDID (8 bytes) All others reserved 	RO	Req ^b	Req ^b	Opt	Opt
var	FRUGUID data bytes.	RO	Req ^b	Req ^b	Opt	Opt
1	SerialNumber Encoding/Length ^c (Table 148: Encoding/Length Byte)	RO	Req	Req	Req	Req
var	SerialNumber data bytes The FRU manufacturer assigns the FRU serial number.	RO	Req	Req	Opt	Opt
1	PartNumber Encoding/Length (Table 148: Encoding/Length Byte)	RO	Req	Req	Opt	Opt
var	PartNumber data bytes The FRU manufacturer assigns the FRU part number.	RO	Req	Req	Opt	Opt
1	Model Encoding/Length (Table 148: Encoding/Length Byte)	RO	Req	Req	Opt	Opt
var	Model data bytes The FRU manufacturer assigns the FRU model name.	RO	Req	Req	Opt	Opt
1	Version Encoding/Length (Table 148: Encoding/Length Byte)	RO	Req	Req	Opt	Opt
var	Version data bytes The FRU manufacturer assigns the FRU version number.	RO	Req	Req	Opt	Opt
1	ManufacturerName Encoding/Length (<u>Table 148: Encoding/Length</u> Byte)	RO	Req	Req	Opt	Opt
var	ManufacturerName	RO	Req	Req	Opt	Opt
1	ProductName Encoding/Length (use null if FRU is not sold or intended to be viewed as a separate product.) (<u>Table 148: Encoding/Length Byte</u>)	RO	Req	Req	Opt	Opt

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Table	154	FRUInfo	Record
10010			110001 4

field size (bytes)	field	Read/Write	PA_Module	NPA_Module	N_ModuleXCA	N_ModuleSw
1	ManufacturerID All following ManufacturerID data bytes are encoded as binary, least significant byte first, unless otherwise specified. 00h = none specified (0 data bytes follow) 01h = Company ID per EUI-64 / 48 (3 bytes) 02h = IANA Enterprise Number-based ID (3 bytes)	RO	Req_ UA	Req_ UA	Req_ UA	Req_ UA
var	ManufacturerID data bytes	RO	Opt	Opt	Opt	Opt
1 or 4	 Mfg. Date / Time Number of minutes from 0:00 hrs, GMT 1/1/2000. (0:00 hrs is midnight 12/31/1999). Field size = four bytes if populated, one byte if null. (The definitions of month and year in this field are based on ISO 8601 specification.) A value of 0000_0000h indicates un-specified. Format (stored least significant byte first): [31:22] - Year Given as number of years from GMT 1/1/2000. 1-based. 0 corresponds to the year 2000. (1023 years) [21:18] - Month 1-based. 1 = January. [17:13] - Day of the month. 1-based. [12:08] - Hours Number of hours from 0:00 hrs on day of manufacture 1-based. ('24 hr' format). 0 means time is between 0:00 hours and 1:00 hours. [07] - DateTimeDataPresent 0b = bits 8:31 not present. This field is null. Bits 7:1 are reserved and should be 0000000b. 1b = bits 8:31 present. Bits 31:1 hold time value. [06] -reserved. [05:00] - Minutes from 0:00 hrs on day of manufacture. 1-based. 0 means time is exactly on the hour. 	RO	Req_ UA	Req_ UA	Req_ UA	Req_ UA
1	C0h (Encoding/Length byte encoded to indicate no more info fields). [Only required when space exists between the end of the last field and the Checksum]	RO	Opt	Opt	Opt	Opt
var	PAD [0 to N bytes]. An implementation is allowed to pad records with FFh values.	RO	Opt	Opt	Opt	Opt
1	Checksum	RO	Req	Req	Req	Req

a. The lower case "m" in module means that the module (assembly) is not an IB-Module.

b. ModuleGUID is required in ModuleInfo Record. FRUGUID data bytes are not required unless the FRUGUID does not follow EUI-36 64. If not populated, set FRUGUID to 00 (none specified). 37

c. These areas are always encoded as ASCII to facilitate serial number comparison and tracking by management software applications.

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13.7.9 PORTCONNECTIONINFO RECORD

The PortConnectionInfo variable-length record provides information about the entity to which the port connects A BuddyInfo record must be present in the device, including any extensions, to provide the Node-GUIDHandles necessary for this record.

Table 155 PortConnectionInfo Record - Record Format Version=2

fi s (bː	ield size ytes)	field	Read/Write	PA_Module	NPA_Module	N_ModuleXCA	N_ModuleSw
	1	ConnectionInfoCount - Number of NodeGUIDHandle/PortNo/ConnectionType/BackplaneConnection field sets following. 1-based. It is recommended, but not required, that one NodeGUID/PORTNO/ConnectionType field sets be provided for each link present on the Module. A value of FFh represents more than FEh.	RO	Req	Req	Req	Req
unt x	1	NodeGUIDHandle - Handle of NodeGUID to which the related fields apply.	RO	Req	Req	Req	Req
ConnectionInfoCo	2	PortNo - Port Number The value that this port will return in PortInfo:LocalPortNumber (see <i>InfiniBand Architecture Specification, Volume 1</i> , Chapter "Subnet Man- agement", Section "Subnet Management Class")	RO	Req	Req	Req	Req

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field size (byte	s)	field	Read/Write	PA_Module	NPA_Module	N_ModuleXCA	N_ModuleSw
ConnectionInfoCount × (structure continuation)	I ConnectionTy [7:6] - Intern 00b = un 01b = Cc 10b = Cc 000b = u 001b = Ir 010b = Ir 000b = u 000b = u 000b = u 010b = N Bann 010b = N 111b = Tr fully others = Examples: 01_011_111 10_011_010 10_011_011	pe alConnection ^a specified. Innection terminates at another Node without going ugh a cable or a connector. Innection terminates at another Node after going through ble or a connector. Internal connection Class Inspecified finiBand specified Copper Cable finiBand specified Fiber-optic Cable CB Repeater on the FRU, then Copper Cable ^b Repeater on the FRU, then Fiber-optic Cable Repeater on the FRU, then Fiber-optic Cable Repeater on the FRU, then A Node Iserved ExtionClass Inspecified Ion-specified Removable [Connection is via a non-Infini- d specified connector type] thassis side of a Backplane Slot Connector Iodule side of a Backplane Slot Connector Iodule side of a Backplane Slot Connector Ion-removable [Port is 'hard wired' to the Module] ne information is not found in this field; other fields are descriptive. reserved Non-specified Removable (proprietary connector for internal use) Non-specified Removable (proprietary connector for use outside of the enclosure housing the FRU) Backplane Slot Connector (Chassis HCA connected to a Slot) Module Slot Connector (Module TCA connected to its Backplane Connector	RO	Req_UNA	Req_UNA	Z Req_ UA	z Req_ UA
	10_001_111 10_010_111	Copper Cable (e.g. Switch connected to a Copper Cable) Fiber Cable (e.g. HCA connected to a Fiber Cable)					
	10_101_111	Fiber Cable (e.g. HCA, connected to a Fiber Cable via a Repeater)					

Table 155 PortConnectionInfo Record - Record Format Version=2

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field size (bytes)	field	Read/Write	PA_Module	NPA_Module	N_ModuleXCA	N_ModuleSw
ConnectionInfoCount x (structure continuation)	BackplaneConnection - Indicates mapping to backplane designations based on value of ConnectionType:ConnectionClass If ConnectionType:ConnectionClass = 010b (Chassis side), the field encodes the designation defined in Section 9.1.3.1, "Slot Designations," on page 360 [7] - Reserved [6] - Connector Location ^c Ob = Primary 1b = Optional [5:3] - Reserved [2:0] - Physical Port Number within the connector (as defined in Section 10.3.3 on page 419) Oh = Reserved 1h = Port 1 2h = Port 2 3h = Port 3 All others reserved If Connector Location ^c Ob = Primary 1b = Optional [5:3] - Reserved [6] - ConnectorOclass = 011b (Module side), the field encodes the designation defined in Section 9.1.3.2, "Module Port Designations," on page 361 [7] - Reserved [6] - Connector Location ^c Ob = Primary 1b = Optional [5:4] - Connector Slot Number ^c within the slots the module occupies Oh = Reserved [3] - Reserved [4] - Port 1 2h = 2 - Adjacent 3h = Reserved [3] - Reserved 1h = Port 1 2h = Port 2 3h = Port 3 All others reserved If a Port 3 All others reserved If Port 1 2h = Port 3 All others reserved If Port 2 3h = Port 3 All others reserved If Port 2 3h = Port 3 All others reserved If ConnectionType:ConnectionClass = any others, field contents are undefined	RO	Req	Req	Req	Req

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24 25

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field size bytes)	field	Read/Write	PA_Module	NPA_Module	N_ModuleXCA	N_ModuleSw
var	Additional NodeGUIDHandle/PortNo/ConnectionType/BackplaneCon- nection field sets, if any.	RO	Req ^d	Opt	Opt	Req ^d
var	OEM fields. A group of one or more OEM fields must be preceded with an OEM Prefix field.	-	Opt	Opt	Opt	Opt
1	C0h (Encoding/Length byte encoded to indicate no more info fields). [Only required when space exists between the end of the last field and the Checksum]	-	Opt	Opt	Opt	Opt
var	PAD [0 to N bytes]. An implementation is allowed to pad records with FFh values.	-	Opt	Opt	Opt	Opt
1	Checksum	-	Req	Req	Req	Req

c. See Section 3.2, "Physical Port," on page 58.

d. There shall be a PORTNO/Connection Type field pair for each IB connection.

13.7.10 MODULEPOWERINFO RECORD

The ModulePowerInfo record returns information about the power consumption, startup characteristics, and power management capabilities for a Module.

Table 156 ModulePowerInfo Record

field size (bytes)	field	Read/Write	PA_Module	NPA_Module	N_ModuleXCA	N_ModuleSw	27 28 29 30 31
3	OperationalThermalPower Maximum amount of power dissipated under normal operation including any vendor supplied exerciser over any sliding 60 second window. 0 = unspecified. [23:17] - Reserved [16: 0] - Power in mW. Range: 1 - 131071 mW	RO	Req_ UNA	Req_ UNA	Req_ UA	Req_ UA	32 33 34 35
2	OperationalCurrent Maximum amount of current drawn under normal operation including any vendor supplied exerciser across the range of VBulk. 0 = unspecified. [15:14] - Reserved [13: 0] - Current in mA. Range: 1-16383 mA	RO	Req_ UNA	Req_ UNA	Req_ UA	Req_ UA	36 37 38 39 40

field size bytes)	field	Read/Write	PA_Module	NPA_Module	N_ModuleXCA	N_ModuleSw
2	IdleCurrent Amount of current that a fully initialized device draws when waiting for functional requests. 0 = unspecified. [15:14] - Reserved [13: 0] - Current in mA. Range: 1-16383	RO	Req_ UNA	Req_ UNA	Req_ UA	Req_ UA
2	InitCurrent Amount of current drawn during Modules Built-In Self Test or self-initialization execution across the range of VBulk. 0 = unspeci- fied. [15:14] - Reserved [13: 0] - Current in mA. Range: 1-16383	RO	Req_ UNA	Req_ UNA	Req_ UA	Req_ UA
2	InitTime The amount of time (in 10's of ms) from the end of Module Reset to when the Module is available for initialization by the Subnet Manager using SMPs and by other software. The InitTime includes any implemented BIST functionality. 0=unspecified.	RO	Req_ UNA	Req_ UNA	Req_ UA	Req_ UA
1	ModulePMCapability. [7:2] - Reserved [1] IsMStandbySupported 0 =: No 1 =: Yes [0] - IsPowerManagementSupported 0 = No 1 =: Yes	RO	Req	Req	Req	Req
1	UnitPMCapability A multi-unit Module shares the same UnitPMInfo for all of its units [7:2] - Reserved [1] IsUSleepSupported 0 =: No 1 =: Yes [0] - IsUStandbySupported 0 = No 1 =: Yes	RO	Req	Req	Req	Req

Table 156 ModulePowerInfo Record

	Table 156 ModulePowerInfo Rec	ord					1
field size (bytes)	field	Read/Write	PA_Module	NPA_Module	N_ModuleXCA	N_ModuleSw	- 2 3 4 5 6
1	ModulePowerParms [7:6] = reserved [5:4] PowerClass 00b = unspecified 01b = Power Class I 10b = Power Class II 11b = reserved [3:2] = reserved [1:0] = RedundantPower Module incorporates redundant power converters. 00b = unspecified 01b = No redundancy 10b = Redundancy 11b = reserved	RO	Req_ UNA	Req_ UNA	Req_ UA	Req_ UA	77 8 9 1 1 1 1 1 1 1 1 1 1
var	OEM fields . A group of one or more OEM fields must be preceded with an OEM Prefix field.	-	Opt	Opt	Opt	Opt	
1	C0h (Encoding/Length byte encoded to indicate no more info fields). [Only required when space exists between the end of the last field and the Checksum]	-	Opt	Opt	Opt	Opt	
var	PAD [0 to N bytes]. An implementation is allowed to pad records with FFh values.	-	Opt	Opt	Opt	Opt	
1	Checksum	-	Req	Req	Req	Req	2

13.7.11 IOCPMINFO RECORD

The IOCPMINFo record indicates the power management capabilities of the IOCs associated with an IOUnit. If a Module contains multiple IOUnits

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and several IOCs, the information about all such IOCs appear sequentially in the IOCPMInfo record.

eld ze field tes)	Read/Write	PA_Module	N_ModuleXC	N_ModuleSw
IOC_Count The number of nine-byte IOC capabilities (IOCPMCapability field through IStandbyCurrent) defined in this record.	RO	Req ^a	Req ^a	Req ^a
1 IOCPMCapability IOC Power Management Capability Mask [7] IsIDozeSupported 0: No 1: Yes [6] IsINapSupported 0: No 1: Yes [5] IsISIeepSupported 0: No 1: Yes [5] IsISIeepSupported 0: No 1: Yes [4] IsIStandbySupported 0: No 1: Yes [3] WREisIDozeSupported 0: No 1: Yes - WRE can be generated by this node while in Ipoze State [2] WREisINapSupported 0: No 1: Yes - WRE can be generated by this node while in Ipoze State [1] WREisISleepSupported 0: No 1: Yes - WRE can be generated by this node while in Ippep State [0] WREisIStandbySupported 0: No 1: Yes - WRE can be generated by this node while in Ippep State [0] WREisIStandbySupported 0: No 1: Yes - WRE can be generated by this node while in Ippep State [0] WREisIStandbySupported 0: No 1: Yes - WRE can be generated by this node while in Ippep State [0] WREi	RO	Req	Req	Req
 IDozeCurrent The amount of total current drawn from the Bulk Power while in I_{Doze} PM state. Range: 0 - 16384 mA (0 - 16.384 A) [15:14] - Reserved [13: 0] - Current in mA 	RO	Req	Req	Req

Table 157 IOCPMInfo Record

Table 157 IOCPMInfo Record							
field size (bytes)	field	Read/Write	PA_Module	N_ModuleXCA	N_ModuleSw		
2	 INapCurrent The amount of total current drawn from Bulk Power while in I_{Nap} PM state. Range: 0 - 16384 mA (0 - 16.384 A) [15:14] - Reserved [13: 0] - Current in mA 	RO	Req	Req	Req		
2	 ISleepCurrent The amount of total current drawn from Bulk Power while in I_{Sleep} PM state. Range: 0 - 16384 mA (0 - 16.384 A) [15:14] - Reserved [13: 0] - Current in mA 	RO	Req	Req	Req		
2	IStandbyCurrent The amount of total current drawn from Auxiliary Power while in I _{Standby} PM state. Bulk Power drawn is defined to be 0A. Range: 0 - 16384 mA (0 - 16.384 A) [15:14] - Reserved [13: 0] - Current in mA	RO	Req	Req	Req		
var	Additional nine-byte IOC capabilities (IOCPMCapability through IStandbyCurrent) field sets as indicated by IOC_Count.	-	Opt	Opt	Opt		
var	OEM fields . A group of one or more OEM fields must be preceded with an OEM Prefix field.	-	Opt	Opt	Opt		
1	C0h (Encoding/Length byte encoded to indicate no more info fields). [Only required when space exists between the end of the last field and the Checksum]	-	Opt	Opt	Opt		
var	PAD [0 to N bytes]. An implementation is allowed to pad records with FFh values.	-	Opt	Opt	Opt		
1	Checksum	-	Req	Req	Req		

a. There **shall** be one IOC capabilities for each IOC if one or more IOC's IsPowerManaged.

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13.7.12 CMEINFO RECORD

The CMEInfo record contains additional information about the CME.

Table 158 CMEInfo Record

field size bytes)	field	Read/Write	Requirement
1	CMEGUID All CMEGUID data bytes are encoded as binary, least-signif- icant byte first, unless otherwise specified. 00h = none specified (0 data bytes follow) 01h = EUI-64 (8 data bytes follow) 02h = EUI-48 (6 data bytes follow) 03h = SMBIOS/IPMI/OSF/ Wired for Management/Microsoft GUID/UUID (16 data bytes follow) 04h = SMBus 2.0 UDID (8 bytes)	RO	Req_ UA
var	CMEGUID data bytes. Field not present if CMEGUID field is set to 'none'.	RO	Opt
2	CME Firmware Revision in BCD Least Significant Number first. Format is xx.yy where the first byte holds BCD digits for the minor revision and the second byte holds two BCD digits for the major revision. 0000h = unspecified.	RO	Req_ UA
var	 SlotNumbers - One or more 8-bit bitfields indicating for which slots (identified by slot numbers) the CME provides IB-ML access. The field allows slot numbers to be non-sequential. Slot numbers must be in the range 1-254. 0 is assigned to the CME and its containing Chassis via CME. [7] - extension. 1b = There is at least one other SlotNumbers field byte following this one. 0b = This is the last byte of the SlotNumbers field in this record. [6:0] - Each bit represents one of seven corresponding slot numbers, with bit 1 of the first SlotNumbers field corresponding to slot number 1, and bit 0 of the second SlotNumbers field is reserved.) 	RO	Req_ UA
var	OEM fields. A group of one or more OEM fields must be preceded with an OEM Prefix field.	-	Opt
1	C0h (Encoding/Length byte encoded to indicate no more info fields). [Only required when space exists between the end of the last field and the Checksum]	-	Opt
var	PAD [0 to N bytes]. An implementation is allowed to pad records with FFh values.	-	Opt
1	Checksum	-	Reg

13.7.13 OEM RECORD

The OEM record contains OEM-specified data. The format of the data in the OEM Data portion of the field.

Table 159 OEM Record							
field size (bytes)	field	Read/Write	Requirement				
1	 [7:4] OEM ID Type 1h = Company ID per EUI-64 / 48 (3 bytes) FFh, FFh, FFh = Infini-Band specified fields 2h = IANA Enterprise Number-based ID (3 bytes). FFh, FFh, FFh = reserved all others = reserved [3:0] ID Length - # of OEM ID data Bytes following 	RO	Req				
var	OEM ID data bytes	RO	Req				
var	OEM Data Format per OEM identified by OEM ID Type and OEM ID data fields.	-	Opt				
1	Checksum	-	Req				

There are non-volatile writable regions in xInfo devices into which the CME, the Module, or the Baseboard Manager may write. The written data in specified writable areas **shall** follow the OEM Record format.

13.7.14 BUDDYINFO RECORD

The BuddyInfo record contains NodeGUIDs of InfiniBand Nodes and other entities that belong to the same enclosure.

There **shall** not be any connector or cable between any Node or other entity whose NodeGUID or GUID appear in a BuddyInfo Record. There **shall not** be any connector or cable between the Nodes or entities whose NodeGUID or GUID appear in a BuddyInfo Record and the Node reporting the BuddyInfo Record.

f s (b	ield size ytes)	field					
	1	BuddyCount	R/W	Req			
		 [7:2] The number of InfiniBand nodes that belong to the same enclosure as the node reporting this record. 00000b = 'none' (No other node belongs to the same enclosure as 					
		this node.)					
		11111b = More than 31d					
		 [1:0] GUID encoding: All BuddyNodeGUID data bytes are encoded as binary, least-significant byte first, unless otherwise specified. 00b = EUI-64 (8 data bytes per GUID follow) 04b = EUI-64 (0. data bytes per GUID follow) 					
		01b = EUI-48 (6 data bytes per GUID follow)					
		GUID/UUID (16 data bytes per GUID follow)					
		11b = SMBus 2.0 UDID (8 bytes per GUID follow)					
BuddyCount \times	var	BuddyGUID - data bytes for all the entities counted by BuddyCount. Field not present if BuddyCount field is set to 'none'. If GUID represents an IBA node, the value is the EUI-64 ID assigned for the node as reported in NodeInfo:NodeGUID to which the port is associated. (see <i>InfiniBand Archi-</i> <i>tecture Specification, Volume 1</i> , Chapter "Subnet Management", Section "Subnet Management Class")	RO	Req			
	1	NodeGUIDHandle - Unique value associated with the above NodeGUID. Serves as an index into PortConnectionInfo records.	RO	Req			
	var	OEM fields. A group of one or more OEM fields must be preceded with an OEM Prefix field.	R/W	Opt			
	1	C0h (Encoding/Length byte encoded to indicate no more info fields). [Only required when space exists between the end of the last field and the Check-sum]	R/W	Opt			
	var	PAD [0 to N bytes]. An implementation is allowed to pad records with FFh values.	R/W	Opt			
	1	Checksum	R/W	Req			

Table 160 BuddyInfo Record - Record Format Version=2

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13.7.15 AssetTag Record

As <u>Table 161</u> shows, the AssetTag record is a writable Record which contains an AssetTag field.

Table 161 AssetTag Record

field size (bytes)	field	Read/Write	Requirement
1	FRU_Handle The FRU_Handle identifies Records that are associated with the same FRU. The scope of the value for the FRU_Handle is the xInfo device and its extension devices.	R/W	Req
1	AssetTag Encoding/Length (Table 148: Encoding/Length Byte)	R/W	Req
var	AssetTag data bytes	R/W	Req
var	OEM fields. A group of one or more OEM fields must be preceded with an OEM Prefix field.	R/W	Opt
1	C0h (Encoding/Length byte encoded to indicate no more info fields). [Only required when space exists between the end of the last field and the Checksum]	R/W	Opt
var	PAD [0 to N bytes]. An implementation is allowed to pad records with FFh values.	R/W	Opt
1	Checksum	R/W	Req

CHAPTER 14: OS POWER MANAGEMENT

14.1 INTRODUCTION

"**Power Management**" is the set of state definitions and facilities that allow for an Operating System (or a prescribed agent) to control the power consumption of InfiniBand adapter module and, to a limited degree, switches.

Power Management of devices or media not directly attached to the Infini-Band fabric as an addressable node are outside the scope of this specification. (aka Fibre Channel or SCSI disks, Ethernet, etc).

14.2 OVERVIEW

14.2.1 POWER MANAGEMENT STATES

Power management policies rely on the existence of states which define the possible levels of power consumption. For InfiniBand, there are four (4) types of states defined:

Port Power State (X) Applies to a given link in the fabric
Module Power State (M) Applies to a module which may contain one or more I/O units
Unit Power State (U) Applies to the I/O unit at the end of a link, typically an xCA
IOC Power State (I) Applies to the I/O Controller(s) (IOC) on an I/O Unit

Some of the individual states within the above types are termed "meta" states because they are only discernible by implication. That is, they are derived states based on the independent states that make them up. There are no specific architectural facilities defining such states.

14.2.1.1 META STATES

Figure 176 shows the applicability of these states to a generic InfiniBand module.



* Refer to <u>Chapter 13: Hardware Management</u> on IB-ML, IB-ML Agents and implications of multiple IB-ML interfaces

Figure 176 I/O Node Power Management Structure

Typically, operating system level software, based on policies it or the system owner establishes, controls the state entry and exit of a given unit.

In this chapter, the software component responsible for power management policy is referred to as the "Power Manager". Through its policies, this software may place none, some or all of the units that it owns into varying degrees of power management states such to achieve the savings desired. It is outside the scope of the InfiniBand specification to define these policies; rather, InfiniBand defines mechanisms through which implemented policies may be realized. These policies may be based on system load, timed operations, or external events.

The majority of the facilities that control the Power Management states are architected as part of the Baseboard Management class; thus, the Power Manager must have software relationship with the Baseboard Manager for the fabric to be able to access these facilities. This relationship is not specified. However, possible implementations include, but are not limited to:

- having the Power Manager be a component of the Baseboard Manager,
- having the Power Manager be separate and utilize the Baseboard Manager as a proxy to the control facilities,

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	baying the Power Manager directly c	ontrolling the states through

 having the Power Manager directly controlling the states through a sharing of B-Keys.

Additionally, the Power Manager would need a relationship with the Subnet Manager if it implements policies that utilize the X States.

Some of the states defined allow for the continued functionality of the InfiniBand links such that the Power Manager can, through the use of defined Baseboard management datagrams (MAD), restore a unit to an operational state. However, to achieve the highest degrees of power savings, states are defined that allow node implementations to remove bulk power from the unit and yet allow for it to be powered back on from the InfiniBand fabric. Additionally, means are defined to allow for an Infini-Band unit to indicate that it, having been previously configured to do so, desires to have the system be restored to the operating condition as defined by the policy. These are known as "Wake Request Events".

14.2.2 WAKE REQUEST EVENTS

Wake Request Events (WREs) are those events that can be produced by an InfiniBand module that desires to return a "sleeping" or "low power" system to an operational state given the system had been previously enabled to do so. The actions that need to take place when a device recognizes a WRE are:

- Provide an indication to the chassis power subsystem to affect a "power on" as needed
- 2) Provide an indication to the "Power Manager" that the WRE has occurred such that this agent can perform the remaining wake-up actions as set by system policy.

14.2.3 SIMPLE SYSTEM TOPOLOGY

Figure 177 depicts a basic two power domain topology for Power Management.



In the more generic case, one or more switch elements can be inserted between the I/O Unit and the Host whereby Power Management operations (state changes and wake-up "events") must be routable between these.

14.2.4 LOW POWER STATE ENTRY

Through the Baseboard class and the **[Set/Get]ModulePMControl**, **[Set/Get]UnitPMControl** and **[Set/Get]IOCPMControl** attributes, the Power Manager software can control the transition to a low powered state. See <u>Section 13.6.2</u>, "Baseboard MAD Commands (BM MAD Attributes)," on page 570.

Hardware will, upon link training failure, enter either the X_{Polling} or X_{Sleep} state based on link port attribute modifiers. See <u>Section 5.6, "Link Initial-</u><u>ization and Training," on page 118</u> for details.

14.2.5 LOW POWER STATE EXIT

A node may exit from a low power state due to one of two mechanisms:

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	• An event generated by the node. These are ter quests (WRE).	med Wake Event Re-
	 Activity on the InfiniBand link indicating wake-u WakeonIB. 	p. This is termed $\begin{bmatrix} 2\\ 3 \end{bmatrix}$
	Further, the waking due to the InfiniBand fabric may source actions:	r be due to one of two $\frac{1}{5}$
	• Power management or other software targeted node using already powered portions of the fab	at specific link or 7 ric. 8
	The cascading of a WakeonIB conditions through a low powered fabric	gh the use of Beacon 9 10
14.2.5.1 WAKE REQUEST EVENT		11
	IOCs may detect or otherwise generate Wake Req enabled. The module enables its power converter a IMxPReq_L signal on the backplane connector. Th serted may cause the system power supply to trans if the system power is enabled to do so. If the syste the ON state, this assertion is ignored.	uest Events (WRE), if and asserts the is signal being as- sition from OFF to ON m power is already in 17
	The enablement of module power, either due to the power or both, will cause the module to enter the L whereby a training sequence (otherwise known as quence") is periodically transmitted on the InfiniBan ment of a trained link, further state transitions are u	e converter or system ink Polling state the "Beacon se- d link. Upon establish- inder software control. 23
	On the companion end ("Host Entity" in this topology beacon sequence on the IB link will generate a logi This signal, powered from V_{Aux} , is used to transition system power supply for that domain to ON (M_{On} or <u>WakeOnIB</u> logical signal is typically ignored if the point of the state.	/), the presence of the cal WakeOnIB signal.24 25 26 26 26 27 27 28 29
	The software interface defined below to transition to may also be used to transition from a low powered	o a low powered state state if it is accessible.
14.2.5.2 WAKE ON FABRIC		33
	For the case that the Wake Event Request was get node or that software on a powered node desires to the fabric to return to operational conditions, the W nism is used.	nerated on an HCA o cause other parts of ake on Fabric mecha-
	A Wake on Fabric operation is a two step process.	38
	 The Power Manager interfaces with the Subnet link taken from Link Sleeping (X_{Sleep}) to Link U 	Manager to have a p (X_{On}) state such to

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	reestablish the link to a low power endnode.	The process of bringing

reestablish the link to a low power endnode. The process of bringing the link to the Link Up state involves the use of the Beacon Sequence and will effectively produce a <u>WakeOnIB</u> logical signal that will restore power (M_{On}) to the node if enabled to do so.

 The Power Manager then controls the Unit and IOC states using [Get/Set]UnitPMControl and [Get/Set]IOCPMControl attributes, respectively.

14.2.6 POWER SUBSYSTEM NOTIFICATION OF WRE

Systems using InfiniBand may be built in one of two basic structures:

- **Single Domain** where all nodes capable of generating a wake request event are in the same power domain as the node or nodes that will execute the policy based actions.
- **Multiple Domain** where any nodes capable of generating a wake request event is in a different power domain as the node or nodes that will execute the policy based actions.

Each of these domains can be viewed as a "Local Domain" relative to the InfiniBand devices that reside in them. In the case of the "Single Domain" structure, the "Local Domain" is synonymous with "Single Domain".

14.2.6.1 SINGLE DOMAIN / LOCAL DOMAIN

The Single Domain structure represents the single board system topology typical in many low-end systems (desktops, workstations, single box servers). In this case, the notification mechanism available from the WRE detecting adapter board can be used to wake-up the power subsystem of the entire domain.





The "wake-on" indication that spans power domains is produced on the InfiniBand link in the form of Training Sequence 1 as described in Chapter 5: Link/Phy Interface on page 79. For the purposes of Power Management, this is also referred to as the "Beacon Sequence".

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	There are three possibilities for the state of a given domain receiving an incoming beacon sequence or dressed:	local domain (i.e. that on a port) that are ad-
	1) Bulk Power On, Auxiliary Power On	4
	Training Sequence 1 received on a port that is simply begins the normal training process witho action with the power subsystem.	not in Disabled state 5 but any additional inter- 7
	2) Bulk Power Off, Auxiliary Power On	8
	The detection of Training Sequence 1 must pro the local power subsystem similar to that as de <u>Section 14.2.6.1, "Single Domain / Local Domain</u> power is restored, further receipt of Training Se normal link training process to bring a link activ	9boduce an indication toescribed inin," on page 636.0nce11equence 1 begins the12/e.
	Note: this version of the specification does not restoring a switch from auxiliary power while re	define the means for14etaining its context.15
	3) Bulk Power Off, Auxiliary Power Off	16
	As no power is available, the Training Sequence and is ignored.	e 1 can not be detected
	Given power is restored to the domain, further ope Band defined sequences or packets.	erations flow as Infini-
14.2.7 Contexts		22
	"Context" is information or states that pertain to a gi functions can resume operation. This section desc that are pertinent to Power Management.	ven aspect from which ribes those contexts
14.2.7.1 FUNCTION CONTEXT		27
	The Function Context is that information specific to vice function that indicates the device's operational tion Context is that state after the hardware device driver has initialized but operations have not comm	o the implemented de- l state. Initialized Func- and any associated nenced.
14.2.7.2 FABRIC CONTEXT		33
	The Fabric Context is that information which allow erations to be received and transmitted on the Infin cludes, but is not limited to, the following:	s for management op- niBand fabric. This in-
	 M_Keys and associated control bits 	37
	 P_Keys and associated control bits 	39
	B_Keys and associated control bitsQP0 context	40 41 42

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	QP1 Baseboard Class	
14.2.7.3 WRE CONTEXT		
	The WRE Context is the state information that a tection, generation, and reporting of Wake Requ	llows for the enabling, de- uest Events.
	Specifically, this includes Attribute IOCPMContr abled and WREStatus .	r ol , Components WREEn-
14.2.7.4 Switch Context		
	The Switch Context is that information that allow Beacon Sequence event.	ws for the distribution of a
	If the switch has bulk power remaining to it, no ment context is required. If a Beacon Sequence the port successfully trains, the Subnet Manager of the port upon its next fabric sweep. Optionally a <i>SubnTrap(NewNodeonFabric)</i> to the Subnet Manager should subscribe for these events for X _{Sleep} state for as part of its policy.	explicit power manage- is received on a port and r will find the state change /, the switch may produce the Manager. The Power nodes that it uses the
	Auxiliary powered switches are not architected i ification.	in this version of the spec-
14.2.8 Power Manager Not	IFICATION	
	System power management policy and system point of the WRE notification into the "in-band" p is basically enabling a given set of end nodes to enabling a potentially different set of end nodes to Given system policy and implemented features, action with one or more power systems (due to which the intervening switches reside) along the end node and the "notification" end node(s).	design affect the "entry" portion of the system. This wait on a WRE while also to get notified of the WRE. this may involve the inter- the power domains in a path from the "detecting"
	Ultimately, this notification needs to get to a Ch power reenablement, allows the Power Manage a WRE has occurred such that it can then perfor restoration.	annel Adapter that, upon er to gain knowledge that orm policy based function
	The mechanism for passing this notification from to the "notification" end node involves the follow	n the "detecting" end node ving operational steps:
	1) An Auxiliary Powered I/O Unit generates a	WRE.
	 The local power domain is brought up using scribed in <u>Section 14.2.6.1, "Single Domain</u> <u>page 636</u>. 	the mechanism de- / Local Domain," on

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	3) T c	he I/O Unit sends Training Sequence 1 as a Beac ompanion, presumably a Switch or HCA.	con Sequence to its
	4) T	he Switch or HCA is either on Bulk Power or Aux	xiliary Power. 2
	lf	the Switch or HCA is on Bulk Power, then:	4
	•	The "waking link" is trained;	5
	•	If a Switch, the training of a previous Sleeping the Switch create SubnTrap(NewNodeonFak the Subnet Manager.	or Polling link has 6 pric) message to 8
	•	If an HCA, it provides implementation specific ested entities in that node	notification to inter- 9
	lf	the Switch or HCA is on Auxiliary Power, then	1
	•	The HCA power subsystem is enabled as des <u>Section 14.2.6.2, "Multiple Domains," on page</u>	cribed in 12 637.
	•	A Switch on Auxiliary Power is not defined in t specification.	his version of the
14 3 PORT POWER MANAGEME	INT ST	ATES	1
	The I opera to fac tiona	Port Power Management States are meta ⁵ states ational states of the link with the power available. cilitate a bridge between power management tern I link states.	that combine the They are defined ninology and opera- 2 2
	Table section	<u>162</u> summarize these states; they are defined from the states is the states in the states is the	ully in the following 23
			2:
			25
			2
			20
			2
			3
			3
			3
			3
			3
			3
			3
			3/
			3
			4
	5. Me	eta is defined in <u>Section 14.2.1.1, "Meta States," on pa</u>	<u>age 631</u> . 4 4'

Table 162	Port Power	Management States
		manayement States

x	Port	Power		Power	Port	Near End	
State	Recv Xmit		Link States ^a	Consumption	Implementation	Recovery Latency	
X _{On}	Bulk	Bulk	LinkUp, Configuration, Recovery	Full	Required ^b	None	
X _{Polling}	Bulk	Bulk	Polling	Low	Required ^b	1 ms	
X _{Sleep}	Bulk	Bulk	Sleeping	Low	Required ^b	1 ms	
X _{Disabled}	Bulk	Bulk	Disabled	Low	Required ^b	N/A	
X _{Standby}	Aux	Off	Beacon Enabled ^c	Lowest (while restor- able)	Optional ^d	100 ms	
X _{Off}	Off	Off	N/A	None	Given	Indefinite	

a. The states shown are defined in <u>Section 5.6.4</u>, "Link Training State Machine," on page 123 except as noted.
b. The requirement for this state is defined in <u>Section 5.6</u>, "Link Initialization and Training," on page 118 and repeated here for a complete description of these meta states.

c. This link state is not defined in <u>Section 5.6.4</u>. Rather, this is the enablement of the Beacon Detection circuitry which may or may not be present in the same device that implements the other Link States.

d. Based on whether *M*_{Standby} is supported (as indicated by *IsMStandbySupported* in *ModulePowerInfo* record.

14.3.1 X_{ON} LINK POWER STATE

This state indicates that the InfiniBand link is fully powered. Any link state, as reported by **Subn.PortInfo(LinkState)**, other than Port Polling, Port Sleep, and Port Disabled defines the port as being in **X**_{On}.

14.3.2 X_{POLLING} LINK POWER STATE

This state is defined as having the port receiver look for the beaconing sequence from the companion end while periodically sending a beacon sequence on the port transmitter. The companion end may or may not be present.

Architecture Note

This state is considered a low power state for an uncontested port but was not designed for power management policy of a connected link. This is due to the fact that if the companion end is in a low power state (X_{Sleep} or $X_{Standby}$), the receipt of a beacon sequence during the poll will cause a transition to X_{On} . Thus, power management policy software would be advised to use X_{Sleep} for placing a powered port which is connected to a companion into a low power state.

14.3.3 X_{SLEEP} LINK POWER STATE

This state is defined as having the port receiver look for the beaconing sequence from the companion end while leaving the port transmitter static. The companion end may or may not be present.

Architecture Note

This state is useful when waiting for a hot add event or when one or both ends is in a power saving mode. Either end can initiate a wake-up event by sending the Beacon Sequence. In the case of an endnode, this would happen due to a WRE or initial power-up of the endnode. In the case of a switch, this could also be due to Power Management software desiring to reenable the link.

14.3.4 X_{STANDBY} LINK POWER STATE

This state is defined as having the port receiver look for the beaconing sequence while operating on auxiliary power. The companion end may or may not be present.

14.3.5 X_{OFF} LINK POWER STATE

This state is defined as having neither Bulk nor Auxiliary Power available to the port and the port will not respond to the beaconing sequence.

14.4 MODULE POWER STATES

Module Power States control the local power converter enablement for InfiniBand defined pluggable modules. Other nodes on the fabric that are not packaged on these form factors may or may not utilize these states. <u>Table 163</u> provides a summary of the Module Power states that are fully defined in the following sections.

Table 163 Module Power States				
Module Power State	Bulk Power Converter	Auxiliary Power	Wake Request Event (if supported)	Requirement
M _{On}	Enabled	Enabled	No effect	Required
M _{Standby}	Disabled	Enabled	Enabled	Optional
M _{NoWake}	Disabled	Enabled	Disabled	Meta
M _{Off}	Disabled	Disabled	Disabled	Meta

o14-1: All modules that implement Power Management as indicated by *ModulePowerInfo.ModulePMCapability(IsPowerManagementSupported)*=1 **shall** provide the "M" states indicated as "Required" in the column labeled "Requirement" in <u>Table 163</u> and provide access and control of these states through the *[Get/Set]ModulePMControl* Attributes defined in <u>Section 13.6.2</u>, "Baseboard MAD Commands (BM MAD Attributes)," on page 570.

14.4.1 M_{ON}

14.4.2 M_{STANDBY}

The M_{On} state indicates that the power converters on the module that are required for operation are enabled.

 $M_{Standby}$ indicates that the power converter(s) on the module are disabled but can be reenabled without Backplane intervention. Auxiliary power is available.

o14-2: All modules that implement the $M_{Standby}$ state as indicated by *ModulePowerInfo.ModulePMCapability(IsMStandbySupported)*=1 **shall** provide the ability to detect a Beacon Sequence on the InfiniBand link. A delay of 10ms +100/-0% **shall** be provided between the entry into $M_{Standby}$ and the enablement of the Beacon Detect circuitry to allow for the link quiescent condition to be achieved.

14.4.3 M_{NOWAKE}

The **M**_{NoWake} state indicates that power converter(s) on the module are disabled by the backplane through **VBxEn_L** and can only be enabled by the backplane using **VBxEn_L**. Auxiliary power is available. Entry into and exit out of this state is exclusively under control of the backplane.

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14.4.4 M_{OFF}

The **M**_{Off} state is a mechanical off state whereby either the module is not inserted in a slot or that the chassis in which the module is plugged has no auxiliary power available. In this state, the module does not receive Bulk power

14.4.5 MODULE POWER STATE TRANSITIONS

Figure 180 shows the valid transitions for the Module Power States.



Figure 180 Module Power State Diagram

14.5 I/O UNIT POWER STATES

I/O Unit States are defined for endnodes that have a TCA and one or more IOCs having one or more power management functions implemented.

<u>Table 164</u> provides a summary of the I/O Unit Power states that are defined fully in the following sections.

Table 164 I/O Unit Power States

Unit Power State	Module State	Wake Request (if supported)	Requirement
U _{On}	M _{On}	Don't Care	Required
U _{Sleep}	M _{On}	Don't Care	Optional
U _{Standby}	M _{Standby}	Enabled	Meta
U _{Off}	M _{Off}	Disabled	Meta

o14-3: All modules that implement Power Management as indicated by *ModulePowerInfo.ModulePMCapability(IsPowerManagementSupported)*=1 **shall** provide the "U" states indicated as "Required" in the column labeled "Requirement" in <u>Table 164</u> and provide access and control of these states through the *[Get/Set]UnitPMControl* Attributes defined in <u>Section 13.6.2, "Baseboard MAD Commands (BM MAD Attributes)," on page 570</u>.

The U_{On} state indicates that the I/O Unit is generally enabled for operations. Specific power management policy is further influenced through affecting the "*I*" states of underlying IOCs.

14.5.2 U_{SLEEP}

14.5.1 U_{ON}

o14-4: All modules that implement the **U**_{Sleep} state as indicated by *ModulePowerInfo.UnitPMCapability(IsUSleepSupported)*=1 **shall** provide the functionality described in <u>Section 14.5.2</u>.

The U_{Sleep} state indicates that the I/O Unit is functionally disabled, but the TCA is capable of responding to the following if its Port is in X_{on} :

- 3737All QP0 operations38QP1 operations:39• BMSend.GetUnitPMControl40• BMSend.SetUnitPMControl41
- InfiniBandSM Trade Association

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	BMSend.GetModulePMControl	
	BMSend.SetModulePMControl	
	From the IB S/W point of view, the underlying IOC this state and may be in I_{Off} state .	Cs are not accessible in
	If a port is not in X_{on} , although not accessible, the I/O Unit may be in any state.	e underlying IOCs and
14.5.3 USTANDOV		
STANDBY	The U_{Standby} state is a meta state indicating that t I/O Unit resides is in M_{Standby}	he module on which this
	From the software point of view, the underlying IO this state and may be in <i>I_{Off}</i> state.	Cs are not accessible in
14.5.4 Uorr		
UTP OFF	The U_{Off} state is a mechanical state of having bo power being unavailable. If the module on which t M_{Off} , the unit is considered to be in this state.	th bulk and auxiliary his I/O Unit resides is in
14.5.5 I/O UNIT POWER STATE	TRANSITIONS	
	Figure 181 shows the valid transitions for the I/O	Unit Power States.


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<u>Table 165</u> provides a summary of the IOC Power states that are defined fully in the following sections.

Table 165 IOC Power States							
IOC State	Operations to Unit	Operations from Unit	Context	Power	Latency to I _{Operational}	Requirement	
I_{Operational}	All	All	Function	Full	None	Required	
I _{Uninit}	Driver Specified	Driver Specified	None	Full	Drv Spec'd	Required	
I _{Doze}	QP0, QP1 Base- board Class	WRE Trap	Function, WRE ^a	Low	us	Optional	
I _{Nap}	QP0, QP1 Base- board Class	WRE Trap	Function, WRE ^a	Lower	ms	Optional	
I _{Sleep}	QP, QP1 Base- board Class	WRE Trap	WRE ^a	Lower	S	Optional	
I _{Standby}	Beacon Sequence	None	WRE ^a	<1.2W		Optional	
I _{Off}	None	None	None	None	N/A	Meta	

a. WRE Context is only maintained for those IOCs that support Wake Request Event generation.

o14-5: All modules that implement Power Management as indicated by
ModulePowerInfo.ModulePMCapability(IsPowerManagementSup-
ported)=1 shall provide the "I" states indicated as "Required" in the
column labeled "Requirement" in Table 165 and provide access and con-
trol of these states through the [Get/Set]IOCPMControl Attributes de-
fined in Section 13.6.2, "Baseboard MAD Commands (BM MAD
Attributes)," on page 570.21212222232424252627

14.6.1 IOPERATIONAL		28
	The I_{Operational} state indicates that the IOC is fully operational.	29 30
14.6.2 ILININIT		31
China	The <i>I_{Uninit}</i> state is transitional and is not visible to Power Management	32 33
	software. It indicates that the IOC is capable of running at rated speed al-	34
	a driver.	35 36
14.6.3 IDoze		37
BOZE	A44 C . All modules that implement the L state as indicated by (OOD	38
	014-6: All modules that implement the I _{Doze} state as indicated by <i>IUCP</i> -	39
	MInto.IUCPMCapability(IsIDozeSupported)=1 for an IUC shall provide	40
	Mate Inclinality described in <u>Section 14.0.3</u> and provide the IOCP-	41
		42

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	I_{Doze} is a light sleep state where some functional activity on the board (such as media network monitoring for sp other activity is typically suppressed. This state require tain implementation specific context to fully recover to dition upon the detection of a "Wake-on" event.	y may be occurring becial packets) but es the IOC to main- its <i>I_{Operational}</i> con-	1 2 3 4 5
	In the <i>I_{Doze}</i> state, the IOC shall only initiate link operat Request Event has occurred whereby a <i>BMTrap.WRL</i> Baseboard Manager.	ions when a Wake ∃ is sent to the	6 7 8
14.6.4 I _{NAP}			9
	o14-7: All modules that implement the I _{Nap} state as in <i>MInfo.IOCPMCapability(IsINapSupported)</i> =1 for an IOC functionality described in <u>Section 14.6.4</u> and provide the <i>apCurrent</i> field for that IOC.	dicated by <i>IOCP-</i> C shall provide the he <i>IOCPMInfo.IN-</i>	10 11 12 13 14
	<i>I_{Nap}</i> is a long sleep state where an endnode is not intersome amount of time as set by system policy. This stat to maintain implementation specific context to fully rectional condition upon the detection of a "Wake-on" even	ided to be used for e requires the IOC over to its <i>I_{Opera-}</i> nt.	15 16 17 18 19
	In the I_{Nap}state , the IOC shall only initiate link operation Request Event (WRE) has occurred whereby a <i>BMTra</i> the Baseboard Manager.	ons when a Wake ap.WRE is sent to	20 21 22
14.6.5 I _{SLEEP}			23
	o14-8: All modules that implement the I _{Sleep} state as in <i>MInfo.IOCPMCapability(IsISleepSupported)</i> =1 for an I the functionality described in <u>Section 14.6.3</u> and provid <i>MInfo.ISleepCurrent</i> field for that IOC.	ndicated by <i>IOCP</i> - OC shall provide de the <i>IOCP-</i>	24 25 26 27 28
	<i>I</i> _{Sleep} is a long sleep state where an endnode is not infor some amount of time as set by system policy. This IOC to only maintain WRE context to fully recover to its tion upon the detection of a "Wake-on" event.	tended to be used state requires the s <i>I_{Operational}</i> condi-	29 30 31 32
	In the I_{Sleep}state, the IOC shall only initiate link operat Request Event has occurred whereby a BMTrap.WRL Baseboard Manager.	ions when a Wake ∃ is sent to the	34 35 36
14.6.6 I _{Standby}	o14-9: All modules that implement the I _{Standby} state a <i>CPMInfo.IOCPMCapability(IsIStandbySupported)</i> =1 for ment shall provide the functionality described in <u>Section</u> provide the <i>IOCPMInfo.IStandbyCurrent</i> field for that I	s indicated by <i>IO</i> - or an IOC Manage- <u>on 14.6.3</u> and OC.	37 38 39 40 41 42

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	Is a truly dormant state whereby only au	xiliary power is provided
	to the IOC. No function context is maintained in	this state. If Wake Re-
	quest Events are supported from Istandby the as	ssociated WRE context
	shall be maintained. Full initialization by softwar	e will need to take place
	when exiting this state (to <i>Uninit</i>).	
14671		
I T.O.7 IOFF	L is the logical state of either mechanical off (th	a IOC having no bulk or
	1 Off is the logical state of either mechanical off (if	te IOC naving no bulk of
	auxiliary power available). No context is retained	

14.6.8 IOC POWER STATE TRANSITIONS



14.7.1 IOPERATIONAL

Table 166 I _{Operational} Power State Combinations							
Module State	Unit State	Xcvr State	IOC State	Operations to IOC	Operations from IOC	Context	Power
M _{On}	U _{On}	X _{On}	I _{Operational}	All	All	Function, Fabric	Full
<	All others	>	I _{Operational}		Invalid		

14.7.2 I_{Doze}

Table 167 I_{Doze} Power State Combinations

Module State	Unit State	Xcvr State	IOC State	Operations to IOC	Operations from IOC	Context	Power
M _{On}	U _{On}	X _{On}	I _{Doze}	BMSend ^a , DevMgtAc- tion(IOCreset)	WRE ^b	Function, Fabric WRE ^b	<full< td=""></full<>
<	All others	>	I _{Doze}		Invalid		
a. Required t	o exit this st	ate.					

b. If supported in IDoze mode

14.7.3 INAP

Table 168 I_{Nap} Power State Combinations

Module State	Unit State	Xcvr State	IOC State	Operations to IOC	Operations from IOC	Context	Power
M _{On}	U _{On}	X _{On}	I _{Nap}	BMSend ^a , DevMgtAc- tion(IOCreset)	WRE ^b	Function, Fabric, WRE ^b	<full< td=""></full<>
M _{On}	U _{On}	X _{On}	I _{Nap}	TS1 ^c	WRE ^b	Function, WRE ^b	<full< td=""></full<>
<	All others	>	I _{Nap}		Invalid		

a. Required to exit this state.

b. If supported in $\mathbf{I_{Nap}}$ mode c. Required to exit $\mathbf{X_{Sleep}}$ state

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war State Combinations

14.7.4 I_{SLEEP}

Table 103 ISleep I ower State Combinations								
Unit State	Xcvr State	IOC State	Operations to IOC	Operations from IOC	Context	Power		
U _{On}	X _{On}	I _{Sleep}	BMSend ^a , DevMgtAc- tion(IOCreset)	WRE ^b	Function, Fabric, WRE ^b	Full		
U _{On}	X _{On}	I _{Sleep}	TS1 ^c	WRE ^b	Function, WRE ^b	<full< td=""></full<>		
U _{Sleep}	X _{Sleep}	I _{Sleep}	TS1 ^c	WRE ^b	WRE ^b	<full< td=""></full<>		
All others	>	I _{Sleep}		Invalid				
	Unit State U _{On} U _{On} U _{Sleep}	Unit Xcvr State State U _{On} X _{On} U _{On} X _{On} U _{Sleep} X _{Sleep} All others>	Unit Xcvr IOC State State State UOn Xon ISleep UOn Xon ISleep UOn Xon ISleep USleep Xsleep ISleep USleep Xsleep Isleep	Unit State Xcvr State IOC State Operations to IOC Uon Uon Xon ISleep ISleep BMSend ^a , DevMgtAc- tion(IOCreset) Uon Xon ISleep ISleep TS1 ^c Usleep Xsleep ISleep TS1 ^c Isleep TS1 ^c	Unit StateXcvr StateIOC StateOperations to IOCOperations to from IOCUOn UOn XonISleepBMSend ^a , DevMgtAc- tion(IOCreset)WRE ^b Uon UOn UOn XonISleepTS1 ^c WRE ^b UsleepXsleepISleepTS1 ^c WRE ^b	Unit StateXcvr StateIOC StateOperations to IOCOperations to from IOCOperations Context U_{On} U_{On} X_{On} I_{Sleep} BMSend ^a , DevMgtAc- tion(IOCreset)WRE ^b Function, Fabric, WRE ^b U_{On} U_{On} X_{On} I_{Sleep} TS1 ^c WRE ^b Function, Fabric, WRE ^b U_{On} U_{Sleep} X_{Sleep} I_{Sleep} TS1 ^c WRE ^b Function, WRE ^b U_{Sleep} X_{Sleep} I_{Sleep} TS1 ^c WRE ^b WRE ^b U_{Sleep} X_{Sleep} I_{Sleep} TS1 ^c WRE ^b WRE ^b		

a. Required to exit this state.

b. If supported in \mathbf{I}_{Sleep} mode

c. Required to exit X_{Sleep} state

14.7.5 I_{Standby}

Table 170 I_{Standby} Power State Combinations

Module State	Unit State	Xcvr State	IOC State	Operations to IOC	Operations from IOC	Context	Power
M _{Standby}	U _{Standby}	X _{Standby}	I _{Standby}	TS1 ^a	IMxPReq_L	WRE ^b	<1.2W
<	All others	>	I _{Standby}		Invalid		

a. Required to exit this state from the fabric. A local Wake Event can also cause an exit if supported.

b. If WRE is supported in this mode

14.8 SWITCH POWER MANAGEMENT

The architecture provides for the ability to put individual ports into a low power state to allow system policy to reduce power dissipation if desired.

If the port is in a low power mode (X_{Sleep}) , two ways are provided to exit this mode and have the port return to an active state:

- 1) under management software control
- 2) due to a hot plug or WRE event

Auxiliary powered switches are not architected in this version of the specification. InfiniBandTM Architecture Release 1.2 VOLUME 2 - PHYSICAL SPECIFICATIONS

OS Power Management

14.8.1 HOT PLUG EVENTS

For the case of hot plug events, upon the completion of a module poweron, a Training Sequence 1 is sent from the plugged module to the companion port. This will initiate the full training sequence described in <u>Section 5.6, "Link Initialization and Training," on page 118</u>.

14.8.2 WRE EVENTS

For WRE events, there are two cases: 1) the WRE endnode is local (in the same power domain as this switch) and 2) the WRE endnode is remote (in some other domain from the switch).

For the local domain case, the architecture only specifies the case where the switch has had bulk power maintained to it. Thus, the WRE event on the detecting endnode looks like a hot plug event (See Section 14.8.1).For the remote domain case, there are 2 possibilities: 1) the switch is currently powered and 2) the switch's power domain is currently not powered, other than auxiliary power, and needs to be enabled. For the case of the switch is powered and the port is in an X_{Sleep} state, the WRE is seen as a Beacon Sequence and looks like a hot plug event.

As previously stated, the case where the switch is on auxiliary power is not architected in this version of the specification.

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CHAPTER 15: VOLUME 2 COMPLIANCE SUMMARY

15.1 COMPLIANCE DEFINITION

This chapter specifies the Compliance Categories which are approved for labeling various products which contain InfiniBand content. This will allow vendors to label their products and claim InfiniBand compliance without creating confusion in the marketplace. This chapter addresses compliance to the feature set defined by Volume 2 of the InfiniBand Specification. Additional cross-references to the Compliance Summary for Volume 1 of the InfiniBand Specification will be added when necessary.

15.1.1 PRODUCT APPLICATION

Each product, which has InfiniBand content, **may** claim InfiniBand Compliance at one or more of the categories defined in the Compliance Summaries of the InfiniBand Specification. A product **shall not** simply claim "InfiniBand Compliant". Each claim of compliance **shall** be composed of two parts as follows:

Volume 2 Compliance Category: Volume 1 Compliance Category

The Volume 1 Compliance categories are defined in *InfiniBand Architecture Specification, Volume 1*, <u>Chapt 20: Volume 1 Compliance Summary</u>.

The valid Volume 2 Compliance categories are defined in <u>Section 15.2</u>

15.2 VALID VOLUME 2 COMPLIANCE CATEGORIES

Volume 2 Compliance Categories refer to the functionality of a physical entity which has one or more InfiniBand elements described in Volume 2. <u>Table 171</u> summarizes all valid Volume 2 compliance categories.

Detailed compliance requirements are listed for each category in <u>Section 15.3, "Compliance Requirements," on page 662</u>.

Category	Product Type	Qualifier	Product Definition	Reference ^a	
CU	С	U (Unmanaged)	Unmanaged IB Chassis	Section 15.3.1 on page 662	_
CA	(Chassis)	A (Actively Managed)	Actively Managed Chassis	Section 15.3.2 on page 663	_
CP		P (Passively Managed	Passively Managed Chassis	Section 15.3.3 on page 665	-

Table 171 Valid Volume 2 Compliance Categories

Category	Product Type	Qualifier	Product Definition	Reference ^a
PS	Р	S (Standard)	Standard IB Protocol Aware Module	Section 15.3.4 on page 667
PW	(Protocol aware	W (standard Wide)	Wide IB Protocol Aware Module	Section 15.3.5 on page 671
PT	module)	T (Tall)	Tall IB Protocol Aware Module	Section 15.3.6 on page 675
PTW		TW (Tall-Wide)	Tall-Wide Protocol Aware Module	Section 15.3.7 on page 679
RS	R	S (Standard)	Standard IB Repeater Module	Section 15.3.8 on page 683
RW	(Repeater module)	W (standard, Wide)	Wide IB Repeater Module	Section 15.3.9 on page 686
RT		T (Tall)	Tall IB Repeater Module	Section 15.3.10 on page 689
RTW		TW (Tall, Wide)	Tall Wide Repeater Module	Section 15.3.11 on page 692
CC01	CC	01 (1x cable)	1x Copper cable	Section 15.3.12 on page 695
CC04	(Copper Cable)	04 (4x cable)	4x Copper cable	Section 15.3.13 on page 696
CC08	,	08 (8x cable)	8x Copper cable	Section 15.3.14 on page 698
CC12		12 (12x cable)	12x Copper cable	Section 15.3.15 on page 699
CC12-4x		12x to 3-4x (cable)	12x to 3-4x Copper cable	Section 15.3.16 on page 700
CS01		01 (1x cable)	1x SFP Copper cable	Section 15.3.17 on page 701
FS01	FS	01 (1x cable)	1x SX Fiber optic cable	Section 15.3.18 on page 702
FS04	(Fiber, Short	04 (4x cable)	4x SX Fiber optic cable	Section 15.3.23 on page 704
FS08	haul)	08 (8x cable)	8x SX Fiber optic cable	Section 15.3.20 on page 703
FS12		12 (12x cable)	12x SX Fiber optic cable	Section 15.3.21 on page 703
FL01	FL	01 (1x cable)	1x LX Fiber optic cable	Section 15.3.22 on page 703
FL04	(Fiber, Long haul)	04 (4x cable)	4x LX Fiber optic cable	Section 15.3.23 on page 704
FL08	o ,	08 (8x cable)	8x LX Fiber optic cable	See note <u>a.</u>
FL12		12 (12x cable)	12x LX Fiber optic cable	See note <u>a.</u>
PC01	PC	01 (1x cable port)	1x Copper cable port	Section 15.3.24 on page 704
PC04	(Port, Copper	04 (4x cable port)	4x Copper cable port	Section 15.3.25 on page 705
PC08	cable)	08 (8x cable port)	8x Copper cable port	See note <u>a.</u>
PC12		12 (12x cable port)	12x Copper cable port	Section 15.3.27 on page 709
PS01	PS	01 (1x cable port)	1x SX Fiber optic cable port	Section 15.3.28 on page 711
PS04	(Port, Short haul	04 (4x cable port)	4x SX Fiber optic cable port	Section 15.3.29 on page 711
PS12	fiber)	12 (12x cable port)	12x SX Fiber optic cable port	Section 15.3.30 on page 712

Table 171 Valid Volume 2 Compliance Categories

Category	Product Type	Qualifier	Product Definition	Reference ^a
PL01	PL	01 (1x cable port)	1x LX Fiber optic cable port	Section 15.3.31 on page 712
PL04	(Port, Long haul	04 (4x cable port)	4x LX Fiber optic cable port	Section 15.3.32 on page 713
PL12	fiber)	12 (12x cable port)	12x LX Fiber optic cable port	See note <u>a.</u>
PP01	PP	01 (1x)	1x Pluggable Port	Section 15.3.33 on page 714
PP04	(Port, Plugga-	04 (4x)	4x Pluggable Port: - R1.2	Section 15.3.34 on page 714
PP08	ble)	08 (8x)	8x Pluggable Port	See note <u>a.</u>
PP12		12 (12x)	12x Pluggable port	See note <u>a.</u>
AP04	AP	04 (4x)	4x Active Cable Port	Section 15.3.35 on page 714
AP12	(Active Port)	12 (12x)	12x Active Cable Port	Section 15.3.36 on page 715
AC04	AC	04 (4x)	4x Active Cable	Section 15.3.37 on page 715
AC12	(Active Cable)	12 (12x)	12x Active Cable	Section 15.3.38 on page 716
DC01	DC	01 (1x)	1x Pluggable copper cable device	Section 15.3.39 on page 716
DC04	(Device Copper,	04 (4x)	4x Pluggable copper cable device - R1.2	Section 15.3.40 on page 717
DC08	Plugga- ble)	08 (8x)	8x Pluggable copper cable device	See note <u>a.</u>
DC12	,	12 (12x)	12x Pluggable copper cable device	See note <u>a.</u>
DS01	DS	01 (1x)	1x Pluggable SX fiber optic device	Section 15.3.41 on page 718
DS04	(Device Short haul	04 (4x)	4x Pluggable SX fiber optic device	Section 15.3.42 on page 719
DS08	Fiber, Plugga-	08 (8x)	8x Pluggable SX fiber optic device	See note <u>a.</u>
DS12	ble)	12 (12x)	12x Pluggable SX fiber optic device	See note <u>a.</u>
DL01	DL	01 (1x)	1x Pluggable LX fiber optic device	Section 15.3.43 on page 721
DL04	(Device Longhaul	04 (4x)	4x Pluggable LX fiber optic device	See note <u>a.</u>
DL12	Fiber, Plugga- ble)	12 (12x)	12x Pluggable LX fiber optic device	See note <u>a.</u>

Table 171 Valid Volume 2 Compliance Categories

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Category	Product Type	Qualifier	Product Definition	Reference ^a
NMA_ID	NM (Not an IB defined Module or	xCA (Functionality of an IB defined Adaptor; a TCA or HCA) _ID (Chassis GUID)	An IB TCA or HCA function whose phys- ical implementation does not comply with the InfiniBand Volume 2 Specifica- tion and provides a Chassis GUID.	Section 15.3.44 on page 721
NMA_NID	slot form factor)	xCA (Functionality of an IB defined Adaptor; a TCA or HCA) _NID (NoChassis GUID)	An IB TCA or HCA function whose phys- ical implementation does not comply with the InfiniBand Volume 2 Specifica- tion and provides no Chassis GUID.	Section 15.3.45 on page 722
NMS_ID		S (Functionality of an IB defined Switch) _ID (Chassis GUID)	An IB Switch function whose physical implementation does not comply with the InfiniBand Volume 2 Specification and provides a Chassis GUID.	Section 15.3.46 on page 724
NMS_NID		S (Functionality of an IB defined Switch) _NID (No Chassis GUID)	An IB Switch function whose physical implementation does not comply with the InfiniBand Volume 2 Specification and provides no Chassis GUID.	Section 15.3.47 on page 725
NMR_ID		R (Functionality of an IB defined Router) _ID (Chassis GUID)	An IB Router function whose physical implementation does not comply with the InfiniBand Volume 2 Specification.	Section 15.3.48 on page 726
NMR_NID		R (Functionality of an IB defined Router) _NID (No Chassis GUID)	An IB Router function whose physical implementation does not comply with the InfiniBand Volume 2 Specification.	Section 15.3.49 on page 727
BM	BM	N/A	Baseboard Manager Software	Section 15.3.50 on page 728

Table 171 Valid Volume 2 Compliance Categories

a. These compliance categories are named but not defined in this level of documentation.

15.2.1 VOLUME 2 COMPLIANCE QUALIFIERS

Compliance Qualifiers indicate which compliance statements apply only if a product supports an optional feature or specified combination of optional features.

Some compliance statements may apply to multiple Compliance Categories, and thus appear in the Compliance Statement List under each applicable Category. Some of these "shared" compliance statements may include Qualifiers associated with functionality that is optional in some Categories and mandatory in others. In each Category where the functionality is mandatory, the associated Qualifier will be shown in **bold italics** for that Category's "Valid Qualifier's" entry in <u>Table 171</u>. (This release of the specification does not include any such qualifiers or valid qualifiers entries.)

15.2.1.1 CLAIMING SUPPORT FOR OPTIONAL FEATURES

C15-1: If a product claims to support a given optional feature, the product **must** comply with **all** compliance statements that apply to that optional feature.

For example, a Protocol Aware Module that claims to compliance with "Enhanced Signaling" must comply with all statements under the relevant Protocol Aware Statement List that apply, given the ES Qualifier.

A product **shall not** include in its list of supported *optional* features any features that are in fact *mandatory* for the Category the product claims compliance to. Qualifiers for these mandatory features will be shown in **bold italics** in <u>Table 171</u>, as necessary.

A product may claim support for multiple optional features, in which case the product must comply with all compliance statements that apply to the particular set of optional features claimed by the product, noting that some compliance statements apply only for specific combinations of qualifiers.

<u>Table 172</u> lists and describes the Volume 2 Compliance Qualifiers that a product can claim compliance to. To abbreviate the optional support, one or more Qualifiers can be listed after the Category in braces. For example, a Standard IB Protocol Aware Module that supports Enhanced Signaling can be abbreviated with PS{ES}.

Table 172 Volume 2 Compliance Qualifiers

Qualifier	Description
ES	Enhanced Signaling (Release 1.2 extensions)

If an optional compliance statement does not contain a valid qualifier, refer to the text of the optional compliance statement to determine its applicability. The text of a compliance statement always takes precedence over the compliance qualifier.

15.2.1.2 COMPLIANCE STATEMENTS WITH MULTIPLE QUALIFIERS

Some compliance statements may contain combinations of Qualifiers, and apply only if the specified combination is true. For example, a compliance statement beginning with "RD and Atomics:" applies only if *both* RD and Atomics are supported. If a compliance statement begins with "RD or Atomics:", the statement **shall** apply if *either* RD or Atomics is supported.

15.2.2 COMPLIANCE STATEMENT LISTS

Within each Compliance Category section is a list of the compliance statements that apply to that particular category. Here is a sample list entry: Volume 2 Compliance Summary

• o5-9.2.1:ES:Link Initialization and Training, enhanced Page 119

15.2.2.1 HYPERTEXT LINKS

Online versions of this specification have hypertext links present before each of the lines in the Compliance Statement lists. These links are indicated by the "•" at the beginning of the line and will lead to the actual statement in the body of the specification that contains the details for each of the compliance entries.

Each Compliance Statement List entry also contains the page number for use with hard-copy versions of the specification.

15.2.2.2 COMPLIANCE STATEMENT LABELS

All formal compliance statements throughout the specification are labeled so they can be uniquely identified. Each label begins with either a "C" or an "o", indicating whether the compliance statement applies in all cases with respect to its category or whether the compliance statement is qualified with respect to optional features. The "o" is uncapitalized to make it more easily distinguishable from the "C" in Compliance Statement Lists.

The next portion of the label is the number of the chapter in which the formal compliance statement appears. The final portion of the label is a compliance statement number, which starts with "1" in each chapter. "C" and "o" compliance statements are numbered independently.

15.2.2.3 COMPLIANCE STATEMENT TITLES

Each line within a Compliance Statement List contains a brief title for the respective compliance statement. Because of the limited space and lack of context, each title is only intended to convey the topic of the compliance statement, and not necessarily convey its actual requirements.

Compliance statements that apply only to optional functionality is indicated by the presence of one or more Qualifiers at the beginning of the title, followed by a colon. For example, the above sample Compliance Statement Title contains the "ES" qualifier.

15.2.3 COMMON REQUIREMENTS

Some Compliance Categories share common requirements, such as those that apply to all ports. To avoid unnecessary duplication, certain common requirement sets have been collected and referenced by the appropriate Compliance Categories instead of replicating those lists of requirements under each separate Category.

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15.3 COMPLIANCE REQUIREMENTS

15.3.1 CATEGORY "CU" - CHASSIS, UNMANAGED

In order to claim compliance to the InfiniBand Volume 2 specification at a compliance category of "CU", or "Chassis, Unmanaged", a product **shall** meet all requirements specified below. 5

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	C4-2:	Primary Port (1) backplane connection	Page 72	7
	C6-1:	General coverage statement for Obsolete	Page 177	
	C6-1.2.1:	General coverage statement for signaling, SDR	Page 177	8
	06-1.2.1:	ES: DDR operation is optional	Page 177	9
	06-1.2.1:	ES: QDR operation is optional	Page 177	4.0
	06-1.2.1:	ES: Non-contiguous LinkSpeed support	Page 177	10
	06-1.2.2:	ES: DDR speed operation	Page 177	11
•	06-1.2.3:	ES: QDR speed operation.	Page 177	4.0
•	C6-2:	ESD Requirements - Obsolete	Page 178	12
•	C6-2.1.1:	ESD Requirements, recoverability - Obsolete	Page 178	13
	C6-2.2.1:	ESD Requirements	Page 178	1 /
	C6-2.2.2:	ESD Requirements, recoverability	Page 178	14
	C6-3:	Unexpected not removal or insertion allowed	Page 178	15
		Specifications apply within defined env Obsolete	Page 178	16
	C6-4.2.1:	Specifications apply within defined environment	Page 178	10
		Output Requirements - Obsolete	Page 180	17
		DDD link anord operation	Page 180	18
	00-7.2.1:	ODP link speed operation	Page 180	10
	00-7.2.2.	DC Plocking Canaditors for Packplane Obsolete	Page 100	19
	00^{-1}	DC Blocking Capacitors for Backplane at SDP	Page 100	20
	00-7.2.1.	DC Blocking may be located at transmitter	Page 180	20
	00-2.	DC Blocking may be located at transmitter	Page 180	21
	C6-9	litter limits and equalization requirements - Obsolete	Page 182	22
	C6-9 2 1	litter limits and equalization requirements	Page 182	
	C6-9 2 2	ES: litter limits & equalization requirements at SDR	Page 183	23
	C6-9.2.3:	ES: Jitter limits & equalization at DDR & QDR	Page 183	24
	C6-11:	High speed input requirements - Obsolete	Page 191	25
	C6-11.2.1	High speed input requirements at SDR.	Page 191	20
	06-11.2.1	High speed input requirements at SDR	Page 191	26
	06-11.2.2	ES: High speed input requirements at QDR	Page 191	27
	C6-12:	Beacon detection required - Obsolete	Page 198	~ 1
	C6-13:	Beacon detector requirements defined Obsolete	Page 198	28
	C6-13.2.1	:Beacon detection required	Page 198	29
	C6-13.2.2	:Beacon detector requirements defined	Page 198	20
	C6-14:	Receivers false data generation - Obsolete	Page 199	30
	C6-14.2.1	:Receivers must not generate false data w/ no input	Page 199	31
•	C6-16:	Attenuation (loss) limits defined Obsolete	Page 199	20
•	C6-16.2.1	Attenuation limits defined for topologies at SDR.	Page 199	32
	C6-16.1.1	Backplane connection amplitude and Obsolete	Page 203	33
	C6-16.1.2	Cable connection amplitude and eye Obsolete	Page 203	3/
		Backplane connection amplitude and eye at SDR	Page 203	54
	00-16.2.1	ES. DER with compliant tx & channel, DDR	Page 203	35
	C6-17-		Page 204	36
		Multiple backplane ports: configuration labeling	Page 200	00
	CQ_Q.	Filler modules in unoccupied slots	Dana 382	37
	C9-21	Backnlane connector spacing-adjacent	Page 302	38
	C9-22	Backplane connector spacing within a tall slot	Page 305	
	C9-23	Chassis slot dimensional requirements	Page 397	39
	C9-24	Chassis slot cooling requirements	Page 399	40
	C9-29:	Chassis EMI seal	Page 402	ЛЛ
	C9-30:	EMI gasket material & compression	Page 402	41
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	• C10-8:	Backplane connector pin assignment Page 419	4
	• 010-8.1.1	If implementing multiple 4X ports Page 419	1
	• 010-8.1.2	If implementing multiple 1X ports Page 419	2
	C10-9.1.1	:backplane wiring impedance Page 424	_
	C10-10:	Backplane connector intermateability Page 424	3
	C10-11:	Backplane connector outline dimensions Page 424	Δ
	• C10-12:	Backplane requirements, compression/press-fit Page 430	_
	• C10-13:	Backplane connector mechanical requirements Page 432	5
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	C10-15:	Backplane connector environmental requirements Page 434	0
	• C11-2:	Minimum power port capability Page 435	7
	• 011-1:	Additional power port capability Page 435	8
	• C11-3:	VBxCap indication of less than 25W Page 435	0
	• C11-8:	VBxCap electrical values Page 440	9
	• C11-11:	VBxCap on delivery of less than 50W Page 441	10
	• C11-12:	VBxCap on delivery of 50W or more Page 441	10
	• C11-13:	VBxPFW L electrical values Page 441	11
	• C11-14:	VBxPFW L function provision Page 441	12
	• C11-15:	VBxPFW L minimum low time Page 442	
	• C11-16:	VBxPFW L minimum high time Page 442	13
	• C11-17:	Auxiliary power contact electrical values Page 446	14
	• C11-19:	IMxDat, IMxClk electrical values Page 448	1-1
	• C11-23:	IB-ML capacitive load Page 449	15
	• C11-24:	IB-ML pull-ups Page 449	16
	• C11-26:	IMxInt L electrical values Page 449	10
	• C11-27:	IMxPRst electrical values Page 451	17
	o11-6:	IMXPRst monitoring for module presence Page 452	18
	o11-8:	Chassis performs reset to module using IMxPRst Page 452	10
	o11-9:	Chassis performs reset prior to module operation Page 452	19
	• C11-31:	IMxPReq_L electrical values Page 452	20
	• 011-11:	IMxPReq_L used to reenable power subsystems Page 452	20
	• C12-15:	VBxEn_L assertion Page 470	21
	• C12-16:	Minimum auxiliary power supply Page 470	22
	• 012-6:	Tall module auxiliary power. Page 470	
	• C13-56:	Non-volatile xInfo device Header and Record Page 600	23
	C13-64:	xInfo Headers Page 602	24
	• C13-65:	xInfo Format Page 603	05
	• C15-1:	Optional features: compliance statement applicability . Page 660	25
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Α;	SSIS, ACTIV	ELY MANAGED	27
			28
	In order to	claim compliance to the InfiniBand Volume 2 specification at a	29
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15.3.2 CATEGORY "CA" - CHASSIS, ACTIVELY MANAGED

In order to claim compliance to the InfiniBand Volume 2 specification at a compliance category of "CA", or "Chassis, Actively Managed", a product **shall** meet all requirements specified below.

	C4-2: C6-1: C6-1.2.1: o6-1.2.1: o6-1.2.1:	Primary Port (1) backplane connection Page 72 General coverage statement for Obsolete Page 177 General coverage statement for signaling, SDR Page 177 ES: DDR operation is optional	32 33 7 34 7 34 7 35
•	06-1.2.1:	ES: QDR operation is optional	35
•	06-1.2.1:	ES: Non-contiguous LinkSpeed support Page 177	7 00
•	o6-1.2.2:	ES: DDR speed operation Page 177	7 36
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15.3.12 CATEGORY "CC01" - COPPER CABLE, 1X

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	in order to claim compliance to the miniband volume 2 specifi	cation at a
	compliance category of "CC04", or "Copper Cable, 4x", a proc	uct shall
	meet all requirements specified below.	
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15.3.14 CATEGORY "CC08" - COPPER CABLE, 8X

In order to claim compliance to the InfiniBand Volume 2 specification at a compliance category of "cc08", or "Fiber optic cable, Short haul, 8x", a product **shall** meet all requirements specified below. 4

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	order to claim compliance ompliance category of "C neet all requirements spece C6-1 : General coverage	ce to the InfiniBand Volume 2 sp C12", or "Copper Cable, 12x", a cified below.	ecification at a 8 product shall 9 10 11	
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In order to claim compliance to the InfiniBand Volume 2 specification at a compliance category of "CC12-4x", or "Copper Cable, 12x to 3-4x", a product **shall** meet all requirements specified below.

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15.3.17 CATEGORY "CS01" - COPPER SFP CABLE, 1X

In order to claim compliance to the InfiniBand Volume 2 specification at a	22
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• C6-2.1.1: ESD Requirements, recoverability - Obsolete Page 178	29
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• C6-2.2.2: ESD Requirements, recoverability Page 178	21
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	In order to claim compliance to the InfiniBand Volume 2 compliance category of "FS01", or "Fiber optic cable, S product shall meet all requirements specified below.	! specification at a Short haul, 1x", a
	 C8-1: 1x fiber cable summary requirements C8-15: 1X Optical Cable, connector requirements C8-17: 1x-SX optical connector adapter & receptacle of C8-23: Optical fiber cable all, requirements - Obsolete C8-23.2.1:Optical fiber cable all, requirements C8-23.2.2:8x-SX Optical fiber cable all, requirements C8-24: Optical Cables, Passive loss - Obsolete C8-25: 1X Optical adaptor & splice requirements o9-32.1.1:InfiniBand port icon C15-1: Optional features: compliance statement applice 	Page 287 Page 334 Page 335 Page 342 Page 342 Page 342 Page 342 Page 344 Page 344 Page 344 Page 344 Page 344 Page 345 Page 408 Page 408 Page 660
15.3.19 CATEGORY "FS04" -	FIBER OPTIC CABLE, SHORT HAUL, 4X	
	In order to claim compliance to the InfiniBand Volume 2 compliance category of "FS04", or "Fiber optic cable, S product shall meet all requirements specified below.	! specification at a Short haul, 4x", a
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15.3.20 CATEGORY "FS08" - FIBER OPTIC CABLE, SHORT HAUL, 8X

In order to claim compliance to the InfiniBand Volume 2 specification at a compliance category of "FS08", or "Fiber optic cable, Short haul, 8x", a product **shall** meet all requirements specified below.

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15.3.21 CATEGORY "FS12" - FIBER OPTIC CABLE, SHORT HAUL, 12X

In order to claim compliance to the InfiniBand Volume 2 specification at a compliance category of "FS12", or "Fiber optic cable, Short haul, 12x", a product **shall** meet all requirements specified below.

 C8-3: C8-21: C8-23: C8-23.2.1 C8-23.2.1 C8-24: C8-24: C8-24:1.1 C8-27: o9-32.1.1 	12x Fiber optic cable summary requirementsPage 29412x-SX Optical Cable, connectors specificationsPage 340Optical fiber cable all, requirements - ObsoletePage 342I:Optical fiber cable all, requirementsPage 3422:8x-SX Optical fiber cable all, requirementsPage 342Optical Cables, Passive loss - ObsoletePage 344I:Optical Cables, Passive lossPage 344	18 19 20 21 22 23
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product sn	all meet all requirements specified below.	29
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• C8-18:	1x-LX optical connector adapter & receptacle color Page 335	33
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15.3.23 CATEGORY "FL04" - FIBER OPTIC CABLE, LONG HAUL, 4X

In order to claim compliance to the InfiniBand Volume 2 specification at a compliance category of "FL04", or "Fiber optic cable, Long haul, 4x", a product **shall** meet all requirements specified below.

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15.3.24 CATEGORY "PC01" - PORT, COPPER CABLE, 1X

In order to claim compliance to the InfiniBand Volume 2 specification at a compliance category of "PC01", or "Port, Copper Cable, 1x", a product **shall** meet all requirements specified below.

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	in order to		cation at a
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15.3.28 CATEGORY "PS01"- PORT, SHORT HAUL FIBER, 1X

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•	C8-6.2.2:	Optical Transmitter Mask, Nx-SX & 1x-LX - at DDR	Page 297	0
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15.3.29 CATEGORY "PS04" - PORT, SHORT HAUL FIBER, 4X

In order to claim compliance to the InfiniBand Volume 2 specification at a compliance category of "PS04", or "Port, Short haul fiber, 4x", a product **shall** meet all requirements specified below.

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	In order to claim compliance to the InfiniBand Volume compliance category of "PS12", or "Port, Short haul fib shall meet all requirements specified below.	2 specification at a ber, 12x", a product 12 13
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	In order to claim compliance to the InfiniBand Volume compliance category of "PL01", or "Port, Long haul fib shall meet all requirements specified below.	2 specification at a 36 er, 1x", a product 37 38
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15.3.32 CATEGORY "PL04" - PORT,	LONG HAUL FIBER, 4X	19
In ord	ler to claim compliance to the InfiniBand Volume 2 specificati	ion at a 20
comp	pliance category of "PL04", or "Port, Long haul fiber, 4x", a pre-	roduct
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shall • C8- • C8-	eet all requirements specified below. 2.1.3: 4x-LX Optical transceivers	22 age 290 23 age 296 24
Shall • C8- • C8- • C8- • C8-	2.1.3: 4x-LX Optical transceivers	22 age 290 23 age 296 24 age 296 25
Shall • C8- • C8- • C8- • C8- • C8- • C8-		22 age 290 23 age 296 24 age 296 25 age 296 25 age 296 26
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Shall C8- C8- C8- C8- C8- C8- C8- C8-	meet all requirements specified below.21.3: 4x-LX Optical transceiversPa4: BER requirements for all optical ports.Pa5: Optical Port, Tx Mask, Polarity, & Quie ObsoletePa6: Optical Port, Signal grounding requirementsPa6: Optical Port, Quiescent conditions &Optical PolarityPa6: Optical Transmitter Mask, Nx-SX & 1x-LXPa6: Optical Transmitter Mask, Nx-SX & 1x-LXPa6: Optical Transmitter Mask, Nx-SX & 1x-LXPa6: Optical Transmitter Mask, Nx-SX & 1x-LX - at DDRPa6: 1: Nx-SX & 1x-LX - Optical Jitter requirements - ObsoletePa7: Jitter requirements for all Optical Ports - ObsoletePa7: 1: Nx-SX & 1x-LX - Optical Jitter requirements at SDRPa7: 2: Ax-LX Optical Jitter Requirements - ObsoletePa7: 2: Nx-SX & 1x-LX Optical Jitter requirements at DDRPa7: 2: Nx-SX & 1x-LX Optical Jitter requirements at DDRPa7: 2: Nx-SX & 1x-LX Optical Jitter RequirementsPa7: 2: Nx-SX & 1x-LX Optical Jitter RequirementsPa7: 4x-LX Optical Jitter RequirementsPa8: 0ptical ports, skew while operating at DDRPa8: 1: Optical ports, skew while operating at QDRPa9: 12: 2: 4x-LX Optical Eye Safety, Tx & Rx - ObsoletePa14: Optical Receptacle requirementsPa14: Optical Port, receptacle and fiber orientationPa20: 1: 2: 4x-LX Optical Port, receptacle and fiber orientationPa20: 1: 2: 4x-LX Optical Port, scoptacle and fiber orientationPa21: 0ptical Port Aux power	22 age 290 23 age 296 24 age 296 25 age 297 26 age 297 27 age 297 28 age 302 30 age 302 30 age 302 31 age 302 32 age 307 33 age 307 34 age 307 35 age 319 36 age 333 37 age 354 39 age 408 40 age 660 41

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15.3.33 CATEGORY "PP01" - PORT, PLUGGABLE, 1X

In order to claim compliance to the InfiniBand Volume 2 specification at a 2 compliance category of "PP01", or "Port, Pluggable, 1x", a product shall 3 meet all requirements specified below. 4

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C6-7.1.1: Jitter, 1x Pluggable Port Type 2 - Obsolete Page 180	5
C6-7.2.2: Jitter, 1x Pluggable Port Type 2 Page 180	6
C6-16.1.3: Pluggable connection amplitude and Obsolete Page 203	7
C6-16.2.4: Pluggable connection amplitude and eye at SDR Page 203	0
C7-15.1.3:1x Pluggable SFP port, Physical & Mechanical Page 234	0
C7-15.1.4:1x Pluggable SFP port, electrical requirements Page 235	9
• o9-32.1.3: InfiniBand Icon Visibility Page 408	10
C15-1: Optional features: compliance statement applicability Page 660	11

15.3.34 CATEGORY "PP04" - PORT, PLUGGABLE, 4X

In order to claim compliance to the InfiniBand Volume 2 specification at a compliance category of "PP04", or "Port, Pluggable, 4x", a product shall meet all requirements specified below.

• C6-16.1.3: Pluggable connection amplitude and Obsolete	Page 203
• C6-16.2.4: Pluggable connection amplitude and eye at SDR	Page 203
• C7-15.2.1:4X Pluggable Port, Physical Requirements	Page 239
• C7-15.2.2:4X Pluggable Port, Pin Assignments	Page 240
• C7-15.2.3:4X Pluggable Port, General Signaling Interface	Page 242
 C7-15.2.4:4x Pluggable Port, High speed output requirements 	Page 243
C7-15.2.4:4X Pluggable Port, Electrical requirements.	Page 243
 C7-15.2.5:4x Pluggable Port, High speed input requirements 	Page 243
• C7-15.2.5:4X Pluggable Port, Input electrical requirements	Page 243
• C7-15.2.6:4X Pluggable Port, loss from IC to connector	Page 243
C7-15.2.7:4x Pluggable port, amplitude and eye opening	Page 243
• o9-32.1.3: InfiniBand Icon Visibility	. Page 408
• C15-1: Optional features: compliance statement applicability	Page 660

15.3.35 CATEGORY "AP04" - ACTIVE CABLE PORT, 4X

In order to claim compliance to the InfiniBand Volume 2 specification at a compliance category of "AP04", or "Active Cable Port, 4x", a product shall meet all requirements specified below.

 C7-28.2.6:4x active port, board connector. Page 265 C7-28.2.7:14x active port, connector pin assignment. Page 265 C7-28.2.8:4x active port, no 12V and 3.3V simultaneous. Page 265 C7-28.2.15:4x active cable, cable port connectors. Page 272 C7-28.1.1:4x active port, no 12V and 3.3V simultaneous. Page 272 C7-28.2.27:Active port, 12V voltage tolerance. Page 281 C7-28.2.29:Minimum current supplied, 12V. Page 281 C7-28.2.31:Minimum current supplied, 3.3V Page 281 C7-28.2.34:Active port, sense pin requirements. Page 281 C7-28.2.35:Active port, power disable when sense grounded. Page 282 C7-28.2.36:Active port, hot plugging. 	34 34 30 37 38 38 39 40 40
 C7-28.2.36: Active port, hot plugging	4′ 42
	- 7.6

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	 C7-28.2.38: Active port, load impedance C7-28.2.39: Active port, power when Bulk Power not available C7-28.2.40: Active port, bypassing at freq's over 100 MHz C15-1: Optional features: compliance statement applicability . 	Page 282 Page 282 Page 282 Page 660
15.3.36 CATEGORY "AP12" -	Active Cable Port, 12x	
	In order to claim compliance to the InfiniBand Volume 2 specifi	cation at a
	compliance category of "AP12", or "Active Cable Port, 12x", a shall meet all requirements specified below.	product
	 C7-28.2.9:12x active port, use by 8x active cable. C7-28.2.11:12x active port for 8x, no 12V & 3.3V simultaneous. C7-28.2.12:12X active port, board connector C7-28.2.13:12x active port, connector pin assignment. C7-28.2.14:12x active port, no 12V and 3.3V simultaneous. C7-28.1.2:12x active port, no 12V and 3.3V simultaneous. C7-28.1.3:12x active port, no 12V and 3.3V simultaneous. C7-28.2.27:Active port, 12V voltage tolerance. C7-28.2.29:Minimum current supplied, 12V. C7-28.2.31:Minimum current supplied, 3.3V. C7-28.2.31:Active port, sense pin requirements. C7-28.2.35:Active port, hot plugging. C7-28.2.37:Active port, hot plugging. C7-28.2.38:Active port, load impedance. C7-28.2.39:Active port, load impedance. C7-28.2.39:Active port, load impedance. C7-28.2.40:Active port, bypassing at freq's over 100 MHz. C15-1: Optional features: compliance statement applicability. 	Page 266 Page 267 Page 269 Page 269 Page 274 Page 274 Page 281 Page 281 Page 281 Page 282 Page 282
15.3.37 CATEGORY "AC04" -	ACTIVE CABLE, 4X	
	In order to claim compliance to the InfiniBand Volume 2 specifi	cation at a
	compliance category of "AC04", or "Active Cable, 4x", a produ	ct shall
	meet all requirements specified below.	
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	• C7-28.2.8:4X active cable, no 12V and 3.3V simultaneous	Page 265
		Page 272
	• C7 29 2 19:4x active cable, pin assignment	Page 272
	• C7 29 1 1.4x active cable, vcc not wired through	Page 272
	• C7 28 2 27. Active capie, no 12V and 3.3V simultaneous	Page 201
	C7 28 2 29 Active cable, 1∠V Voltage tolerance	Page 201
	• C7 28 2 20 Movimum outront draw at minimum voltage 40 /	Page 201
	• C7-20.2.30: Waximum current draw at minimum voltage, 12V	Page 201
	C7.29.2.32 Maximum current draw at max voltage, 2.21/ § 421/	Page 201
	• C7-28.2 34: Active cable sense pip requirements	Page 201
	• C7-28 2 35: Active cable, nower disable when some grounded	Dago 201
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• C15-1:

C7-28.2.36: Active cable, hot plugging Page 282

• C7-28.2.37: Active cable, short circuit protection Page 282

• C7-28.2.38: Active cable, load impedance Page 282 • C7-28.2.39: Active cable power when Bulk Power not available . . Page 282

• C7-28.2.40: Active cable, bypassing at freq's over 100 MHz Page 282

Optional features: compliance statement applicability . Page 660

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15.3.38 CATEGORY "AC12" - ACTIVE CABLE, 12X

In order to claim compliance to the InfiniBand Volume 2 specification at a compliance category of "AC12", or "Active Cable, 12x", a product shall 3 meet all requirements specified below. 4

-	(77.29.2.11)	Dogo 267	5
•	$\mathbf{C7-20.2.11}$ CT-20.2.1 Control to the cable for ox, no 12V as so simultaneous $\mathbf{C7-28.2.14}$:12x active cable, no 12V and 3.3V simultaneous	Page 207	6
é	C7-28.2.19: 12x active cable used for 8x, cable connector	Page 274	0
•	C7-28.2.20: 12x active cable used for 8x, metal backshell	Page 274	7
•	C7-28.2.21: 12x active cable used for 8x, pin assignment	Page 274	2
•	C7-28.2.22:12x active cable for 8x. Vcc not wired through	Page 274	0
•	C7-28.1.2: 12x active cable for 8x. no 12 & 3.3V simultaneous I	Page 274	9
•	C7-28.2.23:12x active cable, cable connector.	Page 277	10
•	C7-28.2.24:12x active cable, metal backshell	Page 277	10
•	C7-28.2.25:12x active cable, pin assignment	Page 277	11
•	C7-28.1.3:12x active cable, no 12V and 3.3V simultaneous I	Page 278	12
•	C7-28.2.27: Active cable, 12V voltage tolerance	Page 281	1 4
•	C7-28.2.28: Active cable, 3.3V voltage tolerance	Page 281	13
•	C7-28.2.30:Maximum current draw at minimum voltage, 12V I	Page 281	14
•	C7-28.2.32:Maximum current draw at minimum voltage, 3.3V	Page 281	
•	C7-28.2.33:Max current draw at max voltage, 3.3V & 12V I	Page 281	15
•	C7-28.2.34: Active cable, sense pin requirements I	Page 281	16
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15.3.39 CATEGORY "DC01" - DEVICE, COPPER SFP PLUGGABLE, 1X

In order to claim compliance to the InfiniBand Volume 2 specification at a compliance category of "DC01", or "Device, Copper SFP Pluggable, 1x", a product shall meet all requirements specified below.

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15.3.40 CATEGORY "DC04" - DEVICE, COPPER SFP PLUGGABLE, 4X

In order to claim compliance to the InfiniBand Volume 2 specification at a compliance category of "DC04", or "Device, Copper SFP Pluggable, 4x", a product **shall** meet all requirements specified below.

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In order to claim compliance to the InfiniBand Volume 2 specification at a compliance category of "DL01", or "Device Long haul fiber, Pluggable, 1x", a product **shall** meet all requirements specified below.

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In order to claim compliance to the InfiniBand Volume 2 specification at a compliance category of "NMA_ID", or "Non-Module Adapter with Chassis 33 GUID", a product **shall** meet all requirements specified below. 34

Symbol Encoding (8B/10B). Control Symbols and Ordered-sets - Obsolete Control Symbols & Ordered-sets ES: Control Symbols & Ordered-sets, enhanced Management Datagram Interface - Obsolete Management Datagram Interface ES: Management Datagram Interface, enhanced Packet Ordering Packet Formats Ya Dacket Formats	Page 80 Page 95 Page 95 Page 95 Page 104 Page 104 Page 105 Page 111 Page 113	36 37 38 39 40 41
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# 15.3.46 CATEGORY "NMS_ID" - NON-MODULE SWITCH, ID

In order to claim compliance to the InfiniBand Volume 2 specification at a compliance category of "NMS_ID", or "Non-Module Switch with Chassis 3 GUID", a product **shall** meet all requirements specified below. 4

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• C5-2.2.1:	Control Symbols & Ordered-sets	Page 95	7
05-221·	ES: Control Symbols & Ordered-sets enhanced	Page 05	1
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• 05-3.2.1:	ES: Management Datagram Interface, ennanced	Page 105	10
• C5-4:	Packet Ordering	Page 111	10
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o5-5:	Receiver Lane Reversal - 8x	Page 151	20
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• C5-14:	Clock Tolerance Compensation	Page 160	51
• C5-15.2.1	ES: Link Heartbeat	Page 167	32
• C5-15.2.2	:ES: Physical Layer Compliance Test (Phy Test)	Page 169	22
• 06-17.2.1	ES: Physical Test and Characterization Facilities	Page 211	55
• 09-32.1.1	InfiniBand port icon	Page 408	34
• 09-32.1.2	InfiniBand icon color	Page 408	25
• C13-5:	Non-Module Switch HM Features	Page 494	55
o13-4:	InfiniBand LEDs	Page 508	36
• C13-46:	Baseboard MAD commands	Page 580	27
• C13-47:	Baseboard MAD Commands	Page 580	57
• C13-48	IB-ML Maximum Transaction & Message Length	Page 580	38
• C13-51	MME Registers	Page 590	20
• 013-16:	IB-ML timeout parameters.	Page 597	39
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• 013-19:	xInfo Format	Page 601	ЛЛ
• C13-60	xInfo Records	Page 602	41
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15.3.47 CATEGORY "NMS_NID" - NON-MO	DDULE SWITCH, NO ID	5	5
In order to c compliance GUID", a pr • C5-1: • C5-2:	laim compliance to the InfiniBand Volume 2 specific category of "NMS_NID", or "Non-Module Switch wit oduct <b>shall</b> meet all requirements specified below. Symbol Encoding (8B/10B) Control Symbols and Ordered-sets - Obsolete	Cation at a th Chassis Page 80 Page 95	, 3 3 1 C 1 1
<ul> <li>C5-2.2.1:</li> <li>o5-2.2.1:</li> <li>C5-3:</li> <li>C5-3.2.1:</li> <li>o5-3.2.1:</li> <li>C5-4:</li> <li>C5-5:</li> <li>C5-6:</li> </ul>	ES: Control Symbols & Ordered-sets Management Datagram Interface - Obsolete Management Datagram Interface ES: Management Datagram Interface, enhanced Packet Ordering Packet Formats 1x Packet Format	Page 95 Page 95 Page 104 Page 104 Page 105 Page 111 Page 113	12 13 14 15 16
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<ul> <li>C5-13:</li> <li>o5-6:</li> <li>C5-14:</li> <li>C5-15.2.1:</li> <li>C5-15.2.2:</li> <li>o6-17.2.1:</li> <li>o9-32.1.1:</li> </ul>	Internal Serial Loopback Clock Tolerance Compensation ES: Link Heartbeat ES: Physical Layer Compliance Test (Phy Test) ES: Physical Test and Characterization Facilities InfiniBand port icon	Page 150 Page 159 Page 160 Page 167 Page 169 Page 211 Page 408	35 36 37 38
• 09-32.1.2: • C13-5: • 013-4: • C13-46:	InfiniBand icon color Non-Module Switch HM Features InfiniBand LEDs Baseboard MAD commands	Page 408 Page 494 Page 508 Page 580	59 10 11 12

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15.3.48 CATEGORY "NMR_ID	' - Non-Mo	DULE ROUTER, ID	9
	In order to o compliance GUID", a pi	claim compliance to the InfiniBand Volume 2 specif category of "NMR_ID", or "Non-Module Router wi roduct <b>shall</b> meet all requirements specified below	ication at a 1 th Chassis
	<ul> <li>C5-1:</li> <li>C5-2:</li> <li>C5-2:</li> <li>C5-2:</li> <li>C5-3:</li> <li>C5-3:</li> <li>C5-3:</li> <li>C5-3:</li> <li>C5-4:</li> <li>C5-6:</li> <li>O5-6:</li> <li>O5-7:2.1:</li> <li>O5-7.2.1:</li> <li>O5-9:2.1:</li> <li>O5-12:</li> <li>O5-5:</li> <li>O5-5</li></ul>	Symbol Encoding (8B/10B) Control Symbols and Ordered-sets - Obsolete Control Symbols & Ordered-sets ES: Control Symbols & Ordered-sets, enhanced Management Datagram Interface - Obsolete Management Datagram Interface ES: Management Datagram Interface, enhanced Packet Ordering Packet Format 1x Packet Format 2x Packet Format 4x Packet Format ES: 1x Packet Format, 8x ports ES: 4x Packet Format ES: 8x Packet Format ES: 10x Initialization and Training - Obsolete Link Initialization and Training, enhanced Serial Data Inversion - Obsolete Lane Reversal - 4x - Obsolete Lane Reversal - 4x - Obsolete Lane Reversal - 4x Lane Reversal - 12x State Machine Delays Transmitter Lane Reversal - 4x Transmitter Lane Reversal - 4x Transmitter Lane Reversal - 4x Transmitter Lane Reversal - 4x Receiver Interface and Behavior Receiver Lane Reversal - 4x Receiver L	Page 80       14         Page 95       19         Page 95       10         Page 104       17         Page 104       18         Page 105       18         Page 105       18         Page 105       18         Page 104       18         Page 105       14         Page 105       14         Page 113       20         Page 113       21         Page 113       21         Page 113       21         Page 114       22         Page 115       23         Page 116       24         Page 117       25         Page 118       24         Page 119       25         Page 119       26         Page 119       27         Page 119       26         Page 119       27         Page 119       26         Page 119       26         Page 119       37         Page 119       38         Page 147       37         Page 148       37         Page 151       37         Page 151       37         Page
	<ul> <li>o5-6:</li> <li>C5-14:</li> <li>C5-15.2.1</li> <li>C5-15.2.2</li> </ul>	Internal Serial Loopback Clock Tolerance Compensation ES: Link Heartbeat ES: Physical Layer Compliance Test (Phy Test)	Page 159       4         Page 160       4         Page 167       4         Page 169       4

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<ul> <li>o6-17.2.1:ES: Physical Test and Characterization Facilities Page 211</li> <li>o9-32.1.1: InfiniBand port icon</li></ul>	1 2 3 4 5 6 7 8 9 10 11
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# 15.3.49 CATEGORY "NMR_NID" - NON-MODULE ROUTER, NID

In order to claim compliance to the InfiniBand Volume 2 specification at a compliance category of "NMR_NID", or "Non-Module Router without Chassis GUID", a product **shall** meet all requirements specified below.

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•	C5-1	Symbol Encoding (8B/10B)	Page 80	4 -
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•	C5-2.2.1:	Control Symbols & Ordered-sets	Page 95	18
•	05-2.2.1:	ES: Control Symbols & Ordered-sets, enhanced	Page 95	10
•	C5-3:	Management Datagram Interface - Obsolete	Page 104	19
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•	05-6.2.1:	ES: 1x Packet Format, 8x ports	Page 113	20
•	C5-7:	4x Packet Format	Page 114	24
•	C5-7:	4x Packet Format, 12x ports	Page 114	25
•	05-7.2.1:	ES: 4x Packet Format, 8x ports	Page 115	
•	05-7.2.1:	ES: 8x Packet Format	Page 116	26
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•	C5-9:	Link Initialization and Training - Obsolete	Page 118	28
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•	05-9.2.1:	ES: Link Initialization and Training, enhanced	Page 119	20
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•	05-9.2.1:	Serial Data Inversion	Page 119	31
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•	05-2:	Lane Reversal - 12x - Obsolete	Page 119	SZ
-	05-9.2.1:		Page 119	33
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	05-5	Receiver Lane Reversal - 4x	Page 151	39
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	05-5	Receiver Lane Reversal - 12x	Page 151	11
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<ul> <li>05-6:</li> <li>C5-14:</li> <li>C5-15.2.2</li> <li>C5-15.2.2</li> <li>06-17.2.1</li> <li>09-32.1.1</li> <li>09-32.1.2</li> <li>C13-1:</li> <li>013-4:</li> <li>C13-47:</li> <li>C13-48:</li> <li>C13-51:</li> <li>013-16:</li> </ul>	Internal Serial LoopbackPage 159Clock Tolerance CompensationPage 160I:ES: Link HeartbeatPage 1672:ES: Physical Layer Compliance Test (Phy Test)Page 1691:ES: Physical Test and Characterization FacilitiesPage 2111:InfiniBand port iconPage 4082:InfiniBand icon colorPage 4082:InfiniBand LEDsPage 508Baseboard MAD CommandsPage 580IB-ML Maximum Transaction & Message LengthPage 590IB-ML timeout parametersPage 597	1 2 3 4 5 6 7 8
• 09-32.1.2	InfiniBand icon color Page 408	_
C13-1:	For Hardware Management, follow NMS_NID Page 480	5
o13-4:	InfiniBand LEDs Page 508	6
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• C13-65:	xInfo Format Page 603	
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• C15-1:	Optional features: compliance statement applicability . Page 660	10
C15-1:	Optional features: compliance statement applicability . Page 660	13
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# 15.3.50 CATEGORY "BM" - BASEBOARD MANAGER

In order to claim compliance to the InfiniBand Volume 2 specification at a compliance category of "BM", or "Baseboard Manager", a product **shall** meet all requirements specified below.

• C13-11:	Graceful Hot Removal Handshake with BM	Page 506
C13-47:	Baseboard MAD Commands	Page 580
C13-48:	IB-ML Maximum Transaction & Message Length	Page 580
• C15-1:	Optional features: compliance statement applicability .	Page 660

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	1	7
	1	8
	1	9
	2	0
	2	1
	2	2
	2	3
	2	4
	2	5
	2	6
	2	7
	2	8
	2	9
	3	0
	3	1
	3	2
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	3	5
	3	6
	3	7
	3	8
	3	9
	4	0
	4	1
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# ANNEX A1: MECHANICAL ANNEX

#### A1.1 MODULE DESIGN EXAMPLES

The design of the module cover is left extremely flexible. Figure 95 on page 364 describes required cover dimensions to ensure proper clearances with other modules and with chassis slot guides. Material and internal cover features are entirely flexible. It is recommended, however, that if a metal cover is used, careful attention be paid to the ground contact between the module and cover in order to avoid potential EMI problems. Figure 183 shows an example of a cover that might be used on an IB Module.





# Figure 184 Example IB Module Carrier

The module carrier is also intentionally left somewhat flexible in design with mainly interface dimensions and material compatibility specified. The drawings provided in this annex are of an example design that has been detailed and prototyped and should provide an excellent starting point.





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The example in Figure 187 implies a board thickness specific to this example only. Refer to Section 9.3.3, "Board Thickness," on page 395 for complete information on board thickness.





# Figure 189 Example IB Carrier Flat Pattern

# A1.2 COMPUTATIONAL FLUID DYNAMICS (CFD) RESULTS

37 The InfiniBand Module has been sized specifically to operate within component temperature limits in what is considered a severe system imple-38 mentation. CFD models and empirical testing have been employed to 39 determine module and system resistance's and flow rates. The models 40 have also been used to study the effect of variables such as card height, slot spacing, vent size, etc. on module flow velocities and component tem-

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peratures. These models may be a useful starting point for the engineer when designing a system to insure that component temperature goals are met, therefore a reference design has been included in this annex.

The reference design was constructed using Flotherm V2.2 and consists 4 of an enclosure 560 mm in length, 133 mm tall, and 217 mm wide. This model represents the implementation of seven InfiniBand Modules in a system enclosure. The airflow is modeled back-to-front (airflow enters module near InfiniBand connector and exits at front vent), but the airflow is allowed to be in either direction (front-to-back or back-to-front) across the module. Directly behind the IB Module section is a fan/blower which splits the enclosure into a low-pressure (rear) compartment and a highpressure (front) compartment. Typical components occupying the front compartment of a system would be hard drives, tape drives, power supplies, etc. These components may significantly affect the system by adding flow resistance and heat to the incoming air. Figure 190, shows an isometric view of the Flotherm model.



This reference design assumes the majority of the front compartment to be occupied by a power supply with some area around its perimeter left to bleed ambient air in and around the supply. The power supply resistance was modeled using a Flotherm linear source term with a loss coefficient defined for each direction of the Cartesian axis system. In addition, 10 C of preheat was assumed across the power supply. The fans modeled were high performance 120 mm fans in series, with two pairs of fans per system. Four of the InfiniBand Modules were explicitly modeled with each component on the circuit board represented by a cuboid or volume source. The remaining modules were modeled with one volume source term each to reduce the size of the model. On the modules that were modeled explicitly, cuboids were used to model components with 2 watts or less heat dissipation, with the heat being dissipated conducted to the board and air. For components with more then 2 watts of heat dissipation, volume source terms were used to model the components with all the heat convected to the air (i.e. components were not coupled to the board). The total model size was about 250,000 nodes.

The goal of the engineer is to insure that component temperature goals are met. To this end, it is necessary to layout components on the board to insure that they receive adequate airflow. In addition, it may be necessary to install heat sinks on high heat density components. It also may be necessary to install a flow defector on the ESD cover to redirect airflow. A flow deflector will redirect airflow over board components, while reducing the shadowing effect caused by the backplane. Figure 191, shows velocity vectors generated by a CFD model across the InfiniBand Module. In this CFD model a flow deflector was used to redirect airflow towards the center of the board. From the figure it can be seen that the airflow is fairly uniform with only minimal recirculation near the backplane. This figure may be used as a reference for insuring adequate velocities across the module.



# Figure 191 Velocity Vector Plot Through Module

# A1.3 MODULE PRESSURE DROP TESTING

#### A1.3.1 GENERAL DESCRIPTION OF A MODULE PRESSURE DROP TEST FIXTURE

The module must have the airflow/pressure drop characteristics as shown in Figure 88. The module pressure drop is defined as the difference in static pressure from point A to point B of Figure 192 on page 741. Although systems may move air in either direction through the module, one direction has been chosen to characterize a module's pressure drop.

An airflow test fixture is required to test that the airflow and pressure of the module fall within the required limits. In general, such a fixture should deliver airflow at the backplane (point A) that is mostly unidirectional towards the module. This can be achieved by constructing a test fixture with a four-

walled chamber just upstream of the module that is sufficiently long (approximately 250mm minimum) to allow for the airflow to fully develop. Flow straighteners are recommended that can assist in straightening the airflow. The fan that supplies the air should be sufficiently upstream of the flow straighteners (approximately 250mm minimum) in order to reduce fan-induced swirling effects. In addition, the width of the four-walled chamber should be large enough (at least 200mm overall wider than the air inlet to the module in both axes) to minimize wall-induced turbulence effects. The fixture must measure the difference in air pressure at point A with respect to ambient air (i.e. outside the fixture) as a function of volumetric airflow.

### A1.3.2 SPECIFIC EXAMPLE OF A MODULE PRESSURE DROP TEST FIXTURE

There are several instruments available to measure pressure drop and volumetric flow rate, such as solid state pressure transducers and manometers (to measure pressure), hot wire anamometers and thermistor sensors (to measure velocity, so multiples are required across a known cross-sectional area to determine volumetric airflow rates) and manometer-across-a-calibrated-nozzle (for measuring airflow rate). Figure 192 on page 741 is of a schematic of a pressure drop test fixture based upon the lowest-cost available technologies. The overall size of the test fixture is approximately 1000mm long by 240mm wide by 240mm tall and construction was based upon standard 6mm (1⁄4 inch) plywood. The test fixture includes four main components: the airmover (fan), the airflow measuring device (in this case, a nozzle and manometer A), the static pressure measurement device (manometer B), and the module holder. A more detailed description follows.



Figure 192 Schematic of pressure drop test fixture

The fan has sufficient capacity to supply enough volumetric airflow and static pressure to overcome the resistance in the fixture while supplying the required airflow and pressure to the module under test. A DC fan was selected so that the it's speed can be varied in order to test various airflow-pressure drop points of the module. In this model, a standard 6-inch diameter by 2-inch deep fan was selected. This type of fan is readily available from most fan vendors. In the model, the fan was powered by a simple 12V (2A) power supply.

Two layers of standard window screen mesh (Screening A) with 1.60mm (.062 inch) square openings that are spaced 25 mm (1.00 in) apart are located approximately 250mm downstream of the fan in order to approximately straighten the airflow before the air reaches the nozzle. The volumetric airflow is measured by means of measuring the pressure drop across a calibrated nozzle using manometer A. The manometer that was selected is a simple, low-cost fluid/mechanical manometer (Dwyer model number 40-1) from Dwyer Instruments (Michigan City, Indiana, USA) that

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is connected via 5.0mm (0.20 in) diameter plastic flexible tubing to barb fittings on the test fixture that are both upstream and downstream of the nozzle. By using the related calibration curve for the nozzle, volumetric airflow can be deduced.

Using a calibrated nozzle is critical to yielding accurate results for volu-5 metric airflow. The nozzle for this model was designed and sized for a 6 standard module, using the "minor headloss" equation found in any fluid mechanics textbook. It was machined from 25.4 mm (1.00 inch) thick alu-8 minum and consisted of a 15.52 mm (0.611 inch) diameter hole and a 30 9 degree (per side) by 3.10 mm (0.122 inch) deep chamfered edge that is oriented on the upstream side of the nozzle (see detail in Figure 192 on page 741). The overall outer dimension of the nozzle is not critical. This particular nozzle was calibrated in an airflow chamber/wind tunnel (see Figure 193 on page 742). The volumetric airflow can be determined by measuring the pressure across the nozzle, then using Figure 193 on page 742 to determine the resultant volumetric airflow.



### Figure 193 Nozzle calibration curve for standard module

A second dual-layer standard screen mesh (Screening B) is located ap-38 proximately 250mm downstream of the nozzle in order to approximately 39 straighten the airflow before the air reaches the module under test. The 40 module is supported by walls that mimic the walls of the enclosure sur-41 rounding the module (including the backplane) as described in Figure 192 42

InfiniBandSM Trade Association

on page 741. Manometer B (the same type as used for manometer A) is used to measure the static pressure just upstream of the module under 2 test and as described in Figure 192 on page 741. 3 The gap around the module between the connector housing and the in-4 side of the slot should be sealed to prevent leakage and to better mimic 5 EMI gaskets that will be in place on a final system. 6 7 A1.3.3 OPERATION OF THE PRESSURE DROP TEST 8 Fixture example: 9 10 To operate the test fixture, the operator sets the speed of the fan so that 11 the volumetric airflow is set to a desired rate by reading manometer A, 12 then the related static pressure is determined by reading manometer B. 13 A more specific description of operation of the test fixture is as follows: 14 15 1. Place the module in the slot of the test fixture. 16 2. Turn on power to the fan. 17 18 Select test criteria. It is suggested that the two airflow levels as 19 shown in Table 94 on page 399 for each module size be tested to confirm that the related module airflow resistance falls between the min-20 imum and maximum levels as described in Figure 123 on page 401. 21 For example, for the Standard module, two different measurements 22 would be made for airflow rates of 6 and 9 CFM. 23 4. From the horizontal axis of Figure 193 on page 742, select airflow 24 level that is to be tested. Then determine the related differential pres-25 sure for the airflow level to be tested by reading the related pressure 26 along the vertical axis. 27 Adjust the speed of the fan until manometer A reads the appropriate 28 pressure from step 4. For example, to achieve 6 CFM of airflow, adjust 29 the fan so that Manometer A reads 0.20 inches of water. 30 6. Read the measured pressure from manometer B to determine the 31 related module resistance for that particular airflow rate. 32 7. Plot the airflow and pressure values onto Figure 123 on page 401. 33 If the point falls between the minimum and maximum curves, then the 34 module meets the specification. 35 36 A1.4 SHIELDING EFFECTIVENESS 37 The following paragraphs describe efforts in shielding performance simu-38 lations and modeling for InfiniBand[™] Modules 39 40 In order to meet the InfiniBandTM shielding effectiveness specification 41 shown in Figure 124 on page 404, a number of different hole patterns, 42

sizes and configurations were modeled using the Finite-Difference Time-Domain (FDTD) technique. This technique is particularly effective for this type of problem, since the thickness of the metal can be varied without the need to increase the model size (and hence its run time).

In <u>Figure 194</u>, <u>Figure 195</u>, <u>Figure 196</u>, and <u>Figure 197</u>, the shielding effectiveness of an InfiniBandTM module was modeled for various hole sizes and metal thickness to determine the required sizes to meet the specified shielding standard.

For figures Figure 198 on page 746, Figure 199, Figure 200, Figure 201, and Figure 202, another set of models was created for larger holes (10 x 10 mm), in 1, 2, 4, or 8 hole configurations to determine the effect of connector openings in the InfiniBandTM connector housing. Once again, various metal thickness were used to determine the required metal thickness to meet the specified shielding standard.

For all of the above simulations a wire source was placed 20 mm from the inside of the shield with holes, in order to represent a worst case situation of an EMI source close to the holes.











Figure 200 Shielding Performance: 10 x 10, Qty-2



2.0E+10

Frequency (Hz)

2.5E+10

3.0E+10

3.5E+10

4.0E+10

1.5E+10

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0

5.0E+09

1.0E+10

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# A1.5 CARRIER ATTENUATION TEST PROCEDURE (NORMATIVE)

#### A1.5.1 INTRODUCTION

This section is normative. InfiniBand[™] specifies very aggressive require-3 ments for module carrier attenuation. With cooling vents included in the 4 module carrier, the module itself becomes a strategic portion of a chassis' 5 emi containment. Figure 124 on page 404 is the specified attenuation 6 curve required for all module carriers. In order to verify these attenuation 7 levels, an attenuation reference chassis has been developed. Details for 8 this test vessel are included in Annex A1.6 on page 754. The intent of this 9 procedure is to test the attenuation of the mechanics of the module carrier and not specifically the module's potential emissions. Each carrier must 10 not only shield its own module emissions, but it also must attenuate po-11 tential emissions generated elsewhere in a real system. For these rea-12 sons, this test is set up to be run with non-operational module (or empty 13 carrier) and a battery powered noise source capable of producing EMI 14 spanning the band from 100 MHz to 12.5 GHz. 15



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For the purpose of this procedure the shielding effectiveness of the module shall be defined as the ratio of two values:

- Numerator: EMI measured with the noise source unobstructed (out in the open)
- Denominator: EMI measured with the noise source in the reference chassis and the module under test in place.

**CA1-0.1.1:** The shielding effectiveness **shall** be measured for both horizontal and vertical antenna polarities, at a source and antenna height of one meter, and a source to antenna distance of 2m. 9

**CA1-0.1.2:** The EMI measurements **shall** be made with the spectrum analyzer in maximum hold mode, while the unit under test is rotated through a 180 degree rotation. The test should be performed within a semi-anechoic chamber and **shall** be conducted over a ground plane.

### A1.5.2 EQUIPMENT REQUIRED

		4.0
•	Semi-Anechoic Chamber with turntable	18
•	HP 8566B Spectrum Analyzer or equivalent (measurement capability up to 12.5 GHz)	19 20
•	EMCO 3148 Log Periodic Antenna or equivalent (measurement ca- pability from.1 to 1 GHz)	22
•	EMCO 3115 Horn Antenna or equivalent (measurement capability of 1 to12.5 GHz)	24
•	Miteq NSP1800-N Preamplifier or equivalent (30 dB preamp, mea- surement capability.1 to 12.5 GHz)	26 27
•	EMI Reference Chassis	28
•	Battery Powered Noise Source(s) (EMI source for.1 to 12.5 GHz)	29 30 31
A1.5.3 MEASUREMENT PROCEDUR	RE: 100 MHz - 1.1 GHz	32
		33

1. Place the low frequency noise source on a wooden table 1m above the ground-plane of the turntable, set its antenna for vertical polarity.

2. Position the Log Periodic Antenna 2m away from the noise source, set its height to 1m, and rotate it for vertical polarization. 37

3. Connect the Preamplifier and Spectrum Analyzer to the Log Periodic39Antenna. Set up the spectrum analyzer as follows:40

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yz	zer Settings, 100 MHz - 1.1	GHz	2
	Reference Level		3 4
	Log Scale		5
	RF attenuation		6
	Video & IF(Resolution)BW		7
	Start Frequency		0 9
	Stop Frequency		10
	Display Mode		11
			12
			13 14
			15
			16
ha	annel A of the Spectrum Analy	zer from	17
			18
	degrade offer retation is some		20
) ) (	view. Set the display mode for	channel	21
а	r/write.		22
fre	ont adapter plate as appropria	to to the	23
a	s shown in <u>Figure 203 on page</u>	<u>e 10 ine</u> <u>e 749</u> .	24
			23
i S Si	rear compartment of the reference s vertically polarized, and seal	ence it inside	27
si	S.		28
:	ation to be tested into the ID.	ah a a a i a	29
)		Chassis	30
			32
ch	annel B of the Spectrum Analy	zer from	33
			34
8	0 degrees, making sure that E	MI from	35
a er	cross the entire front of the IB rotation is complete, set the c	lisplay	37
			38
~	ubtroat troac b from troac - th	- <b>r</b> o	39
s e	ffectiveness of the module and	d must	40
e	ness specified in Figure 124 o	<u>n page</u>	41 42
			+2

# Table 173 Spectrum Analy

4. Turn on the noise source.

50dBuV 10 dB/div 0dB 300 KHz 100 MHz 1100 MHz Channel A - Trace Clear/Write

5. Change the display mode for cl Clear/Write to Maximum Hold.

6. Rotate the turntable through 18 the display mode for channel A to B of the spectrum analyzer to cle

7. Connect the standard or wide f front of the reference-IB chassis

8. Insert the noise source into the chassis, making sure its antenna using the rear cover for the chass

9. Insert the module/carrier comb slot.

10. Change the display mode for c Clear/Write to Maximum Hold.

11. Rotate the turntable through 1 that module has been measured chassis/module combination. After mode for channel B to view.

12. Set the spectrum analyzer to sulting trace will be the shielding comply with the shielding effective

<u>404</u> of the specification. Print the results and maintain as a record to show compliance with the specification.

13. Take the noise source out of the reference chassis, and remove the3reference chassis from the wooden table.4

14. Set the noise on the table such that its antenna is in the horizontal polarity. 7

15. Rotate the Log Periodic antenna into the horizontal Polarity, and repeat steps 3 through 12, insuring that the antenna of the noise source is in the horizontal polarity when it is inserted into the reference chassis.

## A1.5.4 MEASUREMENT PROCEDURE: 1 GHz - 12.5 GHz

1. Place the high frequency noise source on a wooden table 1m above the ground-plane of the turntable, set its antenna for vertical polarity.

2. Position the Horn Antenna 2m away from the noise source, set its height to 1m, and rotate it for vertical polarization.

3. Connect the Preamplifier and Spectrum Analyzer to the Horn Antenna. Set up the spectrum analyzer as follows:

50dBuV	Reference Level
10 dB/div	Log Scale
0dB	RF attenuation
300 KHz	Video & IF(Resolution)BW
1.00 GHz	Start Frequency
12.50 GHz	Stop Frequency
Channel A - Trace Clear/Write	Display Mode

	Fable 174	Spectrum Anal	yzer Settings, 1	GHz - 12.5 GHz
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4. Turn on the noise source.

5. Change the display mode for channel A of the Spectrum Analyzer from Clear/Write to Maximum Hold.

	6. Rotate the turntable through 180 degrees, after rotation is complete set the display mode for channel A to view. Set the display mode for channel B of the spectrum analyzer to clear/write.	1 2 3
	7. Connect the standard or wide front adapter plate as appropriate to the front of the reference chassis as shown in Figure 203 on page 749.	4 5
	8. Insert the noise source into the rear compartment of the reference chassis, making sure its antenna is vertically polarized.	6 7 8
	9. Insert the module/carrier combination to be tested into the IB chassis slot.	9 10
	10. Change the display mode for channel B of the Spectrum Analyzer from Clear/Write to Maximum Hold.	11 12 13
	11. Rotate the turntable through 180 degrees, making sure that EMI from that module has been measured across the entire front of the IB chassis/module combination. After rotation is complete, set the display mode for channel B to view.	14 15 16 17
	12. Set the spectrum analyzer to subtract trace b from trace a, the re- sulting trace will be the shielding effectiveness of the module and must comply with the shielding effectiveness specified in Figure 124 on page 404 of the specification. Print the results and maintain as a record to show compliance with the specification.	18 19 20 21 22
	13. Take the noise source out of the reference chassis, and remove the reference chassis from the wooden table.	23 24 25
	14. Set the noise on the table such that its antenna is in the horizontal po- larity.	26 27 28
	15. Rotate the Horn antenna into the horizontal polarity, and repeat steps 3 through 12, insuring that the antenna of the noise source is in the horizontal polarity when it is inserted into the reference chassis.	29 30 31
A1.5.5 TEST COMPLETION		32
	<b>CA1-0.1.3:</b> After this procedure has been completed, four charts showing the shielding effectiveness of the module will have been generated. These charts fully document the shielding effectiveness of the module over the frequency range of 100 MHz-12.5 GHz for both horizontal and vertically polarized noise sources and <b>shall</b> meet or exceed the shielding effectiveness specified in Figure 124 of the specification. These charts <b>shall</b> be maintained as records to show that the module is in compliance with the IB mechanical specification.	34 35 36 37 38 39 40

## A1.6 FABRICATION AND ASSEMBLY OF THE EMI REFERENCE CHASSIS

#### A1.6.1 INTRODUCTION

Two reference chassis are detailed in this annex. The Standard Height	3
Reference Chassis will support testing of Standard or Wide modules using	4
a separate front cover assembly to adapt to standard or wide. The Tall	5
Height Reference Chassis will support testing of Tall or Tall Wide modules.	6

Detailed fab parts are shown in the following figures. Some of the fab parts are parametrically represented where a parts dimensions deviate for standard versus wide or standard versus tall. In each of these cases, the stan-dard size dimension is represented first followed by the tall (T) or wide (W) dimension in parentheses. 

The chassis consists of a welded enclosure open in the rear and partially open in the front. The chassis is specified with internal removable module guides and specifically located EMI gasketing. The rear of the chassis is void for placement of the signal generator which can be accessed through the removable rear panel (see Figure 204 on page 756). 

## A1.6.2 PARTS LIST

Table 175 is a detailed parts list for each size of EMI reference chassis.

Standard Height Reference Chassis		Tall Heig	th Reference Chassis
QTY	Assy, Fab, or Purchase Part	QTY	Assy, Fab, or Purchase Part
1	Chassis Weldment, Standard	1	Chassis Weldment, Tall
1	Housing, Standard	1	Housing, Tall
1	Front, Standard	1	Front, Tall
1	Base	1	Base
2	Guide	2	Guide
1	Rear Cover Assy, Standard	1	Rear Cover Assy, Tall
1	Rear Cover, Standard	1	Rear Cover, Tall
8	SouthCo 84-20-080-30	8	SouthCo 84-20-080-30
*	EMI Gaskets Cut to Length *	*	EMI Gaskets Cut to Length *
1	Front Cover Assy, Standard	1	Front Cover Assy, Tall
1	Front Cover, Standard	1	Front Cover, Tall
4	SouthCo 84-20-080-30	4	SouthCo 84-20-080-30

# Table 175 Detailed Parts List for Standard and Tall EMI Reference Chassis

Table 175	<b>Detailed Parts</b>	List for	Standard and	Tall EMI	<b>Reference Chassis</b>
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Standard Height Reference Chassis		Tall Height Reference Chassis	
QTY	Assy, Fab, or Purchase Part	QTY	Assy, Fab, or Purchase Part
*	EMI Gaskets Cut to Length *	*	EMI Gaskets Cut to Length *
1	Front Cover Assy, Wide	1	Front Cover Assy, Tall/Wide
1	Front Cover, Wide	1	Front Cover, Tall/Wide
4	SouthCo 84-20-080-30	4	SouthCo 84-20-080-30
*	EMI Gaskets Cut to Length *	*	EMI Gaskets Cut to Length *
3	* EMI Gasket (15" length) Instru- ment Specialties 0097-0910-15	3	* EMI Gasket (15" length) Instru- ment Specialties 0097-0910-15
1	Quarter Turn Application Tool- SouthCo 82-0-14719-11	1	Quarter Turn Application Tool- SouthCo 82-0-14719-11
1	Signal Generator, TBD	1	Signal Generator, TBD

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#### A1.6.3 ASSEMBLY/FABRICATION DRAWINGS












InfiniBand TM Architecture Release 1.2 VOLUME 2 - PHYSICAL SPECIFICATIONS	October, 2004 FINAL
ENI GASKET. CUT TO LENGTH. AFPLY WITHIN SCRIBE MARKS IS 0097-0910-15	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35
Figure 210 Rear Cover Assembly - Standard; Tall	30 37 38 39 40 41
	42



nfiniBand TM Architecture Release 1.2 √OLUME 2 - PHYSICAL SPECIFICATIONS	October, 2004 FINAL
FRONT COVER, STANDARD (FRONT COVER, WIDE) (FRONT COVER, TALL) (FRONT COVER, TALL/WIDE)	
EMI GASKET, CUT TO LENGTH, APPLY WITHIN SCRIBE MARKS IS 0097-0910-15	
QUARTER TURN, 4PL SOUTHCO 84-20-080-30	
Figure 212 Front Cover Assembly - Standard; Wide; Tal	I; Tall/Wide



DLUME 2 - PHYSICAL SPECIFICATIONS	Final

InfiniBandTM Architecture Release 1.2

# ANNEX A2: IB-ML DESIGN GUIDELINES

#### **A2.1 INTRODUCTION**

The purpose of this annex is to aid in the design of the InfiniBand Management Link (IB-ML) using SMBus and/or I²C agents. This annex covers design considerations of the SMBus and I²C bus and also highlights the protocol, electrical, and timing differences between the SMBus and I²C bus. Calculation of proper bus signal pullup resistor values is also covered. It is assumed that the reader is familiar with the concepts of the IB-ML, SMBus and I²C bus.

#### A2.2 PROTOCOL

This section shows the protocol differences between the IB-ML, SMBus and the I²C bus. The InfiniBand Management Link timing and multimaster arbitration protocol is based on the SMBus 1.1 specification[24]. It is recommended that interfaces be designed to also meet the I²C timing specifications.

Although highly recommended, devices are not restricted to using the SMBus protocols. Devices must use protocols that use simple write-read transactions supported by the IB-to-IBML command. Devices are recommended to implement PEC (Packet Error Code) on their interfaces to help ensure data integrity.

One should consider the protocol and specific addresses supported by all agents on the bus to ensure proper bus operation. For a complete list and explanation of protocols supported by each type of bus, refer to <u>Chapter</u> <u>13: Hardware Management</u>, the I²C bus and the SMBus specifications. The I²C Bus specification is available from Phillips Semiconductors [25]. Copies of the SMBus Specification Revision 1.1 are available from Intel Corporation and the Smart Battery Systems Implementers Forum [24].

# A2.2.1 SMBUS AND I²C BUS PROTOCOL DIFFERENCES

The following protocol differences exist between the SMBus and the I²C bus:

 The SMBus specifies device time-outs which can be used to signal a device error condition or that a device is not ready. Device time-out is accomplished by holding either SMBCLK or SMBDATA low for longer than TTIMEOUT. It is recommended that devices automatically drop off the bus whenever TTIMEOUT is exceeded.

2	he SMBus allows a slave device to stretch the cumulative clock low me, in a single message, up to T _{LOW:SEXT} .	1
3	he SMBus allows a master device to stretch the commutative clock ow time, in any single byte, up to T _{LOW:MEXT} .	2 3 4
2	he SMBus can specify the protocol an SMBus agent is allowed to se when acting as a slave when communicating with an SMBus ost.	5 6 7
Ę	he $I^2C$ bus protocol doesn't include the Quick Command, but it is alid and will not cause an error from $I^2C$ devices. The Quick command will look to $I^2C$ devices as a command abort by the bus naster.	8 9 10 11
6	C does not specify a fixed host device address as does the SMBus	. 12
7	he SMBus reserves the same bus protocol addresses as the I ² C us, as well as additional SMBus-specific reserved addresses.	13 14
٤	MBus timing specifies that a master must hold data for 300 ns fol- owing the falling edge of clock, whereas I2C specifies a 0 ns data old time. As a result, some SMBus slave devices may not work cor- ectly if presented with the I ² C timing from a master. However, if a naster implements SMBus timing for driving the bus, both I2C and MBus slaves should work. Conversely, if a slave can work with I2C ming, it should work with both I ² C and SMBus master. Thus, it is ecommended that devices provide the SMBus 300 ns data hold time then driving the bus as a master, and accept the 0 ns I ² C hold time then receiving data as a slave.	15 16 17 18 19 20 21 22 23
٦	SMBus exclusive reserved protocol addresses are listed in Table 176	· 25

Address	SMBus Function
0001 000	SMBus Host (devices on IB-ML should avoid this address unless they implement SMBus Host functionality.)
0001 100	SMBus Alert Response (devices on IB-ML that use this address must do so per the SMBus specification)
1100 001	SMBus Device Default (devices on IB-ML that use this address must do so per the SMBus 2.0 specification)
0101 000	Reserved for ACCESS.BUS (allowed for device use on IB-ML)
0110 111	Reserved for ACCESS.BUS default (allowed for device use on IB-ML)
1001 0xx	Unrestricted Address (allowed for device use on IB-ML)

# Table 176 SMBus Reserved Addresses

Besides the addresses listed as reserved by the SMBus, Table 177 provides a list of command addresses reserved for protocol use by both the

SMBus and the I²C bus. <u>Table 177</u> provides a list of addresses used by some motherboards.

Slave Address	Read/Write # Bit	SMBus and I ² C Bus Function		
0000 000	000 0 General call address			
0000 000	1	START byte ^a		
0000 001	Х	CBUS address ^b		
0000 010	Х	Address reserved for different bus forma		
0000 011	Х	Reserved		
0000 1xX	Х	Reserved		
1111 0XX	Х	10-bit slave addressing ^d		
1111 1xX	Х	Reserved		

#### Table 177 SMBus and I²C Bus Reserved Addresses

a. No device is allowed to acknowledge at the reception of the START byte.

b. The CBUS address has been reserved to enable the inter-mixing of CBUS compatible and I²Cbus compatible devices in the same system. I²C-bus compatible devices are not allowed to respond on reception of this address.

c. The address reserved for a different bus format is included to enable I²C and other protocols to be mixed. Only I²C-bus compatible devices that can work with such formats and protocols are allowed to respond to this address.

d. Support for 10-bit slave addressing is not specified nor required for IB-ML.

# Table 178 Commonly Used Motherboard Addresses

lave Address	Read/Write # Bit	SMBus and I ² C Bus Function
1010 XXX	Х	Common 24C02-style SEEPROM address range. Also used for DIMM module SEEPROMs.
1001 110	Х	I ² C Mux address
1101 001	Х	Clock generator address
0101 101	Х	LM-78/ADM1024-style Monitoring ASIC addresses.

Table 179 on page 770 lists the recommended ranges of addresses us-35able by an InfiniBandTM module. This list is an extension of the list given36in the Chapter 13: Hardware Management. Modules that are embedded37in a chassis can use other addresses at the discretion of the system de-38signer. Note that functional addresses for elements such as the Mod-39uleInfo, ChassisInfo, MME Function registers, and MME IB2IBML40registers should not be claimed even for an embedded module. In particular, the ModuleInfo address must be preserved, since software uses that41

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address as the root for discovering Module and Chassis capabilities via the IB-to-IBML Baseboard Management command functionality.

#### Implementation Note

**IMPORTANT** - Check your bus device addresses carefully.

All SMBus addresses (other than those listed in <u>Table 176</u> and <u>Table</u> <u>177</u>) are stated as being reserved for assignment by the SMBus address coordination committee of the Smart Battery Systems Implementer's Forum (SBS-IF). This is generally only applied to specifying addresses for certain devices that have standardized functional interfaces specified by the SBS-IF, such as battery charger ICs and battery monitors. It is common for device manufacturers to utilize these addresses without coordination with the SBS-IF, particularly on busses where the SMBus functionally addressed devices are not likely to be used, such as on the IB-ML between an InfiniBandTM chassis and InfiniBandTM module.

Philips Semiconductor (the I²C address assignment agency) has created many addresses other than the common SMBus and I²C protocol addresses for use by their specific devices. Designers may want to consult Philips and other vendor catalogs when choosing addresses in case there are components from those vendors the designer may want to use in the future.

Pay close attention to the specific addresses of the bus agents to avoid address conflicts. This especially applies when mixing SMBus devices and  $I^2C$  bus devices on the same physical bus.

Slave Address	8-bit Hex notation	Function			
0100 000 - 0100 011	40h-46h	Module-specific use. Typically used for 8574-8-bit and 8575-type 16-bit I ² C latches.			
0101 001 - 0101 111	50h-5Eh	Module-specific use. LM78/ADM1024 and other 'Hec- eta' -type monitoring devices.			
1001 000 - 1001 111	90h-9Eh	Module-specific use. Typically used for LM75-style temperature sensors.			
1010 000	A0h	ModuleInfo / Module VPD			

# Table 179 Allowed Addresses for InfiniBandTM Modules

Slave Address	8-bit Hex notation	Function
1010 011	A6h	Module-specific use. Typically used for additional SEEPROMs.
1010 110	ACh	Module-specific use. Typically used for additional SEEPROMs.
1010 111	AEh	Module-specific use. Typically used for additional SEEPROMs.
1011 110 - 1011 111	BCh-BEh	Module-specific use.
1100 001	C2h	SMBus Device Default. Module Devices that use this address must do so per the SMBus 2.0 specification, and not use assigned addresses that conflict with the InfiniBand specification.
1101 110 - 1101 111	DCh-DEh	Module-specific use.
1110 000	E0h	MME Function registers
1110 001	E2h	MME IBML2IB registers
1110 100	E4h	MME Command
1110 011	E6h	Module-specific use. Often used for PCA9544-style I ² C bus multiplexer.

# Table 179 Allowed Addresses for InfiniBandTM Modules

#### A2.2.2 IB-ML PROTOCOL DIFFERENCES

The IB-ML supports the SMBus protocol. The differences from I²C are the same as above. Specific addresses reserved for IB-ML devices and the Baseboard Management Agent are located in <u>Table 121 Module IB-ML</u> <u>Slave Addresses on page 496</u> and <u>Table 130 Chassis IB-ML Slave Addresses on page 546</u>.

#### **A2.3 ARCHITECTURAL DIFFERENCES**

This section describes the architectural protocol differences between the IB-ML, SMBus and the  $I^{2}C$  bus.

# A2.3.1 SMBUS AND I²C BUS ARCHITECTURAL DIFFERENCES

The architectural differences between the SMBus and the I²C bus are:

 The SMBus may have an optional SMBUS# signal used in powerdown mode. This signal is an output from the system management device and is used to signal the state of system suspend mode.

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	2)	The SMBus may have an optional SMBALERT# signal used for a slave-only device to signal the bus master that it wishes to communicate.
	3)	Response to the SMBALERT# signal generates a 7 or 10-bit alert re- sponse using the defined alert response address.
A2.3.2 IB-ML ARCHITECTURAL	. Di	FFERENCES
	Th	e architectural differences between the IB-ML and the SMBus/I ² C bus

- 1) The IB-ML does not support the SMBus and I²C bus sideband signals described above.
- 2) The IB-ML is a point to point link between an IB Module and a Chassis. This eliminates address conflict issues between Modules, but support for multi-master arbitration is still required. This is because a CME and module can both attempt to initiate a transaction at the same time. CMEs, MMEs, and any other master on IB-ML must support multi-master arbitration.
- IB-ML has its own electrical drive specifications. Refer to <u>Table 180:</u> <u>Electrical Differences (IB-ML, SMBus and I2C Bus)</u>.

#### A2.4 ELECTRICAL AND TIMING

This section describes the IB-ML, SMBus and I²C electrical and timing differences. Since the IB-ML, SMBus and I²C bus are open-collector technologies, calculating the proper signal pullup resistor values will also be covered.

# A2.4.1 IB-ML, SMBUS AND I²C BUS ELECTRICAL DIFFERENCES

are:

The main difference between the IB-ML, SMBus and I²C Bus electrical characteristics is that the IB-ML/SMBus uses fixed levels and the I²C bus uses levels relative to the Vcc of the bus device. In addition, IB-ML specifies greater drive than the SMBus 1.1 specification does. <u>Table 180</u> lists the electrical differences between the IB-ML, SMBus and the I²C bus.

Parameter		IB-ML		5	SMBus		SMBus		I ² C Bus
	Min.	Max.	Min.	Max.	Min.	Max.			
Vil	-0.5V	0.8V	-0.5V	0.6V	-0.5V	0.3*Vcc			
Vih	2.1V	3.63V	1.4V	5.5V	0.7*Vcc				
Vol		0.4V @ 4.0mA		0.4V @Ipullup Min.	0	0.4V @ 3.0mA (0.6V @ 6.0mA fast)			
lil		+/- 10µA		+/- 10µA		+/- 10µA			
lpullup		4.0mA ^a	100µA ^a	350µA ^a		3.0mA (6.0mA fast)			

# Table 180 Electrical Differences (IB-ML, SMBus and I²C Bus)

a. The value includes both the current through the pullup resistor and current from all bus agents. In this context the parameter lpullup is equivalent to lol.

The value for Ipullup listed in the SMBus specification has been shown to be difficult to meet when larger numbers of agents are connected to the bus. For this reason, some SMBus devices may differ from the Ipullup parameter listed in <u>Table 180</u>. For example a Ipullup of 3.0mA Max will guarantee a Vol of 0.4V @ Ipullup of 3.0mA. This allows a larger number of devices to be connected to the bus without violating the operating levels.

# A2.4.2 BUS AND AGENT VCC VOLTAGE LEVELS

The I²C bus specifies that device input levels are in most cases dependent on Vcc. Note the voltage to which Vcc of each I²C bus agent is connected and to what voltage the bus signal pullup resistors are connected. Mixing these voltages in the wrong way could cause improper input high levels.

The IB Modules auxiliary voltage is used as the supply for the termination of the IB-ML. A module may use a local 3.3V regulator from **VA_In** for the termination supply or use the VA_In supply with a resistive divider termination.

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In some cases, bus agents may only have 3.3V tolerant input levels and therefore the bus signals must only be pulled up to a Vcc of 3.3V. Any other bus agents will have to be connected to the proper voltage levels so that their input levels are compliant with that of the bus. For a reference implementation to provide the necessary translation see Section A2.4.7.

# A2.4.3 IB-ML, SMBUS AND I²C TIMING DIFFERENCES

19 The IB-ML/SMBus and I²C Bus timing differences are mostly concerned with time-out and clock stretching protocols supported by the IB-20 ML/SMBus. These timing differences are listed in Table 181. Note, the de-21

Desembles	IB-ML		SMBus		I ² C Bus	
Farameter	Min.	Max.	Min.	Max.	Min.	Max.
Bus Frequency	10 KHz	100KHz	10 KHz	100KHz	0	100KHz (400KHz Fast)
Clock Low Time-out	25mS	35mS	25mS	35mS	N/A	N/A
Clock High period (ТніGн)	4 us	50 uS	4 us	50 uS ^a	4 us	-
Clock Low Extend (Slave)		25mS		25mS	N/A	N/A
Clock Low Extend (Master)		10mS		10mS	N/A	N/A

a. This parameter provides a simple guaranteed method for masters to detect bus idle conditions. A master can assume that the bus is free if it detects that the clock and data signals have been high for greater than THIGH, MAX.

> signer should still review the actual specifications to get a full comparison of the different bus timings.

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A2.4.4 ARBITRATION RETRIES	S
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If software requests an IB-to-IBML operation, an MME can return an error completion status if it tries to arbitrate for the IB-ML and fails. Software would then need to retry the operation by sending another IB-to-IBML command. It is recommended that a IB-ML master implementation (MME or CME) automatically retry arbitrating for the bus at the next bus-free opportunity at least three times and no more than ten times.

#### A2.4.5 ARBITRATION DELAY

IB-ML, SMBus, and I²C arbitration share the characteristic that the master that transmits the first 0' bit in its message will win arbitration. This means that devices with slave addresses with zeros in lower positions will always win arbitration over devices that have zeros in higher positions. For example, a transaction from the CME to the MME Function registers (1110 1300) will always win arbitration over a simultaneous transaction from the MME to the CME (1110 100).

16 In general, delays and randomness in timing between implementations, 17 and the unlikelihood of arbitration collisions usually prevent one device 18 from locking out another. However, automated back-to-back transfers could cause one device to lock another off the bus until the transfers are 19 completed. It is recommended that devices limit the number of back-to-20 back transactions to three, and then institute a delay of at least 100 us (a 21 little over 1 byte interval) before again trying to arbitrate for the bus. A 22 random factor in the delay interval will further help avoid the potential for 23 'lock out' occurrences. Devices that solely drive transactions in response 24 to a software request (e.g. the MME's IBML-to-IB functionality) generally 25 do not need to implement such limits in hardware, since system software can institute appropriate delays if necessary. 26

#### A2.4.6 BUS PULLUP RESISTOR CALCULATIONS

29 Due to the architecture of both the IB-ML, SMBus and the I²C Bus, all 30 agents on the bus must have open collector (drain) outputs. Because of the nature of these outputs, both the bus clock and data lines must be 31 pulled up to some Vcc value. Both the SMBus and the I²C bus specifica-32 tions require only one pullup resistor per bus signal. The IB-ML specifica-33 tion require two pullup resistors one on the IB Module and one on the 34 chassis. As discussed in Section A2.4.2, the voltage used for the pullup 35 resistors on the bus signals depends on the nature of all of the bus agents. 36

#### A2.4.6.1 GENERAL BUS PULLUP RESISTOR CALCULATIONS

There are three cases that must be considered when calculating the pullup resistor values for either an SMBus or I²C Bus:

• Vih level at rated current.

			-
		Vil level at rated current.	1
		Rise and fall time conditions.	2
	Us	e the above three cases when calculating the bus pullup values. The	3
	DC	C values of Vih and Vil will be used to define a solution space and the rise	4
	an	d fall time requirements will select a specific value in that solution	5
	sp	ace. We recommend this approach to provide a direct method of re-	6
	515		7
	Th	e steps to calculate the solution space are listed in the "Determine Max-	8
	im	um Pullup Resistor Value" and "Determine Minimum Pullup Resistor	9
	Va	lue" procedures in the following sections.	10
			11
A2.4.6.1.1 PROCEDURE 1. DETERMIN	IE M	AXIMUM PULLUP RESISTOR VALUE	12
	То	find the maximum pullup resistor value to use on clock and data lines,	13
	fol	low these steps:	14
	1)	Identify the minimum value of the Veerail (Veemin) where the bus	15
	1)	signal pullup resistors will be connected.	16
	2)	Identify the minimum Vib value for each bus agent when newered by	10
	2)	the minimum Vcc value found in step 1. Use the highest of these Vih	10
		values ( <i>Vihmm</i> ) for the calculations. Choosing the highest minimum	20
		Vih value will guarantee all other Vih conditions are met.	21
	3)	Choose a desired noise margin (NMmin) for the logic high condition	22
		on the bus. This value is typically 0.1V - 0.2V above the maximum	23
		value chosen for <i>Vih</i> . It. is recommended that the first choice for the	24
		noise margin be 0.2V. This will be the minimum noise margin for the	25
		to typical and maximum value, the noise margin will also increase.	26
	4)	Find the total maximum current <i>(libmax</i> ) sunk by all agents for the	27
	ד)	input high condition.	28
	5)	Calculate the maximum value (Romax) for the bus pullup resistor from	29
	0)	the following equation:	30
		Romax - (Vccmin - (Vibmm + NMmin))/ libmax - Equation 1	31
	$\sim$	This result is the upper limit (meximum value) of the pullup resistor	32
	6)	solution space	33
		solution space.	34
A2.4.6.1.2 PROCEDURE 2. DETERMIN	IE M	INIMUM PULLUP RESISTOR VALUE	35
	То	find the minimum pullup resistor value to use on clock and data lines,	30
	fol	ow these steps:	38
	<b>^</b> `		39
	1)	Identity the maximum value of the Vcc rail (Vccmax) where the bus	40
	~		41
	2)	Identify the lowest Vol value (Volmin) for all bus agents.	42

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	3) Identify the maximum current sunk ( <i>lolmax</i> ) by this bus agent at the <i>Volmax</i> value.	<b>)</b> 1
	<ol> <li>Calculate the minimum value (<i>Rpmin</i>) for the bus pullup resistor fro the following equation:</li> </ol>	m 3
	Rpmin = (Vccmax - Volmin) / Iolmax - Equation 2	Ę
	5) This result is the lower limit (minimum value) of the pullup resistor s lution space.	<b>30-</b> 67
	Now we have a minimum and maximum resistance value that our pulle resistor can be while satisfying the DC specifications of our bus. This i our solution space for choosing a resistor value that will satisfy our rise and fall times.	up 8 s 9 e 1
		1
A2.4.6.1.3 PROCEDURE 3. PERFORM	BUS SIGNAL RISE AND FALL TIME CALCULATIONS	1
	The value found from the rise and fall time calculations, together with the solution space defined from the bus DC bus values, will determine the proper value for the bus pullup resistors. The solution from the rise and fall time calculations should fall within the DC solution space to satisfy bus requirements.	ne 1 1 d 1 all 1
	If a value of pullup resistor is found that satisfies our rise and fall time quirements but is not in our DC solution space, parameters in the calcu- tions or the bus design itself may need to be modified.	re- 1 1a- 2
	A good rule of thumb for the pullup value is $Rp < Trise / 2 * Cbus$ . Where <i>Trise</i> is the maximum allowable rise time minus some margin and <i>Cbus</i> the total capacitance on the bus.	is 2
	In this design guideline, a more precise calculation will be used to calculate the pullup resistor values. This calculation will also help verify the ru of thumb calculation. The equation that will be used to calculate signal ritime is one for charging capacitors.	u- 2 ile 2 se 2
	The general form of this equation is:	3
		3
	$Vc = Vcc + [Vo - Vcc] e^{-VRC}$ - Equation 3	3 2
	where $R$ is pullup Rp, $C$ is the total bus capacitance, $t$ is the rise time, is the initial voltage on the bus capacitance, and $Vc$ is the voltage across the bus capacitance at any given time (in this case Vil and Vih values).	Vo SS 3
	Solving Equation 3 for the rise time t yields:	3
		3
	t = -RCIn[(VC - VCC)/(VO - VCC)] - Equation 4	3
A2.4.6.2 RISE TIME CALCULA	TION	4
	Use the following steps to calculate the bus rise time:	4
		2

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	1)	The maximum rise time for both the SMBus and the $I^2C$ Bus is defined to be 1.0 $\mu s.$	
	2)	Choose a rise time margin such that the desired rise time is less than the maximum allowed rise time of $1.0\mu s$ . Usually this is around 50 - 100nS.	
	3)	Calculate the total capacitance of the bus. This includes the capaci- tance of the bus and of all bus agents.	
	4)	For a rising edge, 0 to 1 transition, assume an initial starting voltage ( <i>Vo</i> ) for the logic 0 state. Assuming the bus has settled out to a ground state, this value would be approximately 0V. For worst case bus calculations, assume an initial voltage of 0V.	
	5)	Determine the minimum value of <i>Vcc (Vccmin</i> ) in the system where the pullup resistor will be connected.	
	6)	Determine the maximum value for <i>Vih (Vihmm</i> ) for the minimum value of <i>Vcc</i> found in step 5.	

7) Solve Equation 5 for the pullup resistor R and substitute the known values for the bus parameters. This will yield an equation for the value of the pullup resistor needed.

#### Rp = -t / (C * ln [(Vihmm - Vccmin)/ (Vo - Vccmin)]) - Equation 5

21 If the value obtained from Equation 5 is not in the solution space found in the "General Bus Pullup Resistor Calculations" of Section A2.4.6.1 for the 22 DC levels, one of two steps must be taken. If the value from the above rise 23 time equation is greater than the maximum limit of the DC solution space 24 found in Equation 4, the resistor value may be reduced to a value within 25 the solution space. 26

27 Lowering the resistor value will satisfy the DC solution space and will not 28 violate the rise time specification. A lower resistance value than the one found in Equation 5 will not violate the maximum rise time parameter but 29 will in fact make the rise time less. This can be seen from Equation 4. As-30 suming no parameters change except for the resistance R, a lower resis-31 tance value will yield a lower rise time t. 32

If the result of Equation 5 is lower than the minimum value for the DC solution space found in Equation 2, either the factors influencing the minimum value for the DC solution space must be changed or the factors influencing the value from the rise time calculation must be changed. In the case of the minimum value in the DC solution space, this value must be lowered.

39 From Equation 2 we see that the resistance value may be lowered if the 40 product of Vccmax - Volmin is decreased and/or Iolmax is increased. Since 41 lolmax and Volmin are a function of the bus agent in question, the only so-42

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lution without changing the driving bus agent is to select a lower *Vccmax* of the system.

In the case of the value for maximum rise time, this value must be raised. From Equation 5 we can see that in order to make the value for Rp greater we must increase the desired maximum rise time, decrease the bus capacitance, decrease the *Vihmax – Vccmin* product, and/or increase the *Vo – Vccmin* product.

Generally, the bus capacitance is a function of the bus agents and cannot be changed unless the number of bus agents is changed or the characteristics of the bus agents are changed. The products of *Vihmax* – *Vccmin* and *Vo* – *Vccmin* can be changed appropriately by decreasing the value of *Vo*. The fact that *Vihmax* is a function of *Vccmin* means changing one will change the other so that no net change will occur when the division of the numerator and denominator is performed. The most easily changed parameter is the desired rise time. If some margin has been added to the rise time, the amount of margin can be decreased so that the desired maximum rise time will increase.

The above cases are listed for completeness. In general, the resistor from the rise time calculation will either be in the DC solution space or will be greater than the DC solution space. In these cases little or no work will be needed to adjust for a resistor value that is acceptable for proper bus operation.

# A2.4.6.3 FALL TIME CALCULATIONS

The calculations for fall time involve equations that require knowledge of the output driver, as well as several integrations over the active regions of the output driver. These calculations are beyond the scope of this document and need not be used here.

Instead, we can use the fact that the SMBus and  $I^2C$  Bus specifications require a maximum fall time of 300ns. We can also use the fact that these same specifications require that the output driver of a compliant agent must guarantee a maximum fall time of 250ns over a bus capacitance of 10 - 400pF with up to 3.0mA (6.0mA in the fast  $I^2C$  case) of sink current.

# Implementation Note

Although the SMBus specifies a maximum fall time of 300ns, it makes no specification of the output driver guaranteed fall time. Only the  $I^2C$ bus specifies the 250ns guaranteed driver fall time, as mentioned above. A2.4.6.4 IB-ML

	From the previous paragraph we can assume our bus fall times to be within the 300ns specification if three criteria are matched:	1 2
	<ul> <li>All agents that are capable of driving the bus are I²C compliant to guarantee falltimes of 250ns maximum.</li> </ul>	3 4
	<ul> <li>Our bus has a total capacitance of between 10 and 400pF.</li> </ul>	5
	<ul> <li>The total current that has to be sunk by any output driver in the low state is 3.0mA or less (6.0ma or less in the fast I²C case).</li> </ul>	6 7
	For the total bus current that has to be sunk by any driver in the low state, you can use this equation:	8 9 10
	I total = $((Vcc-Volmin)/Rp) + Iil$ (from all bus agents) - Equation 6	11
	Note that the maximum pullup resistor current occurs at <i>Volmax</i> and <i>Vc-cmax</i> .	12 13 14
BUS PULLUP	RESISTOR CALCULATIONS	15
	The IB-ML termination target voltage is 3.3V nominal. Implementations may utilize a local 3.3V regulator (e.g. +-5%) from VA_In or may use a resistor divider from VA_In. In order to maintain the 3.63V VihMAX and include consideration of the tolerance of VA_In results in a termination voltage of:	16 17 18 19 20
	VTermMAX: 3.63V (VA_In tolerance of +5%)	21
	VTermMIN: 3.063V (VA In tolerance of -8%)	22
		23
	Figure 215 Thevinen Equivalent Termination	25
	VA_In V_term	26
	Rpu SRhevinen	27
		28
	Rpd	29
		30
		31
		32
	If the IB-ML termination solution is determined for the Thevinen equivalent circuit, it can be implemented as the resistor divider shown above. Fither	33
	solution is valid.	34
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The following is a MathCAD analysis for the IB-ML resistor termination using **VA_In** as the termination voltage.

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	Given:	3
	For the IMxClk, IMxDat and IMxPRst bi-directional signals:	4 5
	1) The chassis and IBML input voltage requirements are:	6
	Vil = $-0.5V$ Min and $0.8V$ Max	7
	Vih = 2.1V Min and 3.63V Max	8
	2) The Vaux specification:	9
	$VA_{III} = 5.5V$ Max and 4.6V Mill	11
	3) The Module IBML capacitance is 200pF Max	12
	4) The Chassis IBML capacitance is 100pF Max	13
	5) The Module leakage current is 80uA	14
	6) The Chassis leakage is 400A	15
		16
		1/
		19
Require	ment:	20
		21
1) The	Real must provide valid Vin/Vil levels and AC timing under all the following conditio	22
2) The	VA_In range	23
4) The	e capacitance range	24
Three co	onfigurations are to be studied:	26
1) The	IB Module alone	27
2) The 3) The	B Module and chassis together	28
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		38
		Δr
		10



VA_In V_term T I	1) Vterm nom tar	act is 3.3V	1
Rpu < 🦂 Rthevinen	i) vienn_nom tar	get 13 0.0 V	2
Rod	2) Vterm_max tar VA_In tolera	get is 3.63V which uses the ance of +5%	3 4
		et is 2,020 which uses the	5
	3) vterm_min targ	pet is 3.036 which uses the ance of -8%	6
—			7
			8
			9
Step 1: Determine the Maximum Pullup	Value based on D0	C parameters:	10
			11
Case 1: The chassis alone			12
[Vterm min_ (Vih	min⊢ NM min]		13
$Rpumax_chassis = \frac{[verm_nm_{end}]}{[chassis]}$	max	Rpumax_chassis= $1.84 \times 10^4$	14
101105515	_max		15
Case 2: The module alone			16
			17
Rpumax_module= [Vterm_min-(Vih]	_min+ NM_min)]	Rpumax_module= $9.2 \times 10^3$	18
Imodule	e_max	<b>x</b> —	19
Case 3: The module and chassis to	gether		20
			21
$Rpumax := \frac{[Vterm_min-(V1h_min+N]]}{N}$	M_min)]	$Rpumax = 6.133 \times 10^3$	22
Ileakage_max			23
			24
Stop 2: Determine the Minimum Dullup V		o romotoro.	25
Step 2: Determine the Minimum Pullup Va	alue based on DC	Darameters:	26
Case 1, Case 2, Case 3: Are all the	same		27
			28
$Rpumin:=\frac{(Vterm_max-Vol_min)}{Vterm_max-Vol_min}$	Rpumi	n= 907.5	29
lol_max			21
			22
			32
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Step 3: Determine the Maximum Pullup Value based on the Rise Time requirements:	3
Case 1: The chassis alone	4
	5
$Rpu_chassis = \frac{-T}{\Gamma} \qquad Rpu_chassis = 7.649 \times 10^3$	6
Cchassis $\ln \left( \frac{Vin_min_V \text{term}_min_V}{V_{cl_min_V} V_{comm}} \right)$	7
$\begin{bmatrix} ( (Vol_min-Vterm_min/) \end{bmatrix}$	8
	9
Case 2: The module alone	10
	11
$Rpu_module := \frac{-1}{\left[ -\frac{1}{2} \left( \frac{1}{2} \right)^3 \right]} \qquad Rpu_module = 3.824 \times 10^3$	12
Cmodule $\ln \left( \frac{V \ln \min - V \operatorname{term} \min}{V_{cl} \min - V \operatorname{term} \min} \right)$	13
	14
	15
Case 3: The module and chassis together	10
	10
$Rpu := \frac{-T}{E}$ $Rpu = 2.55 \times 10^{3}$	10
$Ctotal \left( ln \left( \frac{Vih_min-Vterm_min}{Vih_min-Vterm_min} \right) \right)$	20
[ ( ( Vol_min- Vterm_min/ )]	20
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Choosing a nomi	nal terminatior	n value of 907.5 Ohms:	3
This is the minimum pull	up value based on th	ne DC requirements.	4
We will split the Thevine	n equivalent resistor	into pullup/pulldown pairs.	5
Rthevinen:= 907.5			6
Civon			7
Ded	1774 To		8
Vterm_nom= $\frac{\text{Kpd}}{\text{Kpd}}$	Pru - Prd		9
Rnul	Rpd + Rpd		1
Rthevinen= $\frac{Rpu}{Rpu+}$	Rpd		1
			1:
Find(Pnu Pnd)	1375.		1.
$\Gamma \operatorname{Ind}(\operatorname{Kpu}, \operatorname{Kpu}) \rightarrow \left(2669.\right)$	1176470588235294 )		1
Rpu := 1375.	Rpd := 2669	1176470588235294	1
r			1
			1
Splitting the resistors bet	tween the module an	nd the chassis (using the Chassis/IB Mod	1
capacitance ratio) while	maintaining the equiv	valent parallel resistance gives:	2
3		5 · · · · · · · · · · · · · · · · · · ·	2
$\operatorname{Rpu_mod_min} = \operatorname{Rpu}_2$		Rpu_mod_min= $2.063 \times 10^{-10}$	2
Rpu_chas_min= Rpu_mod_	_min2	Rpu_chas_min= $4.125 \times 10^3$	2
			2
3		3	2
$\operatorname{Rpd}_{\operatorname{mod}}_{\operatorname{min}} = \operatorname{Rpd}_{\frac{5}{2}}$		$Rpd_mod_min = 4.004 \times 10^3$	2
Rpd_chas_min:= Rpd_mod_	_min2	Rpd_chas_min= $8.007 \times 10^3$	2
			2
			2
			3
			3
			3
			3
			3
			3
			3
			3
			3
			4
			4
			4

Choosing a nominal terminat	ion value of 2250 Ohms:
his is the maximum pullup value based	on the rise time requirements.
we will split the Thevinen equivalent les	
Rthevinen= 2250	
Civon	
$Vterm_nom=\frac{Rpd \cdot VA_In_nom}{Prm + Prd}$	
Kpu + Kpa	
Rthevinen= $\frac{\text{Rpu-Rpd}}{\text{Rpu} + \text{Rpd}}$	
κρα - κρα	
(3409.090909090909090909	009
Find(Rpu, Rpd) $\rightarrow$ (6617.64705882352941	18)
<b>R</b> _{mu} = 2400 00000000000000000000000000000000	6617 6470599725704119
Kpu := 3409.090909090909090909 Kpu :=	0017.0470388233294118
Splitting the resistors between the modu	ule and the chassis (using the Chassis/IB Mod
capacitance ratio) while maintaining the	equivalent parallel resistance gives:
3	2
$\operatorname{Rpu_mod_max:=} \operatorname{Rpu} \cdot \frac{3}{2}$	Rpu_mod_max= $5.114 \times 10^{3}$
Rpu_chas_max:= Rpu_mod_max2	Rpu_chas_max= $1.023 \times 10^4$
2	
$Rpd_mod_max := Rpd \cdot \frac{3}{2}$	$Rpd_mod_max = 9.926 \times 10^3$
Rpd_chas_max:= Rpd_mod_max2	Rpd_chas_max= $1.985 \times 10^4$

Summary: The following resistor value pairs will meet the DC voltage levels required over the VA_In range as well as the IB-ML AC timing requirements. The resistor selected should include the appropriate tolerances.



# A2.4.6.5 IB-ML PULLUP RESISTOR CALCULATION EXAMPLE

The following is an example of a pullup resistor calculation for the IB-ML using  $I^2C$  slave agents and a single SMBus host.

This example assumes six I²C compliant agents are on the IB Module, ³² one I²C compliant agent and one SMBus master controller on the chassis. ³³

An example SMBus master controller spec:

Vil = 0.6V max.
Vih = 1.4V min.
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- $IiI, Iih = +/- 10\mu A$  39
- Vol = 0.4V max. @ rated lol 40
- lol = 4.0mA max.

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• Ci/o = 12pF max.

#### Implementation Note

The SMBus master controller inputs are assumed to only be 3.3V tolerant so they bus up to a 3.3V supply. In this case Vcc3 is specified at 3.3V + 5% - 8% to reflect the tolerance on VA_In.

I²C compliant bus agents specs.

- Vih = 0.7*Vcc with Vcc = 3.036 3.63V: Vih = 2.12V min., 2.54V max.
- Vil = 0.3*Vcc with Vcc = 3.036 3.63V: Vil = 0.91V min., 1.09V max.
- Iil, Iih =  $+/-10\mu A$
- Vol = 0.4V max. @ rated lol
- Iol = 4.0mA max.
- Ci/o = 10pF max.

#### **Implementation Note**

All of the bus agents have the same specs when they are driving the bus low. This greatly simplifies our calculations since we only need to perform one set of calculations for these common output characteristics.

First we will calculate the pullup resistor solution space from the specified DC parameters for the various agents. In this example we will select a minimum noise margin (*NMmin*) of 0.2V. We see the largest minimum value for *Vih* on any bus agent is 2.1V at minimum *Vcc*. We also note that *lihmax* for the seven agents receiving is  $7*10\mu$ A.

From our equation for maximum pullup resistance:

- Rpmax = (Vccmin (Vihmax + NMmin)) / lihmax
- $Rpmax = (3.036 (2.1 + 0.2)) / 70x10^{-6}$
- Rpmax = 10.514 K

Next we need to calculate the pullup resistor minimum value. The minimum *Vol* value for any agent driving the bus is 0V at an *Iol* of 4.0mA Max. Max. *Vcc* has been determined to be 3.63V. From our equation for *Rpmin*:

- Rpmin = (Vccmax Volmin) / Iolmax 40
- $Rpmin = (3.63 0) / 4x10^{-3}$

• <i>Rpmin</i> = 907.5 K	1
We now have our solution space and may calculate our specific pullup value based on desired rise and fall times.	23
We have a maximum rise time for both the SMBus and $I^2C$ bus of 1.0µs. We now choose a margin for rise time, in this case 100nS. Thus our maximum rise time is 900nS.	4 5 6 7
Note that we now have eight input loads on the bus at any one time during a logic high condition. Seven of these loads are the same, 10pF, and the master controller is 12pF. Thus, we have a total bus capacitance of 82pF.	8 9 10
Voltage conditions are $Vccmax = 3.63V$ , $Vihmax+NM = 2.7V$ , and our assumed worst case Vol is approximately 0V.	12 13
Substituting back into Equation 5 (our Rise Time Calculation), we may now calculate the pullup value based on the above conditions:	14 15 16
<ul> <li>Rp = -t / (C * ln[(Vihmax+NM - Vccmax) / (Vo - Vccmax)])</li> </ul>	17
• $Rp = -900 \times 10^{-9} / (82 \times 10^{-12} * \ln[(2.7 - 3.036) / (0 - 3.036)])$	18
• <i>Rp</i> = 4.986 K	20
We see from our result that the resistor value falls in the pullup resistor solution space calculated from our DC parameters. We may choose this value or choose a different resistor value, as long as it is in the calculated solution space and is less than the value derived from the above rise-time calculation.	21 22 23 24 25
Our decision to choose a different resistor value than the one calculated may be the desire to use a more standard resistor value or the desire to use a value that is already used elsewhere in our design. This decision is left to the designer.	26 27 28 29
In this example, we will choose a more standard resistor value for our pullup. Let this resistor be 4.7K. As mentioned previously, we may adjust the pullup value to be less than the value derived from our rise-time calculation, without causing the bus to function improperly. We see from Equation 4 that if the resistance <i>Rp</i> is decreased, the rise time of the bus will decrease accordingly. This change will not violate the maximum rise time but will instead add more margin to our rise time.	<ul> <li>30</li> <li>31</li> <li>32</li> <li>33</li> <li>34</li> <li>35</li> <li>36</li> </ul>
We can verify this by calculating the rise time with our chosen value of pullup resistor from the equation:	37 38 39

- t = -R * C * In[(Vohmax Vccmax) / (Volmax Vccmax)]
- $t = -4.7 \times 10^{3*} 82 \times 10^{-12*} \ln[(2.7 3.036) / (0 3.036)]$

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	• <i>t</i> = 848 ns	1
	To verify that our choice does not violate the bus fall time we must check that we do not violate the specification for maximum current sunk by an output driver. We note that <i>Itotal</i> delivered to the output driver is:	2 3 4
	<ul> <li>Itotal = ((Vccmax - Volmin) / Rp) + Iil (from all bus agents)</li> <li>Itotal = ((3.63 - 0) / 4.7x10³) + 70x10⁻⁶</li> </ul>	5 6 7
	• $Itotal = 784 \mu A$	8
	This is significantly less than the rated current of 3.0mA, so our value for <i>Rp</i> is satisfactory.	9 10
	While this example shows that a stronger pullup is not required for a design that is not fully loaded, an IB Module or chassis should select a termination value that accounts for the maximum load on either end. The purpose of this example is to explain the concepts and the design concerns that should be addressed in using $I^2C$ slave agents or SMBus devices in an IB-ML design.	11 12 13 14 15 16
A2.4.7 EXAMPLE 5V TO 3.3V	TRANSLATION CIRCUIT	17
	The following is an example circuit to translate from 5V to 3.3V signaling.	18
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VOLUME 2 - PHYSICAL SPECIFICATIONS		FINAL
	Figure 216 IB-ML to 5V I ² C Translation Circu	t
	Bi-directional 5V to 3.3V Level Shifter	
	VCC_5 2.7K VCC_33 2.7K 2.7K	
	I ² C_SIG	MySIG

I²C_SIG «

5V Level

To be added in a future revision.

SCHOTTKY BAT54

Uni-directional 5V to 3.3V Level Shifter

VCC_33

2.7K

2N3904

The following is an example circuit for isolating a device from the IB-ML:

VCC 5

2.7K

5V Level

October, 2004

IMxSIG

IMxSIG

3.3V Level

3.3V Level

InfiniBandSM Trade Association

**A2.4.8 EXAMPLE ISOLATION LOGIC** 

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# ANNEX A3: HARDWARE MANAGEMENT EXAMPLES A3.1 INTRODUCTION The purpose of this annex is to provide representative implementation examples of various Hardware Management feature described in Chapter 13: Hardware Management. A3.2 MODULE AND CHASSIS MANAGEABILITY COMBINATIONS This section outlines InfiniBand Module management and proxies in different manageable Chassis types. A3.2.1 Modules By Chassis Type Table 182 shows the manageability characteristics of modules in different Chassis types.

InfiniBand Module	Passively Managed Chassis	Actively Managed Chassis	Unmanaged Chassis
xCA Module			
Fully Managed	In-band MADs targeted and responded Out-of-band access (chas- sis->Module) available, but not utilized	In-band MADs targeted and responded Out-of-band access (chassis->Module) sup- ported	In-band MADs targeted and responded
Proxy Managed	Not Defined	Not Defined	Not Defined
Unmanaged	Not Defined	Not Defined	Not Defined
Repeater Module			
Fully Managed	Not Defined	Not Defined	Not Defined
Proxy Managed	In-band requires proxy to be manageable Out-of-band access (chas- sis->Module) available, but not utilized	In-band requires proxy to be manageable Out-of-band access (chassis->Module) sup- ported	Not Defined
Unmanaged	Not Defined	Not Defined	Not Defined

## Table 182 Module Management by Chassis Type
#### 15.3.50.1 PROXIES BY CHASSIS TYPES

Since TCAs, Switches, and HCAs are protocol-aware and addressable, they can act as proxies for IB to IB-ML transactions. <u>Table 183</u> shows the possible protocol-aware proxies for the defined chassis types.

#### Table 183 Proxy Capability per Chassis Type

Protocol-aware	Unmanaged	Passively	Actively Managed Chassis		
Unit	Chassis	Managed Chassis	SEEPROM Interface	Split Transactions	
Fully Managed TCA Module as a Proxy	Not Applicable No proxy neces- sary for chassis	Capable SEEPROM Write- Read support is <u>required</u>	Capable SEEPROM Write- Read support is <u>required</u>	Conditional IBML2Ib support is <u>required</u> ; only a TCA supporting IBML2Ib can be a chassis proxy in a Chassis that uses slots as chassis portals.	
Switch as a Proxy	Not Applicable No proxy neces- sary for chassis	Capable SEEPROM Write- Read support is <u>required</u>	Capable SEEPROM Write- Read support is <u>required</u>	Conditional IBML2Ib support is <u>optional</u> ; only a Switches supporting IBML2Ib can be a chassis proxy in a Chassis that uses the Switch as a chassis portal.	
Repeater Module	Not Capable (not addressable)	Not Capable (not addressable)	Not Capable (not addressable)	Not Capable (not addressable)	
HCA Unit as a Proxy	Not Applicable No proxy neces- sary for chassis	Capable SEEPROM Write- Read support is <u>required</u>	Capable SEEPROM Write- Read support is <u>required</u>	Conditional As the HCA and the Chassis in which it resides are both choices of the system implementer, the HCA may be chosen as the proxy and thus would need IB-ML-IB support. Similarly, the system implementer may chose to use a switch or embedded TCA for the proxy.	

#### A3.3 MANAGED CHASSIS USING SLOT SWITCH AND IB-ML SELECTOR PROXY

<u>Figure 217</u> shows a Managed Chassis including an InfiniBand Switch. This Switch may be on the backplane or in a proprietary slot.



## As Figure 217 shows, from the Baseboard Manager's and the module's

## Figure 217 Example Managed Chassis with Switch

points of view, there exists one Chassis VPD per module. The chassis vendor may chose to combine these VPDs in one device.

Figure 217 shows a Chassis Management Entity (CME) which may or may not include a processor. The CME is merely an IB-ML De-Mux in its simplest form. The CME may provide a proxy for access to the modules' IB-MLs. See <u>Section 13.5.2.6, "IB-ML Selector Proxy," on page 548</u>. A proxy is necessary for managing Repeater Modules.

In-band access to the Switch VPD via Switch Management Link (SML). The SML may be implemented as an IB-ML. The Baseboard Manager

running on the Fabric may access the Switch VPD in-band via any port on the Switch-- including the ones connected to the Module Repeaters or TCAs. The CME includes a Selector as a mechanism for selecting individual IB-MLs in its SML address space. Once the Baseboard Manager detects the capabilities of the CME via the IB Switch VPD, it may select any Management Link using the Selector. The Switch VPD includes information about the number of IB-MLs connected to the CME. Once selected, any module's IB-ML is available to the Baseboard Manager as though it was connected directly to the SML. The CME's Selector optionally appears in every IB-ML's address space so that the CME may act as a proxy for inter-IB-ML communication. To manage Repeater Boards, the Baseboard Manager uses either the Switch or a TCA's access to CME. The CME has access to all modules' IB-MLs; otherwise, accessing Repeater modules' VPD is limited to the ones connected to the CME. From the Switch VPD and the Fabric Manager, the Baseboard Manager knows through which port it is entering the Switch. If the module through which the Baseboard Manager is accessing the Switch has only a Repeater on it, the Baseboard Manager uses that Switch Port Number to select the IB-ML of the Repeater module. An module may assert an interrupt. The CME may latch all of the modules' Interrupts in a register, may functionally OR them and may send an IB-ML style message to the Switch. The Switch, in turn, generates a Trap on the Fabric. The implementation of IB-ML to BMTrap is an optional Chassis feature. TCAs are protocol-aware; they provide direct access to TCA Module's IB-ML. Although the IB-ML of a TCA Module is available via the TCA, the Baseboard Manager may choose to access its IB-ML in the same manner it accesses that of a Repeater module. A3.4 XINFO EXAMPLE The following example shows how some of the xInfo records could be populated using the topology shown in Figure 218 Topology for xInfo Example on page 796. All modules are assumed to be standard sized. Given its illustrative nature, there is no consideration intended toward what is practically realizable for other considerations (i.e. building up 6

port switches with 3 port building blocks is not likely to be predominant).



Table 184 shows a potential layout of the records on Module 1 containing three switch nodes as shown in Figure 218 Topology for xInfo Example on 2 page 796. 3 Table 184 Example Module 1 xInfo 4 5 -ength (bytes) 6 Offset (hex) Offset (dec) 7 Field Value Comment 9 10 **DeviceHeader** 11 0 0 1 VPD_FormatVersion 0x11 Version 1.1 12 1 1 1 ExtensionDeviceSlaveAddress 0x00 No extension device 13 2 2 1 LSB of offset to first byte of write-pro-0x00 Begins at offset 0x0000 14 tected area 15 3 3 MSB of offset to first byte of write-pro-0x00 1 16 tected area 17 4 4 1 LSB of offset to last byte of write-pro-0xFF 18 tected area 19 5 5 1 MSB of offset to last byte of write-pro-0x00 tected area 20 21 6 6 Header Checksum (Device Header) Calculated 1 22 ModuleInfo 23 7 7 1 RecordID 0x00 ModuleInfo 24 8 8 1 **RecordParameters** 0b0_0_1_0_0010 LastRecord=no, LengthMultiplier=bytes; Rea-25 dOnly=y; Reserved=0, RecordFormat=2 26 9 1 0x11 ModuleGUID through Checksum 9 RecordLength 27 А 1 Header Checksum Calculated 10 28 11 В 8 ModuleGUID set by vendor 29 30 19 13 1 IBModuleType, ModuleClass xb001_00010 Module is an IB module, Class=Switch 31 14 20 1 NodeCount 0x03 Three (3) nodes present 32 21 1 15 LinkCount 0x0B Needs definition work!!! 33 22 16 1 BackplaneLinkCount 0x03 Three links go into the backplane 34 23 17 1 **IBMLCount** 0x01 One(1) IB-ML per physical connector 35 36 24 18 1 BackplaneIBMLCount 0x01 One(1) IB-ML per physical connector 37 25 19 1 ModuleSize 0x00 Field unpopulated in this example 38 26 1A 1 0x02 Standard Module FormFactor 39 1B 1 Checksum ModuleGUID through NodeGUIDHandle(3) 27 Calculated 40

FRUInfo

# Table 184 Example Module 1 xInfo

Offset (dec)	Offset (hex)	Length (bytes)	Field	Value	Comment
28	1C	1	RecordID	0x02	FRUInfo
29	1D	1	RecordParameters	0b0_0_1_0_0010	LastRecord=no, LengthMultiplier=bytes; Rea- dOnly=y; Reserved=0, RecordFormat=2
30	1E	1	RecordLength	0x42	FRUType through Checksum
31	1F	1	Header Checksum	Calculated	
32	20	1	FRUType	0x01	InfiniBand Module
33	21	1	FRU_Handle	0x0A	Assigned by module vendor. 0x0A done for example.
34	22	1	FRUGUID	0x01	EUI-64 GUID format. 8 bytes to follow.
35	23	8	FRUGUID data bytes	set by vendor	
43	2B	1	Serial Number	0b11_001000	Encoding type=ASCII, Character Count=8
44	2C	8	Serial Number data bytes	0x49_42_41_2D_39_3 8_37_36	IBA-9876 (example) - Vendor assigned
52	34	1	Part Number	0b11_0000110	Encoding type=ASCII, Character Count=6
53	35	6	Part Number data bytes	0x31_32_33_34_30_3 9	123409 (example) - Vendor assigned
59	3В	1	Model Number	0600_000000	Encoding type=Binary/unspecified, Charac- ter Count=0 (Model number not present in this example)
60	3C	1	Version Number	0b00_000001	Encoding type=Binary/unspecified, Charac- ter Count=1
61	3D	1	Version Number data bytes	0x02	2 (example) - Vendor assigned
62	3E	1	Manufacturer Name	0b11_001100	Encoding type=ASCII, Character Count=12
63	3F	12	Manufacturer Name data bytes	ASCII of vendor name	Vendor name
75	4B	1	Product Name	0b11_010000	Encoding type=ASCII, Character Count=16
76	4C	16	Product Name data bytes	ASCII of vendor prod- uct name	Vendor assigned name
92	5C	1	ManufacturerID	0x01	EUI-64 Company ID format, 3 bytes to follow
93	5D	3	ManufacturerID data bytes	vendor company ID	Vendor company ID
96	60	1	Mfg.Date/Time	0x00	Indicates date and time are not present
92	5C	1	Checksum	Calculated	FRUType through Mfg Date / Time
Modul	ePowerl	nfo	1		1
00	50	1	RecordID	0x03	ModulePowerInfo

### Table 184 Example Module 1 xInfo

Offset (dec)	Offset (hex)	Length (bytes)	Field	Value	Comment
94	5E	1	RecordParameters	0b0_0_1_0_0010	LastRecord=no, LengthMultiplier=bytes; Rea- dOnly=y; Reserved=0, RecordFormat=2
95	5F	1	RecordLength	0x10	FRUType through Checksum
96	60	1	Header Checksum	Calculated	
97	61	3	OperationalThermalPower	0x0061A8	Assume 25W
100	64	3	OperationalCurrent	0x007D0	Assume 2A
103	67	2	IdleCurrent	0x1F4	Assume.5A
105	69	2	InitCurrent	0x898	Assume 2.2A
107	6B	2	InitTime	0x320	Assume 8 secs (8 s * 1000ms/s / 10)
109	6D	1	ModulePMCapability	0b00000_0_0	Reserved, IsMStandbySupported=n, IsPow- erManagmentSupported=n
110	6E	1	ModuleUnitCapability	0b00000_0_0	Reserved, IsUsleepSupported=n, IsUStand- bySupported=n
111	6F	1	ModulePowerParms	0b00_01_00_01	Reserved, PowerClass=I, Reserved, Redun- dantPower=n
109	6D	1	Checksum	Calculated	OperationalThermalPower through Module- PowerParms
Buddy	Info	1			
110	6E	1	RecordID	0x07	BuddyInfo
111	6F	1	RecordParameters	0b0_0_1_0_0010	LastRecord=no, LengthMultiplier=bytes; Rea- dOnly=y; Reserved=0, RecordFormat=2
112	70	1	RecordLength	0x1D	BuddyCount through Checksum
113	71	1	Header Checksum	Calculated	
114	72	1	BuddyCount	0b000011_00	Nodes present=3, EUI-64 GUID format.
115	73	8	NodeGUID	set by vendor	Switch 1
123	7B	1	NodeGUIDHandle	0x01	Handles assigned beginning from 1 in this example
124	7C	8	NodeGUID	set by vendor	Switch 2
132	84	1	NodeGUIDHandle	0x02	Incremented
133	85	8	NodeGUID	set by vendor	Switch 3
141	8D	1	NodeGUIDHandle	0x03	Incremented
142	8E	1	Checksum	Calculated	BuddyCount through last NodeGUIDHandle

PortConnectionInfo

### Table 184 Example Module 1 xInfo

Offset (dec)	Offset (hex)	Length (bytes)	Field	Value	Comment
143	8F	1	RecordID	0x04	PortConnectionInfo
144	90	1	RecordParameters	0b1_0_1_0_0010	LastRecord=yes, LengthMultiplier=bytes; ReadOnly=y; Reserved=0, RecordFormat=2
145	91	1	RecordLength	0x2E	ConnectionInfoCount through Checksum
146	92	1	Header Checksum	Calculated	
147	93	1	ConnectionInfoCount	0x0B	Number of ports connected
148	94	1	NodeGUIDHandle	0x01	Switch 1
149	95	1	PortNo	0x01	Port 1
150	96	1	ConnectionType	0b10_011_011	Connector, PCB, Module side of Backplane connector
151	97	1	BackplaneConnection	0b0_0_001_001	Reserved, Primary Slot, Primary Connector, Physical Port 1
152	98	1	NodeGUIDHandle	0x01	Switch 1
153	99	1	PortNo	0x02	Port 2
154	9A	1	ConnectionType	0b01_011_100	No connector, PCB, Non-removable
155	9B	1	BackplaneConnection	0x00	Undefined for internal connections
156	9C	1	NodeGUIDHandle	0x01	Switch 1
157	9D	1	PortNo	0x03	Port 3
158	9E	1	ConnectionType	0b10_001_111	Connector, Copper Cable, Fully defined
159	9F	1	BackplaneConnection	0b0_0_001_001	Undefined for cable connections
160	A0	1	NodeGUIDHandle	0x01	Switch 1
161	A1	1	PortNo	0x04	Port 4
162	A2	1	ConnectionType	0b10_001_111	Connector, Copper Cable, Fully defined
163	A3	1	BackplaneConnection	0x00	Undefined for cable connections
164	A4	1	NodeGUIDHandle	0x02	Switch 2
165	A5	1	PortNo	0x01	Port 1
166	A6	1	ConnectionType	0b01_011_100	No connector, PCB, Non-removable
167	A7	1	BackplaneConnection	0x00	Undefined for internal connections
168	A8	1	NodeGUIDHandle	0x02	Switch 2
169	A9	1	PortNo	0x02	Port 2

### Table 184 Example Module 1 xinfo

Offset (dec)	Offset (hex)	Length (bytes)	Field	Value	Comment
170	AA	1	ConnectionType	0b10_011_011	Connector, PCB, Module side of Backplane connector
171	AB	1	BackplaneConnection	0b0_0_001_010	Reserved, Primary Slot, Primary Connector, Physical Port 2
172	AC	1	NodeGUIDHandle	0x02	Switch 2
173	AD	1	PortNo	0x03	Port 3
174	AE	1	ConnectionType	0b10_001_111	Connector, Copper Cable, Fully defined
175	AF	1	BackplaneConnection	0x00	Undefined for cable connections
176	B0	1	NodeGUIDHandle	0x02	Switch 2
177	B1	1	PortNo	0x04	Port 4
178	B2	1	ConnectionType	0b10_001_111	Connector, Copper Cable, Fully defined
179	B3	1	BackplaneConnection	0x00	Undefined for cable connections
180	B4	1	NodeGUIDHandle	0x03	Switch 3
181	B5	1	PortNo	0x01	Port 1
182	B6	1	ConnectionType	0b01_011_100	No connector, PCB, Non-removable
183	B7	1	BackplaneConnection	0x00	Undefined for internal connections
184	B8	1	NodeGUIDHandle	0x03	Switch 3
185	B9	1	PortNo	0x02	Port 2
186	BA	1	ConnectionType	0b01_011_100	No connector, PCB, Non-removable
187	BB	1	BackplaneConnection	0x00	Undefined for internal connections
188	BC	1	NodeGUIDHandle	0x03	Switch 3
189	BD	1	PortNo	0x03	Port 3
190	BE	1	ConnectionType	0b10_011_011	Connector, PCB, Module side of Backplane connector
191	BF	1	BackplaneConnection	0b0_0_001_011	Reserved, Primary Slot, Primary Connector, Physical Port 3
192	C0	1	No more fields indicator	0xC0	
193	C1	62	Padding	Filled with 0xFF	Pad to Writable Area
255	FF	1	Checksum	Calculated	ConnectionInfoCount through last Back- planeConnection
Asset	Tag				
256	100	1	RecordID	0x08	AssetTag

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23 24

25

Offset (dec)	Offset (hex)	Length (bytes)	Field	Value	Comment
257	101	1	RecordParameters	0b1_0_0_0_0001	LastRecord=yes, LengthMultiplier=bytes; ReadOnly=n; Reserved=0, RecordFormat=1
258	102	1	RecordLength	0x13	FRUType through Checksum
259	103	1	Header Checksum	Calculated	
260	104	1	FRU_Handle	0xA	Handle for FRU
261	105	1	AssetTag	0b11_001000	Encoding type=ASCII, Character Count=16
262	106	16	AssetTag data bytes	Value written	16 ASCII characters for this asset
278	116	1	Checksum	Calculated	FRU_Handle through Asset Tag data bytes

Table 185 shows a potential layout of the records on Module 2 containing two TCA nodes and a switch node as shown in Figure 218 Topology for xInfo Example on page 796. For classification purposes, this module is surfacing itself as a "TCA" even though it physically contains a switch element.

Table 185 Example Module 2 xinfo

Offset (dec)	Offset (hex)	Length (bytes)	Field	Value	Comment	26 27 28 29 30
Device	eHeader					31
0	0	1	VPD_FormatVersion	0x11	Version 1.1	32
1	1	1	ExtensionDeviceSlaveAddress	0x00	No extension device	33
2	2	1	LSB of offset to first byte of write-pro- tected area	0x00	Begins at offset 0x0000	34 35
3	3	1	MSB of offset to first byte of write-pro-	0x00		36
			tected area			37
4	4	1	LSB of offset to last byte of write-pro-	0xDF		38
						39
5	5	1	MSB of offset to last byte of write-pro-	0x00		40
			tected area			41
						42

	Table 185 Example Module 2 xInfo							
Offset (dec)	Offset (hex)	Length (bytes)	Field	Value	Comment			
6	6	1	Header Checksum (Device Header)	Calculated				
FRUIr	nfo							
7	7	1	RecordID	0x02	FRUInfo			
8	8	1	RecordParameters	0b0_0_1_0_0010	LastRecord=no, LengthMultiplier=bytes; Rea- dOnly=y; Reserved=0, RecordFormat=2			
9	9	1	RecordLength	0x4F	FRUType through Checksum			
10	А	1	Header Checksum	Calculated				
11	В	1	FRUType	0x01	InfiniBand Module			
12	С	1	FRU_Handle	0x0A	Assigned by module vendor. 0x0A done for example.			
13	D	1	FRUGUID	0x01	EUI-64 GUID format. 8 bytes to follow.			
4	E	8	FRUGUID data bytes	set by vendor				
22	16	1	Serial Number	0b11_001000	Encoding type=ASCII, Character Count=8			
23	17	8	Serial Number data bytes	set by vendor				
31	1F	1	Part Number	0b11_001000	Encoding type=ASCII, Character Count=8			
32	20	8	Part Number data bytes	set by vendor				
40	28	1	Model Number	0b11_001000	Encoding type=ASCII, Character Count=8			
41	29	8	Model Number data bytes	set by vendor				
49	31	1	Version Number data bytes	0x01	1 (example) - Vendor assigned			
50	32	1	Manufacturer Name	0b11_010000	Encoding type=ASCII, Character Count=16			
51	33	16	Manufacturer Name data bytes	set by vendor	Vendor name			
67	43	1	Product Name	0b11_010000	Encoding type=ASCII, Character Count=16			
68	44	16	Product Name data bytes	ASCII of vendor prod- uct name	Vendor assigned name			
34	54	1	ManufacturerID	0x01	EUI-64 Company ID format, 3 bytes to follow			
85	55	3	ManufacturerID data bytes	vendor company ID	Vendor company ID			
38	58	1	Mfg.Date/Time	0x00	Indicates date and time are not present			
84	54	1	Checksum	Calculated	FRUType through Mfg Date / Time			
Modul	ePower	Info		•	•			
35	55	1	RecordID	0x03	ModulePowerInfo			

# Table 185 Example Module 2 xInfo

Offset (dec)	Offset (hex)	Length (bytes)	Field	Value	Comment
86	56	1	RecordParameters	0b0_0_1_0_0010	LastRecord=no, LengthMultiplier=bytes; Rea- dOnly=y; Reserved=0, RecordFormat=2
87	57	1	RecordLength	0x10	FRUType through Checksum
88	58	1	Header Checksum	Calculated	
89	59	3	OperationalThermalPower	0x0061A8	Assume 25W
92	5C	3	OperationalCurrent	0x007D0	Assume 2A
95	5F	2	IdleCurrent	0x1F4	Assume .5A
97	61	2	InitCurrent	0x898	Assume 2.2A
99	63	2	InitTime	0x320	Assume 8 secs (8 s * 1000ms/s / 10)
101	65	1	ModulePMCapability	0b00000_0_0	Reserved, IsMStandbySupported=n, IsPow- erManagmentSupported=n
102	66	1	ModuleUnitCapability	0b00000_0_0	Reserved, IsUsleepSupported=n, IsUStand- bySupported=n
103	67	1	ModulePowerParms	0b00_01_00_01	Reserved, PowerClass=I, Reserved, Redun- dantPower=n
101	65	1	Checksum	Calculated	OperationalThermalPower through Module- PowerParms
Modul	eInfo				
102	66	1	RecordID	0x00	ModuleInfo
103	67	1	RecordParameters	0b0_0_1_0_0010	LastRecord=no, LengthMultiplier=bytes; Rea- dOnly=y; Reserved=0, RecordFormat=2
104	68	1	RecordLength	0x2C	ModuleGUID through Checksum
105	69	1	Header Checksum	Calculated	
106	6A	8	ModuleGUID	set by vendor	
114	72	1	IBModuleType, ModuleClass	xb001_00000	Module is an IB module, Class=TCA
115	73	1	NodeCount	0x03	Three (3) nodes present
116	74	1	LinkCount	0x07	Needs definition work!!!
117	75	1	BackplaneLinkCount	0x03	Three links go into the backplane
18	76	1	IBMLCount	0x01	One(1) IB-ML per physical connector
119	77	1	BackplanelBMLCount	0x01	One(1) IB-ML per physical connector
20	78	1	ModuleSize	0x00	Field unpopulated in this example
121	79	1	FormFactor	0x02	Standard Module

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	Table 185 Example Module 2 xInfo						
Offset (dec)	Offset (hex)	Length (bytes)	Field	Value	Comment		
122	7A	1	Checksum	Calculated	ModuleGUID through NodeGUIDHandle(3)		
Buddy	Info						
123	7B	1	RecordID	0x07	BuddyInfo		
124	7C	1	RecordParameters	0b0_0_1_0_0010	LastRecord=no, LengthMultiplier=bytes; Rea- dOnly=y; Reserved=0, RecordFormat=2		
125	7D	1	RecordLength	0x2C	BuddyCount through Checksum		
126	7E	1	Header Checksum	Calculated			
127	7F	1	BuddyCount	0b000011_00	Nodes present=3, EUI-64 GUID format.		
128	80	8	NodeGUID	set by vendor	TCA 1		
136	88	1	NodeGUIDHandle	0x80	Handles assigned beginning from 80h in this example		
137	89	8	NodeGUID	set by vendor	TCA 2		
145	91	1	NodeGUIDHandle	0x81	Incremented		
146	92	8	NodeGUID	set by vendor	Switch 3		
154	9A	1	NodeGUIDHandle	0x82	Incremented		
155	9B	1	Checksum	Calculated	BuddyCount through last NodeGUIDHandle		
PortCo	onnectio	nInfo					
156	9C	1	RecordID	0x04	PortConnectionInfo		
157	9D	1	RecordParameters	0b1_0_1_0_0010	LastRecord=yes, LengthMultiplier=bytes; ReadOnly=y; Reserved=0, RecordFormat=2		
158	9E	1	RecordLength	0x1E	ConnectionInfoCount through Checksum		
159	9F	1	Header Checksum	Calculated			
160	A0	1	ConnectionInfoCount	0x07	Number of ports connected		
161	A1	1	NodeGUIDHandle	0x80	TCA 1		
162	A2	1	PortNo	0x01	Port 1		
163	A3	1	ConnectionType	0b10_011_011	Connector, PCB, Module side of Backplane connector		
164	A4	1	BackplaneConnection	0b0_0_001_001	Reserved, Primary Slot, Primary Connector, Physical Port 1		
165	A5	1	NodeGUIDHandle	0x80	TCA 1		
166	A6	1	PortNo	0x02	Port 2		
167	A7	1	ConnectionType	0b01_011_100	No connector, PCB, Non-removable		

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### Table 185 Example Module 2 xInfo

Offset (dec)	Offset (hex)	Length (bytes)	Field	Value	Comment
168	A8	1	BackplaneConnection	0x00	Undefined for internal connections
169	A9	1	NodeGUIDHandle	0x81	TCA 2
170	AA	1	PortNo	0x01	Port 1
171	AB	1	ConnectionType	0b10_011_011	Connector, PCB, Module side of Backplane connector
172	AC	1	BackplaneConnection	0b0_0_001_010	Reserved, Primary Slot, Primary Connector, Physical Port 2
173	AD	1	NodeGUIDHandle	0x81	TCA 2
174	AE	1	PortNo	0x02	Port 2
175	AF	1	ConnectionType	0b01_011_100	No connector, PCB, Non-removable
176	B0	1	BackplaneConnection	0x00	Undefined for internal connections
177	B1	1	NodeGUIDHandle	0x82	Switch 3
178	B2	1	PortNo	0x01	Port 1
179	B3	1	ConnectionType	0b01_011_100	No connector, PCB, Non-removable
180	B4	1	BackplaneConnection	0x00	Undefined for internal connections
181	B5	1	NodeGUIDHandle	0x82	Switch 3
182	B6	1	PortNo	0x02	Port 2
183	B7	1	ConnectionType	0b01_011_100	No connector, PCB, Non-removable
184	B8	1	BackplaneConnection	0x00	Undefined for internal connections
185	B9	1	NodeGUIDHandle	0x82	Switch 3
186	BA	1	PortNo	0x03	Port 3
187	BB	1	ConnectionType	0b10_011_011	Connector, PCB, Module side of Backplane connector
188	BC	1	BackplaneConnection	0b0_0_001_011	Reserved, Primary Slot, Primary Connector, Physical Port 3
189	BD	1	Checksum	Calculated	ConnectionInfoCount through last Back- planeConnection
Asset	Tag				
224	E0	1	RecordID	0x08	AssetTag
225	E1	1	RecordParameters	0b1_0_0_0_0001	LastRecord=yes, LengthMultiplier=bytes; ReadOnly=n; Reserved=0, RecordFormat=1
226	E2	1	RecordLength	0x23	FRUType through Checksum

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### Table 185 Example Module 2 xInfo

Offset (dec)	Offset (hex)	Length (bytes)	Field	Value	Comment	2 3 4 5 6
227	E3	1	Header Checksum	Calculated		7
228	E4	1	FRU_Handle	0xA	Handle for FRU	8
229	E5	1	AssetTag	0b11_010000	Encoding type=ASCII, Character Count=32	9
230	E6	32	AssetTag data bytes	Value written	32 ASCII characters for this asset	10
262	106	1	Checksum	Calculated	FRU_Handle through Asset Tag data bytes	11 - 12

Table 186shows a potential layout of the records on Module 3 containing13a single HCA node as shown in Figure 218 Topology for xInfo Example on14page 796.15

 Table 186 Example Module 3 xInfo

					kiilo	1
Offset (dec)	Offset (hex)	Length (bytes)	Field	Value	Comment	18 19 20 21
Devic	eHeader					• Z
0	0	1	VPD_FormatVersion	0x11	Version 1.1	24
1	1	1	ExtensionDeviceSlaveAddress	0x00	No extension device	25
2	2	1	LSB of offset to first byte of write-pro- tected area	0x00	Begins at offset 0x0000	26 27
3	3	1	MSB of offset to first byte of write-pro- tected area	0x00		28
4	4	1	LSB of offset to last byte of write-pro- tected area	0xE5	End of PortConnectionInfo (for this example)	3(
5	5	1	MSB of offset to last byte of write-pro- tected area	0x00		3
6	6	1	Header Checksum (Device Header)	Calculated		- 34
Modu	leInfo					3!
7	7	1	RecordID	0x00	ModuleInfo	36
8	8	1	RecordParameters	0b0_0_1_0_0010	LastRecord=no, LengthMultiplier=bytes; Rea- dOnly=y; Reserved=0, RecordFormat=2	31
9	9	1	RecordLength	0x1A	ModuleGUID through Checksum	39
10	А	1	Header Checksum	Calculated		- 4(
	I	I	1	I	1	4
						- 42

### Table 186 Example Module 3 xInfo

Offset (dec)	Offset (hex)	Length (bytes)	Field	Value	Comment
11	В	8	ModuleGUID	set by vendor	
19	13	1	IBModuleType, ModuleClass	xb001_00001	Module is an IB module, Class=HCA
20	14	1	NodeCount	0x01	One (1) node present
21	15	1	LinkCount	0x02	Needs definition work!!!
22	16	1	BackplaneLinkCount	0x02	Three links go into the backplane
23	17	1	IBMLCount	0x01	One(1) IB-ML per physical connector
24	18	1	BackplanelBMLCount	0x01	One(1) IB-ML per physical connector
25	19	1	ModuleSize	0x00	Field unpopulated in this example
26	1A	1	FormFactor	0x02	Standard Module
27	1B	1	Checksum	Calculated	ModuleGUID through NodeGUIDHandle(3)
FRUIr	fo				
28	1C	1	RecordID	0x02	FRUInfo
29	1D	1	RecordParameters	0b0_0_1_0_0010	LastRecord=no, LengthMultiplier=bytes; Rea- dOnly=y; Reserved=0, RecordFormat=2
30	1E	1	RecordLength	0x89	FRUType through Checksum
31	1F	1	Header Checksum	Calculated	
32	20	1	FRUType	0x01	InfiniBand Module
33	21	1	FRU_Handle	0xCD	Assigned by module vendor. 0xCD done for example.
34	22	1	FRUGUID	0x01	EUI-64 GUID format. 8 bytes to follow.
35	23	8	FRUGUID data bytes	set by vendor	
43	2B	1	Serial Number	0b10_001000	Encoding type=Unicode, Character Count=8 (note Unicode 3 have 2 byte characters)
44	2C	16	Serial Number data bytes	set by vendor	Vendor assigned
60	3C	1	Part Number	0b10_010000	Encoding type=Unicode, Character Count=16
61	3D	32	Part Number data bytes	set by vendor	Vendor assigned
93	5D	1	Model Number	0b10_010000	Encoding type=Unicode, Character Count=16
94	5E	32	Model Number data bytes	set by vendor	Vendor assigned
94	5E	1	Version Number	0b00_000010	Encoding type=Binary/unspecified, Charac- ter Count=2

# Table 186 Example Module 3 xInfo

Offset (dec)	Offset (hex)	Length (bytes)	Field	Value	Comment
95	5F	2	Version Number data bytes	0x0005	5 (example) - Vendor assigned
97	61	1	Manufacturer Name	0b10_010000	Encoding type=Unicode, Character Count=16
98	62	32	Manufacturer Name data bytes	set by vendor	Vendor assigned
130	82	1	Product Name	0b10_010000	Encoding type=Unicode, Character Count=16
131	83	32	Product Name data bytes	set by vendor	Vendor assigned
163	A3	1	ManufacturerID	0x01	EUI-64 Company ID format, 3 bytes to follow
164	A4	3	ManufacturerID data bytes	vendor company ID	Vendor company ID
167	A7	1	Mfg.Date/Time	0x00	Indicates date and time are not present
168	A8	1	Checksum	Calculated	FRUType through Mfg Date / Time
Modul	ePowerl	nfo			
169	A9	1	RecordID	0x03	ModulePowerInfo
170	AA	1	RecordParameters	0b0_0_1_0_0010	LastRecord=no, LengthMultiplier=bytes; Rea- dOnly=y; Reserved=0, RecordFormat=2
171	AB	1	RecordLength	0x10	FRUType through Checksum
172	AC	1	Header Checksum	Calculated	
173	AD	3	OperationalThermalPower	0x0061A8	Assume 25W
176	B0	3	OperationalCurrent	0x007D0	Assume 2A
179	B3	2	IdleCurrent	0x1F4	Assume .5A
181	B5	2	InitCurrent	0x820	Assume 2.08A
183	B7	2	InitTime	0x1770	Assume 60 secs (60 s * 1000ms/s / 10)
185	B9	1	ModulePMCapability	0b00000_1_1	Reserved, IsMStandbySupported=y, IsPow- erManagmentSupported=y
186	BA	1	ModuleUnitCapability	0b00000_0_0	Reserved, IsUsleepSupported=n, IsUStand- bySupported=n (for this example, the imple- mentation uses IOC functionality to perform power management)
187	BB	1	ModulePowerParms	0b00_10_00_01	Reserved, PowerClass=II, Reserved, Redun- dantPower=n
185	B9	1	Checksum	Calculated	OperationalThermalPower through Module-

# Table 186 Example Module 3 xInfo

Offset (dec)	Offset (hex)	Length (bytes)	Field	Value	Comment
186	BA	1	RecordID	0x09	IOCPMInfo
187	BB	1	RecordParameters	0b0_0_1_0_0010	LastRecord=no, LengthMultiplier=bytes; Rea- dOnly=y; Reserved=0, RecordFormat=2
188	BC	1	RecordLength	0x1A	BuddyCount through Checksum
189	BD	1	Header Checksum	Calculated	
190	BE	1	IOC_Count	0x01	1 node present
191	BF	1	IOCPMCapabilty	0b1_1_1_1_1_1_1_1_1	Doze=y, Nap=y, Sleep=y, Standby=y, WRE- Doze=y, WRENap=y, WRESleep=y, WRE- Standby=n
192	C0	2	IDozeCurrent	0x05DC	Assume 1.5A
194	C2	2	INapCurrent	0x044C	Assume 1.1A
196	C4	2	ISleepCurrent	0x012C	Assume .3A
198	C6	2	IStandbyCurrent	0x00E6	Assume .23A (@ 5V = 1.15W)
200	C8	1	Checksum	Calculated	BuddyCount through last NodeGUIDHandle
Buddy	Info				
201	C9	1	RecordID	0x07	BuddyInfo
202	CA	1	RecordParameters	0b0_0_1_0_0010	LastRecord=no, LengthMultiplier=bytes; Rea- dOnly=y; Reserved=0, RecordFormat=2
203	СВ	1	RecordLength	0x1A	BuddyCount through Checksum
204	СС	1	Header Checksum	Calculated	
205	CD	1	BuddyCount	0b000001_00	Nodes present=1, EUI-64 GUID format.
206	CE	8	NodeGUID	set by vendor	НСА
214	D6	1	NodeGUIDHandle	0x00	Handles assigned beginning from 00h in this example
215	D7	1	Checksum	Calculated	BuddyCount through last NodeGUIDHandle
PortCo	onnectio	nInfo			
216	D8	1	RecordID	0x04	PortConnectionInfo
217	D9	1	RecordParameters	0b1_0_1_0_0010	LastRecord=yes, LengthMultiplier=bytes; ReadOnly=y; Reserved=0, RecordFormat=2
218	DA	1	RecordLength	0x0A	ConnectionInfoCount through Checksum
219	DB	1	Header Checksum	Calculated	
220	DC	1	ConnectionInfoCount	0x02	Number of ports connected

Table 186 Example Module 3 xlr	nfo
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Offset (dec)	Offset (hex)	Length (bytes)	Field	Value	Comment
221	DD	1	NodeGUIDHandle	0x00	НСА
222	DE	1	PortNo	0x01	Port 1
223	DF	1	ConnectionType	0b10_011_011	Connector, PCB, Module side of Backplane connector
224	E0	1	BackplaneConnection	0b0_0_001_001	Reserved, Primary Slot, Primary Connector, Physical Port 1
225	E1	1	NodeGUIDHandle	0x00	НСА
226	E2	1	PortNo	0x02	Port 2
227	E3	1	ConnectionType	0b10_011_011	Connector, PCB, Module side of Backplane connector
228	E4	1	BackplaneConnection	0b0_0_001_010	Reserved, Primary Slot, Primary Connector, Physical Port 2
229	E5	1	Checksum	Calculated	ConnectionInfoCount through last Back- planeConnection
Asset	Tag				
230	E6	1	RecordID	0x08	AssetTag
231	E7	1	RecordParameters	0b1_0_0_0_0001	LastRecord=yes, LengthMultiplier=bytes; ReadOnly=n; Reserved=0, RecordFormat=1
232	E8	1	RecordLength	0x13	FRUType through Checksum
233	E9	1	Header Checksum	Calculated	
234	EA	1	FRU_Handle	0xCD	Handle for FRU
235	EB	1	AssetTag	0b11_001000	Encoding type=ASCII, Character Count=16
236	EC	16	AssetTag data bytes	Value written	16 ASCII characters for this asset
252	FC	1	Checksum	Calculated	FRU_Handle through Asset Tag data bytes

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	Table 187 shows a potential layout of the records on the Chassis con- taining the switch and Ethernet TCA shown in Figure 218 Topology for xInfo Example on page 796.						
			Table 187 Exam	ple ChassisInfo D	Device		
Offset (dec)	Offset (hex)	Length (bytes)	Field	Value	Comment		
Devic	eHeader				·		
0	0	1	VPD_FormatVersion	0x11	Version 1.1		
1	1	1	ExtensionDeviceSlaveAddress	0x00	No extension device		
2	2	1	LSB of offset to first byte of write-pro- tected area	0x00	Begins at offset 0x0000		
3	3	1	MSB of offset to first byte of write-pro- tected area	0×00			
4	4	1	LSB of offset to last byte of write-pro- tected area	0x80			
5	5	1	MSB of offset to last byte of write-pro- tected area	0x00			
6	6	1	Header Checksum (Device Header)	Calculated			
Chase	sisInfo	•					
7	7	1	RecordID	0x01	ChassisInfo		
8	8	1	RecordParameters	0b0_0_1_0_0010	LastRecord=no, LengthMultiplier=bytes; Rea- dOnly=y; Reserved=0, RecordFormat=2		
9	9	1	RecordLength	0x1B	ChassisGUID through Checksum		
10	А	1	Header Checksum	Calculated			
11	В	8	ChassisGUID	set by vendor			
19	13	1	SlotCount	0x03	Three (3) IB slots for this example, removable CME and any others are not included. Assume High Slot Number for the chassis is 8.		
20	14	1	SlotNumbers	0b1_0_01_01_00	Last byte=n, reserved, Standard Slots for each of slots 3, 2, 1		
21	15	1	SlotNumbers	0b1_0_00_00_01	Last byte=n, reserved, Standard Slots for each of slots 6, 5, 4		
22	16	1	SlotNumbers	0b0_0_00_00_00	Last byte=y, reserved, Standard Slots for each of slots 9, 8, 7		
23	17	1	CMEAccess	0b1_0001111	Last byte=n, CME access for each of slots 7, 6, 5, 4, 3, 2, 1		

# Table 187 Example ChassisInfo Device

Offset (dec)	Offset (hex)	Length (bytes)	Field	Value	Comment
24	18	1	CMEAccess	0b0_000000	Last byte=y, CME access for each of slots 14,13, 12, 11, 10 , 9 , 8
25	19	1	SlotNumber	0x00	Indicates this is the chassis containing the CME
26	1A	1	SlotDetails	0b01_1_0_00_00	CMEAccess=y, ProxyAccess=y, reserved, LockDriveCTR=unspecified, Mechanical- LockPresent=unspecified
27	1B	1	NodeCount	0x02	Nodes on this Chassis (2) - Switch and Ether- net device
28	1C	1	Checksum	Calculated	ChassisGUID through NodeGUIDHandle(2)
Buddy	Info				
29	1D	1	RecordID	0x07	BuddyInfo
30	1E	1	RecordParameters	0b0_0_1_0_0010	LastRecord=no, LengthMultiplier=bytes; Rea- dOnly=y; Reserved=0, RecordFormat=2
31	1F	1	RecordLength	0x24	BuddyCount through Checksum
32	20	1	Header Checksum	Calculated	
33	21	1	BuddyCount	0b000010_00	Nodes present=2, EUI-64 GUID format.
34	22	8	NodeGUID	set by vendor	Chassis Switch
42	2A	1	NodeGUIDHandle	0x00	Handles assigned beginning from 00h in this example
43	2B	8	NodeGUID	set by vendor	TCA - Chassis Ethernet
51	33	1	NodeGUIDHandle	0x01	Incremented
52	34	1	Checksum	Calculated	BuddyCount through last NodeGUIDHandle
PortCo	onnectio	nInfo		l	
53	35	1	RecordID	0x04	PortConnectionInfo
54	36	1	RecordParameters	0b1_0_1_0_0010	LastRecord=yes, LengthMultiplier=bytes; ReadOnly=y; Reserved=0, RecordFormat=2
55	37	1	RecordLength	0x3A	ConnectionInfoCount through Checksum
56	38	1	Header Checksum	Calculated	
57	39	1	ConnectionInfoCount	0x0E	Number of ports connected - 13 for switch, 1 for Ethernet device
58	ЗA	1	NodeGUIDHandle	0x00	Switch
59	3B	1	PortNo	0x01	Port 1

# Table 187 Example ChassisInfo Device

Offset (dec)	Offset (hex)	Length (bytes)	Field	Value	Comment		
60	3C	1	ConnectionType	0b10_011_010	Connector, PCB, Chassis side of Backplane connector		
61	3D	1	BackplaneConnection	0b0_0_000_001	Reserved, Connector Location=Primary, Reserved, Physical Port Number=1		
62	3E	1	NodeGUIDHandle	0x00	Switch		
63	3F	1	PortNo	0x02	Port 2		
64	40	1	ConnectionType	0b10_011_010	Connector, PCB, Chassis side of Backplane connector		
65	41	1	BackplaneConnection	060_0_000_011	Reserved, Connector Location=Primary, Reserved, Physical Port Number=3		
66	42	1	NodeGUIDHandle	0x00	Switch		
67	43	1	PortNo	0x03	Port 3		
68	44	1	ConnectionType	0b10_011_010	Connector, PCB, Chassis side of Backplane connector		
69	45	1	BackplaneConnection	060_0_000_010	Reserved, Connector Location=Primary, Reserved, Physical Port Number=2		
70	46	1	NodeGUIDHandle	0x00	Switch		
71	47	1	PortNo	0x04	Port 4		
72	48	1	ConnectionType	0b10_011_010	Connector, PCB, Chassis side of Backplane connector		
73	49	1	BackplaneConnection	060_0_000_001	Reserved, Connector Location=Primary, Reserved, Physical Port Number=1		
74	4A	1	NodeGUIDHandle	0x00	Switch		
75	4B	1	PortNo	0x05	Port 5		
76	4C	1	ConnectionType	0b10_011_010	Connector, PCB, Chassis side of Backplane connector		
77	4D	1	BackplaneConnection	060_0_000_011	Reserved, Connector Location=Primary, Reserved, Physical Port Number=3		
78	4E	1	NodeGUIDHandle	0x00	Switch		
79	4F	1	PortNo	0x06	Port 6		
80	50	1	ConnectionType	0b10_011_010	Connector, PCB, Chassis side of Backplane connector		
81	51	1	BackplaneConnection	060_0_000_010	Reserved, Connector Location=Primary, Reserved, Physical Port Number=2		
82	52	1	NodeGUIDHandle	0x00	Switch		

# Table 187 Example ChassisInfo Device

Offset (dec)	Offset (hex)	Length (bytes)	Field	Value	Comment
83	53	1	PortNo	0x07	Port 7
84	54	1	ConnectionType	0b10_011_010	Connector, PCB, Chassis side of Backplane connector
85	55	1	BackplaneConnection	0b0_0_000_001	Reserved, Connector Location=Primary, Reserved, Physical Port Number=1
86	56	1	NodeGUIDHandle	0x00	Switch
87	57	1	PortNo	0x08	Port 8
88	58	1	ConnectionType	0b10_011_010	Connector, PCB, Chassis side of Backplane connector
89	59	1	BackplaneConnection	0b0_0_000_011	Reserved, Connector Location=Primary, Reserved, Physical Port Number=3
90	5A	1	NodeGUIDHandle	0x00	Switch
91	5B	1	PortNo	0x09	Port 9
92	5C	1	ConnectionType	0b10_011_010	Connector, PCB, Chassis side of Backplane connector
93	5D	1	BackplaneConnection	0b0_0_000_010	Reserved, Connector Location=Primary, Reserved, Physical Port Number=2
94	5E	1	NodeGUIDHandle	0x00	Switch
95	5F	1	PortNo	0x0A	Port 10
96	60	1	ConnectionType	0b10_001_111	Connector, Copper Cable, Fully defined
97	61	1	BackplaneConnection	0x00	Undefined for cable connections
98	62	1	NodeGUIDHandle	0x00	Switch
99	63	1	PortNo	0x0B	Port 11
100	64	1	ConnectionType	0b10_010_111	Connector, Fiber Cable, Fully defined
101	65	1	BackplaneConnection	0x00	Undefined for fiber connections
102	66	1	NodeGUIDHandle	0x00	Switch
103	67	1	PortNo	0x0C	Port 12
104	68	1	ConnectionType	0b01_011_100	No connector, PCB, Non-removable
105	69	1	BackplaneConnection	0x00	Undefined for internal connections
106	6A	1	NodeGUIDHandle	0x00	Switch
107	6B	1	PortNo	0x0D	Port 13
108	6C	1	ConnectionType	0b10_011_001	Connector, PCB, Non-IBA Removable

Offset (dec)	Offset (hex)	Length (bytes)	Field	Value	Comment
109	6D	1	BackplaneConnection	0x00	Undefined for internal connections
110	6E	1	NodeGUIDHandle	0x01	Ethernet TCA
111	6F	1	PortNo	0x01	Port 1
112	70	1	ConnectionType	0b01_011_100	No connector, PCB, Non-removable
113	71	1	BackplaneConnection	0x00	Undefined for internal connections
114	72	1	Checksum	Calculated	ConnectionInfoCount through last Back- planeConnection
Asset	Гад				
128	80	1	RecordID	0x08	AssetTag
129	81	1	RecordParameters	0b1_0_0_0_0001	LastRecord=yes, LengthMultiplier=bytes; ReadOnly=n; Reserved=0, RecordFormat=1
130	82	1	RecordLength	0x13	FRUType through Checksum
131	83	1	Header Checksum	Calculated	
132	84	1	FRU_Handle	0xA	Handle for FRU
133	85	1	AssetTag	0b11_001000	Encoding type=ASCII, Character Count=16
134	86	16	AssetTag data bytes	Value written	16 ASCII characters for this asset
150	96	1	Checksum	Calculated	FRU_Handle through Asset Tag data bytes

Table 187 Example ChassisInfo Device

Table 188shows a potential layout of the records on the CME pluggable28element shown in Figure 218Topology for xInfo Example on page 796...29Note that this element is not an InfiniBand defined module form factor but30it is a node on the InfiniBand fabric.31

### Table 188 Example CMEInfo Device

Offset (dec)	Offset (hex)	Length (bytes)	Field	Value	Comment	34 35 36 37
DeviceHeader						
0	0	1	VPD_FormatVersion	0x11	Version 1.1	39 40
1	1	1	ExtensionDeviceSlaveAddress	0x00	No extension device	41
				•		/2

26 27

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Offset (dec)	Offset (hex)	Length (bytes)	Field	Value	Comment
2	2	1	LSB of offset to first byte of write-protected area	0xFF	Begins at offset 0x0000
3	3	1	MSB of offset to first byte of write-protected area	0xFF	
4	4	1	LSB of offset to last byte of write-protected area	0x00	No writable area
5	5	1	MSB of offset to last byte of write-protected area	0x00	
6	6	1	Header Checksum (Device Header)	Calculated	
CMEI	nfo				
7	7	1	RecordID	0x05	CMEInfo
В	8	1	RecordParameters	0b1_0_1_0_0010	LastRecord=yes, LengthMultiplier=bytes; ReadOnly=y; Reserved=0, RecordFormat=2
9	9	1	RecordLength	0xE	BuddyCount through Checksum
10	А	1	Header Checksum	Calculated	
11	В	1	CMEGUID	0x01	EUI-64 GUID format. 8 bytes to follow.
12	С	8	CMEGUID data bytes	set by vendor	
20	14	2	CMEFirmware Revision	0x0312	"12.3" set by vendor
22	16	1	SlotNumbers	0b1_0_01_01_00	Last byte=n, reserved, Standard Slots for each of slots 3, 2, 1
23	17	1	SlotNumbers	0b1_0_00_00_01	Last byte=n, reserved, Standard Slots for each of slots 6, 5, 4
24	18	1	SlotNumbers	0b0_0_00_00_00	Last byte=y, reserved, Standard Slots for each of slots 9, 8, 7
25	19	1	Checksum	Calculated	BuddyCount through last NodeGUIDHandle
	I	1	1	1	1

### Table 188 Example CMEInfo Device

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Baseboard Management MAD 570	
Baseboard Manager	
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Blink	
blinking	
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BMSequence	
BMTrap	
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