

Multi-core Programming Evolution

Based on slides from Intel Software College and *Multi-Core Programming – increasing performance through software multi-threading* by Shameem Akhter and Jason Roberts,



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Formal Definition of Threads, Processors, and Hyper-Threading in Terms of Resources

- Thread
 - Basic unit of CPU utilization
 - Program counter, CPU state information, stack
- Processor
 - Architecture state: general purpose CPU registers, interrupt controller registers, caches, buses, execution units, branch prediction logic
- Logical Processor
 - Duplicates the architecture space of processor
 - Execution can be shared among different processors
- HyperThreading
 - Intel version of Simultaneous Multi-Threading (SMT)
 - Makes single physical processor appear as multiple logical processors
 - OS can schedule to logical processors

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HyperThreading and Multicore

- HyperThreading
 - Instructions from logical processors are persistent and execute on shared execution resources
 - Up to microarchitecture how and when to interleave the instructions
 - When one thread stalls, another can proceed
 - This includes cache misses, and branch mispredictions
- Multicore
 - Chip multiprocessing
 - 2 or more execution cores in a single processor
 - 2 or more processors on a single die
 - Can share an on-chip cache
 - · Can be combined with SMT













Evolution to Dual Core
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Taking full advantage of Multi-Core requires multi-threaded software

- •Increased responsiveness and worker productivity – Increased application responsiveness when different tasks run in parallel
- •Improved performance in parallel environments – When running computations on multiple processors
- •More computation per cubic foot of data center – Web-based apps are often multi-threaded by nature





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Memory Caching Example

- Each core may have own cache
 - May be out of sync
 - Ex: 2 thread on dual-core reading and writing neighboring memory locations
 - Data values may be in same cache line because of data locality
 - Memory system may mark the line as invalid due to write
 - Result is cache miss even though the data in cache being read is valid
 - Not an issue on single-core since only one cache

Thread Priorities Example

- Applications with two threads of different priorities
 - To improve performance developer assumes that higher thread will run without interference from lower priority thread
 - On single core valid since scheduler will not yield CPU to lower priority thread
 - On multi-core may schedule 2 threads on different cores, and they may run simultaneously making code unstable