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Summary

THE MULTI-DIMENSIONAL ACCESS MEMORY IN STARAN

By Kenneth E. Batcher
Digital Technology Department
Goodyear Aerospace Corporation
Akron, Ohio

Each array module in the STARAN+ associative array processor contains a 256 x 256 multi-dimensional access (MDA) memory (see illustration). Parallel vector arithmetic and associative search operations access memory data by bit-slices, while input, output, and scalar arithmetic operations access memory data by words. The MDA memories use standard random-access memory (RAM), integrated-circuit chips in a novel configuration. Use of standard, high-volume, low pin-count memory devices in place of custom LSI devices reduces costs significantly.

To achieve multidimensional access, data are stored in a scrambled pattern; bit B of word W is stored in bit-location B of memory chip B ⊕ W where ⊕ indicates a component-by-component exclusive-or.

Data are accessed by specifying a stencil shape with an 8-bit access mode and a stencil position with an 8-bit global address. The 256 memory bits covered by a stencil can be fetched or stored in one memory cycle.

The address bus structure of the MDA memory has 16 address lines (as opposed to 8 lines for a conventional RAM). For k = 1, 2, . . . , 8 address line x_k is fed by the kth bit of the global address, while address line y_k is fed by the exclusive-or of the kth bits of the access mode and the global address. Address pin k of memory chip (c_1 c_2 . . . c_8) is connected either to x_k if c_k = 0 or to y_k if c_k = 1.

Memory data are scrambled and unscrambled by a scramble/unscramble network, which can also shift and perform other useful permutations on data fetched from memory.

When memory data are fetched or stored with access mode M and global address G, processing element P accesses bit (M·G) ⊕ (M·P) of memory word (M·G) ⊕ (M·P), where logical negation is indicated by "̅" and the logical product ("and") is indicated by ·."

Bit-slice access is obtained with M = (00000000) and word access is obtained with M = (11111111). Other access modes allow data to be accessed in other ways.

* This is a summary of a paper that has been submitted for publication in the IEEETC Special Issue on Parallel Processing

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Block Diagram of STARAN Array Module