



# 19<sup>th</sup> International Parallel and Distributed Processing Symposium

## Workshop on Massively Parallel Processing

### Friday, April 8, 2005

Start	End	Title
8:00 AM	8:10 AM	<b>Workshop Introduction</b> – Dr. Ray Hoare, University of Pittsburgh
8:10 AM	9:10 AM	<b>Keynote: Comparison of Very Large-Scale Systems: An Application Performance Perspective using Thousands of Processors</b> Dr. Darren Kerbyson Los Alamos National Laboratory
		<b>Session: Communication in Massively Parallel Systems</b>
9:10 AM	9:35 AM	<b>TiNy Threads: a Thread Virtual Machine for the Cyclops64 Cellular Architecture</b> J. Cuvillo, W. Zhu, Z. Hu and G. Gao University of Delaware
9:35 AM	10:00 AM	<b>Sparse Flat Neighborhood Networks (SFNNs): Scalable Guaranteed Pairwise Bandwidth &amp; Unit Latency</b> T. Mattox, H. Dietz and W. Bieter University of Kentucky
10:00 AM	10:30 AM	<b>BREAK</b>
10:30 AM	10:55 AM	<b>An Empirical Comparison of OTIS-mesh and OTIS-hypercube Multicomputer Systems Under Deterministic Routing</b> H. Najafabadi, H. Sarbazi-azad, IPM and Sharif University of Technology, Iran
10:55 AM	11:20 AM	<b>The effect of Virtual channel Organization on the Performance of Interconnection networks</b> M. Rezazad and H. Sarbazi-Azad IPM and Sharif University of Technology, Iran
11:20 AM	11:45 AM	<b>Performance of Fault-tolerant Distributed Shared Memory on Broadcast- and Switch-based Architectures</b> C. Katsinis Drexel University
11:45 AM	1:15 PM	<b>LUNCH</b>
		<b>Session: Massively Parallel Architectures and Models</b>
1:15 PM	1:40 PM	<b>Afternoon Keynote:</b> <b>Industry Perspective: Parallel Processing on a Chip</b> WorldScape Inc.
1:40 PM	2:05 PM	<b>Extracting Speedup From C-code With Poor Instruction-level Parallelism</b> D. Kusic, R. Hoare, A. Jones, J. Fazekas and J. Foster University of Pittsburgh
2:05 PM	2:30 PM	<b>FPGA Implementation of the Massively Parallel GCA Model</b> W. Heenes, R. Hoffmann and S. Kanthak Tech. Univ. Darmstadt
2:30 PM	3:00 PM	<b>BREAK</b>
3:00 PM	3:25 PM	<b>Memory In Processor-Supercomputer On a Chip: Overcoming the Memory Wall to Achieve Massive On-Chip Parallelism</b> N. Venkateswaran, A. Shriraman and N. Soundararajan University of Rochester
3:25 PM	3:50 PM	<b>Stream PRAM</b> D. Ulm and M. Scherger University of Akron, Kent State University
3:50 PM	4:15 PM	<b>A Multiple Associative Model to Support Branches in Data Parallel Applications using the Manager-Worker Paradigm</b> W. Chantamas and J. Baker Kent State University
4:15 PM	5:00 PM	<b>Open Workshop Discussion and Planning for 2006</b>