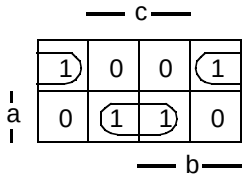
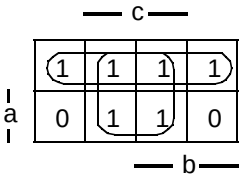
Homework #2 — Due 9/28/98

1. Find the minimized expression that corresponds to each of the following Karnaugh maps:

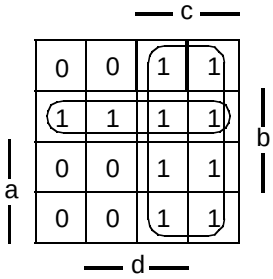


z = a'c' + ac



z = a' + c

2. Use a Karnaugh map to minimize the 4-variable Boolean expression
z = a'b + b'c + abc + abcd



z = a'b + c

Homework #2 — Due 9/28/98 (cont.)

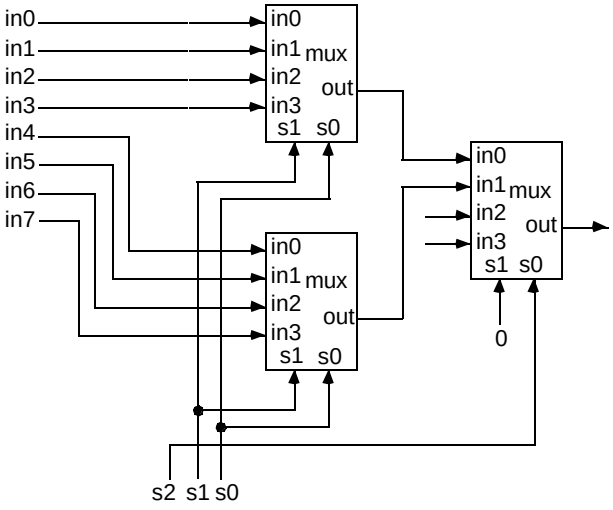
3. The register given on slide 10 of Lecture 08 is simpler than the register given on page 58 of the text. Explain how the two differ.

The one in the lecture "loads" when the load signal goes to the clock input of each D FF, whereas the one on page 58 "loads" when the clock is high and the tri-state devices let the input values through to the inputs of the D FFs.

Also, the one in the book can shift its value one position to the right. When the "load/shift" line is low, the output of each FF connects to the input of the FF to its right.

Homework #2 — Due 9/28/98 (cont.)

4. Show how an 8-input multiplexer (with inputs labeled i7 (msb) to i0 (lsb) can be constructed from 4-input multiplexers. Assume the lsb of the select line is labeled s0.



Homework #2 — Due 9/28/98 (cont.)

5. Can the Boolean expression (A' + B)(C + D') be implemented using a PLA? Explain your answer.

Yes. Using De Morgan's Law (see Lecture 05):

(A' + B)(C + D')
= (A' + B)' + (C + D')'
= AB' + C'D

This result is in sum-of-products form, and can be implemented directly by a PLA.