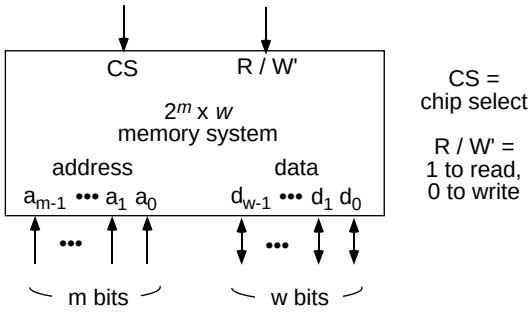
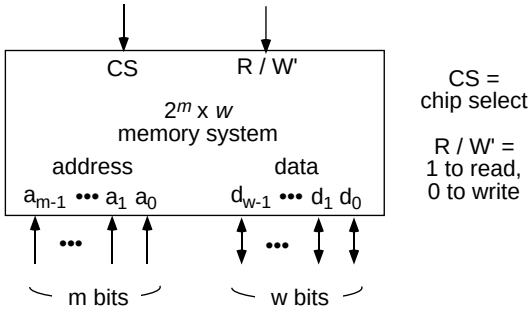
Interface to a Memory System



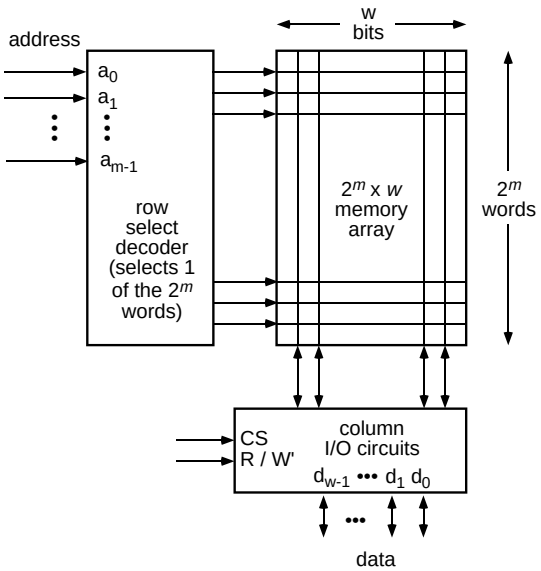
- Address lines — address of memory location to read or write
- Data lines — data read or written
- CS — chip select — if 1, turns the chip on; if 0, turns the chip off
- R/W' — read/write' — if 1, reads from the chip; if 0, writes to the chip
  - Assumed to generally be 0

Operation of a Memory System



- Assuming R/W' is generally low…
- A *read* operation works as follows:
  - Put address on address lines, raise R/W', raise CS, wait, get value from data lines, drop CS, drop R/W'
- A *write* operation works as follows:
  - Put address on address lines and data value on data lines, raise CS, wait, drop CS

2D Memory Organization



- Example: a 1K (1024 bit) chip might be organized as:
  - 64 16-bit words
  - 128 8-bit words

2D Memory Organization (cont.)

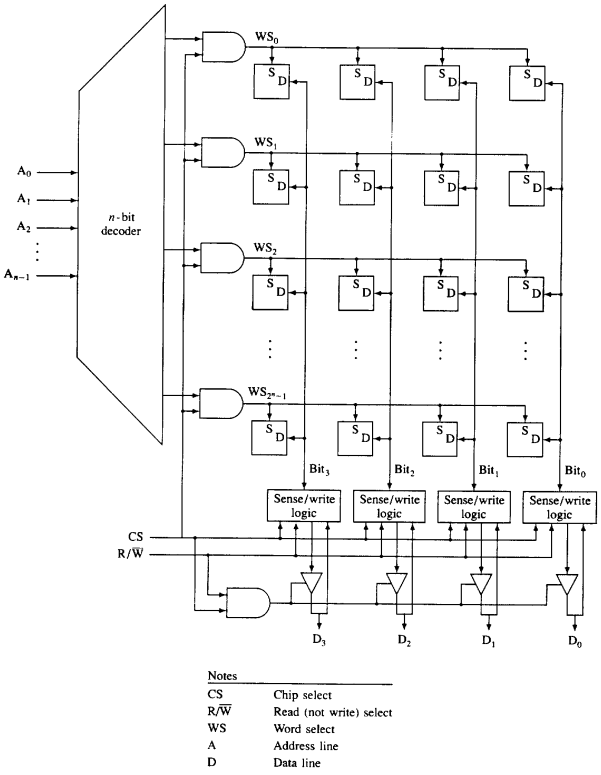
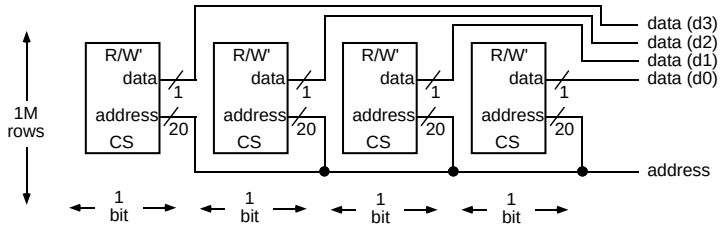


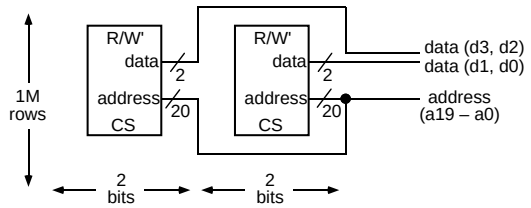
Diagram from *Computer Systems*, Maccabe, Irwin 1993

Building a Memory System

- Implement a 1M (2^{20}) x 4 bit memory system using:
  - 1M x 1 bit memory chips

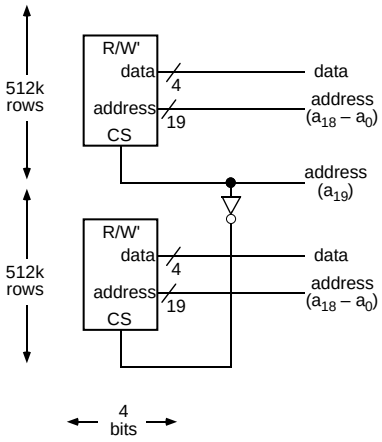


  - 1M x 2 bit memory chips



Building a Memory System (cont.)

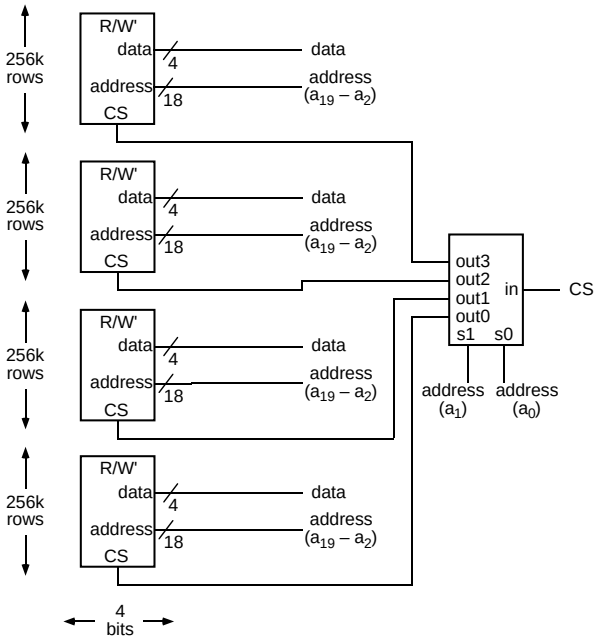
- Implement a 1M (2^{20}) x 4 bit memory system using:
  - 512k x 4 bit memory chips



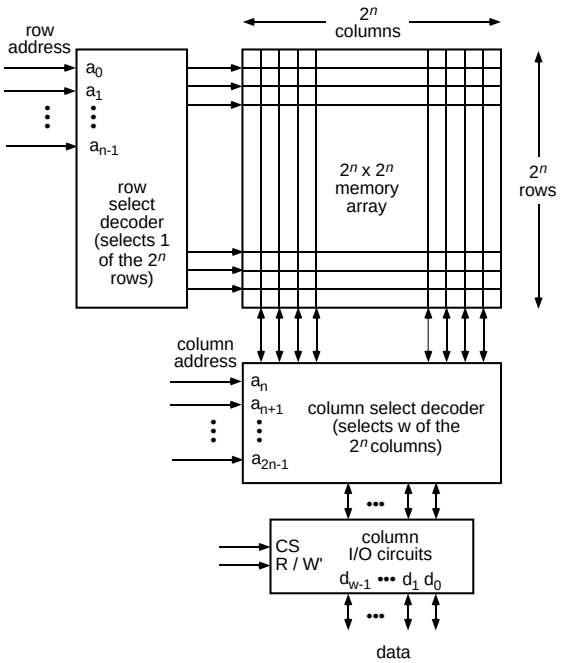
- Would there be any advantage to using a0 as chip select, instead of a19?

Building a Memory System (cont.)

- Implement a 1M (2^{20}) x 4 bit memory system using:
  - 256k x 4 bit memory chips



2 1/2 D Memory Organization



- Example: treat a 64 (2^6) x 64 bit chip as a 4096 (2^{12}) x 1 bit chip
  - Why not use a 4096 x 1 bit chip instead?

2 1/2 D Memory Organization (cont.)

- Improving memory access:
  - Fast page mode DRAM — send row1 address, column1 address, read data1, send column2 address, read data2
    - Faster access to data on same row (“page”) as previous access, since don’t have to send row address again
  - EDO DRAM — similar, but start sending column2 address while reading data1

Homework #3 — Due 10/12/98 (Part 1)

1. Draw a simplified block diagram for a 4M x 4 bit memory system using 2M x 1 bit memory chips