

Microcode for “ADD” Instruction

ifetch:

PC → MAR, READ word

while !MD

MDR → IR, inc PC

decode:

SHIFT **right** (#11, IR) → μBR

MAP μPC

add:

ALU and (#**15**, IR) → src2

SHIFT right (#4, IR) → temp2

ALU and (#**15**, temp2) → src1

SHIFT right (#4, temp2) → temp2

ALU and (#**15**, **temp2**) → dest

ALU add.cc (Reg[src1], Reg[src2]) → Reg[dest]

branch ifetch

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Writing a Microprogram in Microassembly Language

- A microprogram is written in a microassembly language, and stored in the control store (a ROM or PROM)
- Each microinstruction can (but does not have to) contain:
 - A label
 - Same as in assembly language programs
 - A control field
 - A “**while**” or “**if**” clause
 - An operation field
 - List of comma-separated *micro-operations*
 - A branch field
 - To implement branches

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Micro-Operation Grammar

<micro op> :: <memory op> | <reg op> | inc PC |
MAP μBR

<mem op> :: READ word | READ byte | WRITE word
| WRITE byte

<reg op> :: <bus 3 source> → <bus 3 dest> |
<bus 2 source> → MDR

<bus 3 source> :: <shift res> | <alu res> | MDR | PC

<bus 3 dest> :: μBR | IR | src2 | dest | Reg[dest] |
src1 | MAR | temp1 | temp2 | PC

<shift res> :: SHIFT (shift op) (<bus 1 source>, <bus
2 source>)

<shift op> :: left | right | right arith

<alu res> :: ALU <alu op> (<bus 1 source>, <bus 2
source>)

<alu op> :: add | sub | and | or | xor | xorn | add.cc |
sub.cc | and.cc | or.cc | xor.cc | xorn.cc

<bus 1 source> :: <constant> | Reg[src1] | temp1

<bus 2 source> :: IR | Reg[src2] | temp2 | PC

<constant> :: #n

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Hardwired vs. Microprogrammed Control

- Hardwired control
 - Simple to implement
 - Fast (no extra level of instruction fetching, decoding, etc.)
- Microprogrammed control
 - Flexible — easier for designer to modify (microcode is stored in ROM, which can be changed fairly easily)
 - Microcode is classified as *firmware* — in between software and hardware
 - Allows convenient hardware / software tradeoffs — what the hardware doesn't do (e.g., multiplication), do in microcode!
 - Supports families of machines with different price / performance tradeoffs
 - Provides support for very complex instructions

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