Where is Moore's Law Heading?

- Moore's Law (second version), attributed to Intel founder Gordon Moore, says:
  - The number of transistors on a chip will double every 18 months
- What about other characteristics?
  - According to the Semiconductor Research Corporation (details on next slide), the next 15 years will look like this:

Characteristic	1997	1999	2001	2003	2006	2009	2012
Process Technology (µm)	.250	.180	.150	.130	.100	.070	.050
Logic Tansistors (millions)	11	21	40	76	200	520	1400
Clock Speed (MHz)	750	1200	1400	1600	2000	2500	3000
Die Area (mm^2)	300	340	385	430	520	620	750
Wiring Levels	6	6–7	7	7	7–8	8–9	9

Semiconductor Industry Association (SIA)

- Semiconductor Industry Association, founded in 1977, is a trade association
- Some of SIA's wholly-owned subsidiaries:
  - Semiconductor Research Corporation (SRC) supports applied (academic) research in design and process technologies
  - Sematech, formed in 1987 as independent organization, now part of SIA, supports current needs in manufacturing (closely tied to industry)
  - Microelectronic Advanced Research Corporation (Marco), formed in 1997, supports revolutionary solutions to technical problems by developing Focus Centers to solve problems that will impact the industry in 10-15 years
    - 50% funded by SIA, 25% by Sematech members, 25% by government

SIA Roadmap

- Every few years (1992, 1994, 1997), the SIA publishes a "roadmap" for the semiconductor industry, charting industry trends for the next 15 years
  - "The National Technology Roadmap for Semiconductors" is online at http://notes.sematech.org/ntrs/Rdmpmem.nsf
    - 1997 version is latest
  - Estimates (hopefully) realistic targets
    - Example:
    - 0.25µm chips are in production (industry)
    - technology choices have been made for 0.18µm chips (Sematech)
    - several options need to be examined for 0.15µm chips (federal programs)
    - proof-of-concept being examined for 0.13µm chips (SRC & universities)
    - long-rang plans for 0.10µm chips (Marco)

Grand Challenges from 1997 Roadmap

- Affordable scaling
  - Historical 25-30% cost reduction due to design innovation, device shrinks, wafer size increase, yield improvement, equipment utilization improvement
    - Yields are near max
    - Biggest contribution is decreased feature size (means more transistors, faster chips)
  - Complexity is increasing, need new technologies and approaches
- Affordable lithography below 100µm
  - Ultraviolet lithography near physical limits
- New materials and structures
  - Below 100µm, logic and memory on same chip, copper interconnects…
- GHz frequency operation