Illiac IV History

- Major speedup alternatives:
  - Overlap (pipelining & buffering)
  - Multiprocessors
  - SIMD (duplicate the PE, not the CU)
    - Vector processor
- Three earlier designs (vacuum tubes and transistors) culminating in the Illiac IV design, all at the University of Illinois
  - Logical organization similar to the Solomon (prototyped by Westinghouse)
  - Sponsored by DARPA, built by various companies, assembled by Burroughs
  - Plan was for 256 PEs, in 4 quadrants of 64 PEs, but only one quadrant was built
  - Used at NASA Ames Research Center in mid-1970s

Illiac IV Architectural Overview

- One CU (control unit), 64 PEs (processing elements), each PE has a PEM (PE memory)
- CU operates on scalars, PEs on vectors
  - All PEs execute the instruction broadcast by the CU, if they are in active mode
  - Each PE can perform various arithmetic and logical instructions
  - Each PE has a 2048-word 64-bit memory, can be accessed in less than 350 ns
  - PEs can operate on data in 64-bit, 32-bit, and 8-bit formats
- Data can be routed between PEs in various ways
- I/O is handled by a separate Burroughs B6500 computer (stack architecture)

The Illiac IV Array

- Array = CU + processor array
- CU (Control Unit)
  - Controls the 64 PEs (vector operations)
  - Can also execute instructions (scalar ops)
  - 64 64-bit scratchpad registers
  - 4 64-bit accumulators
- PE (Processing Element)
  - 64 PEs, numbered 0 through 63
  - RGA = accumulator
  - RGB = for second operand
  - RGR = routing register, for communication
  - RGS = temporary storage
  - RGX = index register for instruction addrs.
  - RGD = indicates active or inactive state

The Illiac IV Array (cont.)

- PEM (PE Memory)
  - Each PE has a 2048-word 64-bit local random-access memory
  - PE 0 can only access PEM 0, etc.
- PU (Processing Unit) = PE + PEM
- Data paths
  - CU bus — 8 words of instructions or data can be fetched from a PEM and sent to the CU (instructions distributed in PEMs)
  - CDB (Common Data Bus) — broadcasts information from CU to all PEs
  - Routing network — PE *i* is connected to PE *i* -1, PE *i* +1, PE *i* -8, and PE *i* +8
    - Wraps around, data may require multiple transfers to reach its destination
  - Mode bit line — single line from RGD of each PE to the CU

Programming Issues

- Consider the following FORTRAN code:

```
      DO 10 I = 1, 64
10    A(I) = B(I) + C(I)
```

  - Put A(1), B(1), C(1) on PU 1, etc.
    - Each PE loads RGA from base+1, adds base+2, stores into base, where “base” is base of data in PEM
    - Each PE does this simultaneously, giving a speed up of 64
  - For less than 64 array elements, some processors will sit idle
  - For more than 64 array elements, some processors might have to do more work
- For some algorithms, it may be desirable to turn off PEs
  - 64 PEs compute, then one half passes data to other half, then 32 PEs compute, etc.

Illiac IV I/O System

- I/O system = I/O subsystem, DFS, and a B6500 control computer
- I/O subsystem
  - CDC (Control Descriptor Controller) — interrupts the B6500 upon request by the CU, also loads programs and data from the DFS into the PEM array
  - BIOM (Buffer I/O Memory) — buffers (much faster) data from DFS to CPU
  - IOS (I/O Switch) — selects input from DFS vs. real-time data
- DFS (Disk File System?)
  - 1 Gbit, 128 heads (one per track)
  - 2 channels, each of which can transmit or receive data at 0.5 Gb/s over a 256-bit bus (1 Gb/s using both channels)

Illiac IV I/O System (cont.)

- B6500 control computer
  - CPU, memory, peripherals (card reader, card punch, line printer, 4 magnetic tape units, 2 disk files, console printer, and keyboard)
  - Manages requests for system resources
  - OS, compilers, and assemblers
  - Laser memory
    - 1 Tbit write-once read-only laser memory
    - Thin film of metal on a polyester sheet, on a rotating drum
    - 5 seconds to access random data
  - ARPA network link
    - High-speed network (50 Kbps)
    - Illiac IV system was a network resource available to other members of the ARPA network

Illiac IV Software

- Illiac IV delivered to NASA Ames Research Center in 1972, operational sometime (?) after mid -1975
  - Eventually operated M–F, 60-80 hours of uptime, 44 hours of maintenance / downtime
- No real OS, no shared use of Illiac IV, one user at a time
  - An OS and two languages (TRANQUIL & GLYPNIR) were written at Illinois
  - At NASA Ames, since PDP-10 and PDP-11 computers were used in place of the B6500, new software was needed, and a new language called CFD was written for solving differential equations