## Midterm Exam

## VLSI Design

## Friday 17 October 2003

1. The cost for an individual FPGA containing 30,000 gates may be an order of magnitude more than the part cost of an ASIC of the same size, yet FPGA-based designs are usually considered more cost-effective for designs with a volume of tens or hundreds of thousands of units. Explain. ( 25 points)
2. The Altera UP1 Education Board is a good way to test simple designs, but you have to understand how the various components work and how they are integrated onto the board.
a. What does it mean to say the pushbuttons are "active low"? (10 points)
b. Explain the procedure for assigning pins when using one of the pushbuttons with the FLEX chip and why this procedure is necessary. (10 points)
3. Given the two 4-variable Karnaugh maps below, circle the 1 's and write the minimized expression below each map. ( 20 points)

4. Consider the following AHDL code:
```
SUBDESIGN bool2
{
        a0, b0, a1, b1: INPUT;
        s1: OUTPUT;
}
VARIABLE
    inter: NODE;
BEGIN
    inter = a0 & a1 & !b1;
    s1 = inter # b0;
END;
```

a. Draw a schematic diagram that corresponds to this code. (10 points)
b. What would the effect be of interchanging the two lines inside the "BEGIN" / "END" block? Explain. (10 points)

Name:
5. Given the following AHDL code, explain how this code "debounces" a pushbutton. What happens when the key is not pressed? What happens when the key is pressed? Refer to parts of the code and be specific in your answer. (15 points)

```
SUBDESIGN debounce
{
    clk, key_pressed: INPUT;
    strobe: OUTPUT;
}
VARIABLE
    count[6..0]: DFF;
BEGIN
    count[].clk = clk;
    count[].clrn = key_pressed;
    IF (count[].q <= 126) & key_pressed THEN
        count[].d = count[].q+1;
    IF count[].q == 126 THEN
        strobe = Vcc;
    ELSE
        strobe = GND;
    END IF;
END;
```

