Name: _____

CS 4/55111   # Final Exam   **VLSI Design**

Wednesday 10 December 2003

1. FPGAs can be programmed using antifuses, EEPROMs, or static RAM (SRAM).

    a. How do these three technologies compare in terms of the size of the programming elements on the FPGA? (5 points)

    b. Which programming technologies are used by the two FPGAs on the Altera boards in the VLSI Design Lab? (10 points)

2. Many FPGAs, such as Actel's ACT and Xilinx's XC4000, have tracks of various lengths — some span only a channel or two, some are longer, and some span the entire chip. Why are all these different sizes needed? Be specific. (10 points)
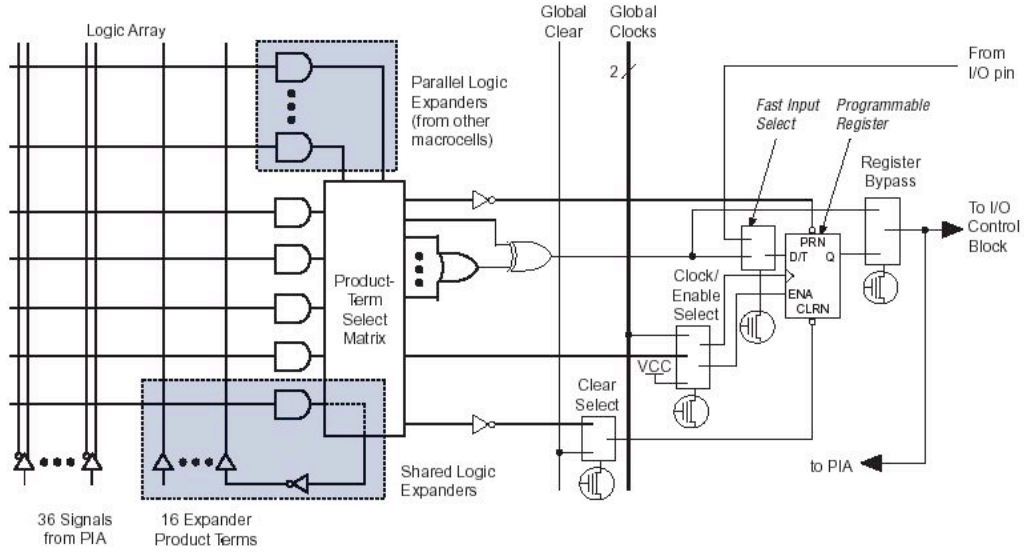
3. Consider the Altera MAX 7000 macrocell, illustrated in the figure below:

a. What does the Product Term Selection Matrix do? (8 points)

b. What functionality is provided by the Parallel Logic Expanders? (7 points)

c. What options are available for setting and clearing (as opposed to simply loading a value into) the D/T register shown on the right? (5 points)

4. Consider the Altera FLEX 10k Logic Array Block, illustrated in the figure below:
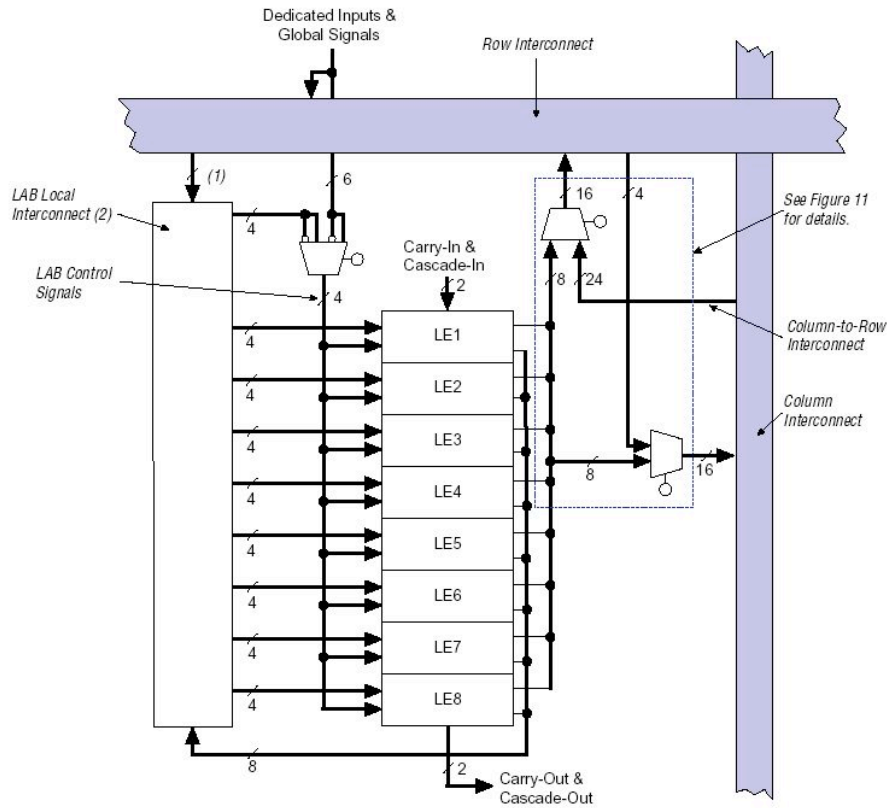
a. What is the point of grouping a number of LEs together into a Logic Array Block like this, instead of treating each one separately? (8 points)

b. What is the functionality of the multiplexors in the rectangle at the upper right (the one labeled "See Figure 11 for details")? (7 points)

5. What functionality is provided by the Embedded Array Blocks (EABs) in the Altera FLEX 10k FPGAs? (10 points)

6. ICs are built on a silicon wafer; how is that wafer produced? (5 points)

7. Consider the VHDL process below. What is the function of the first line of code ("PROCESS (Reset, Clock)"), and how does that functionality interact with the rest of the code? Be specific. (10 points)

```
PROCESS (Reset, Clock)
BEGIN
    IF Reset = '1' THEN
        Q3 <= '0';
    ELSEIF ( Clock'EVENT AND Clock = '1' ) THEN
        Q3 <= D;
    END IF;
END PROCESS;
```

8. Describe some of the differences between AHDL and VHDL. (15 points)