Name: _____

CS 4/55111 **Final Exam** **VLSI Design**

Wednesday 10 December 2003

1. **FPGAs can be programmed using antifuses, EEPROMs, or static RAM (SRAM).**

   a. **How do these three technologies compare in terms of the size of the programming elements on the FPGA? (5 points)**

   Antifuses are smaller than a transistor, about the size of a via.
   EPROM programming points are about the size of a transistor (transistor plus extra gate).
   SRAM programming points are the size of a memory bit, requiring 4-6 transistors.

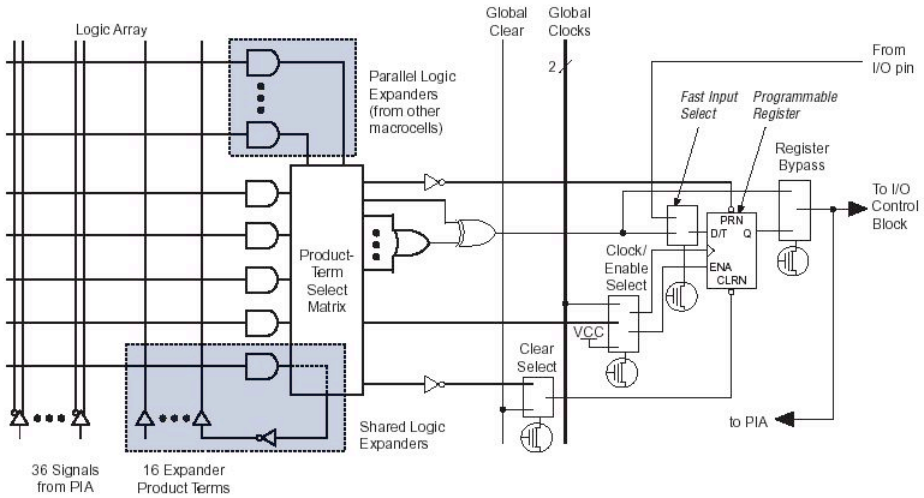
   b. **Which programming technologies are used by the two FPGAs on the Altera boards in the VLSI Design Lab? (10 points)**

   The MAX 7128 uses EEPROM programming; the FLEX 10K20 uses SRAM programming.

2. **Many FPGAs, such as Actel's ACT and Xilinx's XC4000, have tracks of vaxrious lengths — some span only a channel or two, some are longer, and some span the entire chip. Why are all these different sizes needed? Be specific. (10 points)**

   Long tracks are used to communicate between widely separated components. Short tracks are used to communicate between components in adjacent rows / columns, but also permit each channel to be used for multiple tracks (which is more efficient than allocating an entire channel for each short track).

3. **Consider the Altera MAX 7000 macrocell, illustrated in the figure below:**



Name: _____

a. What does the Product Term Selection Matrix do? (8 points)

The Product Term Selection Matrix selects product terms from the 5 AND gates that process the 26 inputs from the PIA, or product terms from the Parallel Logic Expanders or Shared Logic Expanders, and sends those product terms as appropriate to the OR gate (to produce a Sum of Products Boolean equation) or to the elements on the right side of the figure, providing register clear, present, clock, and clock enable.

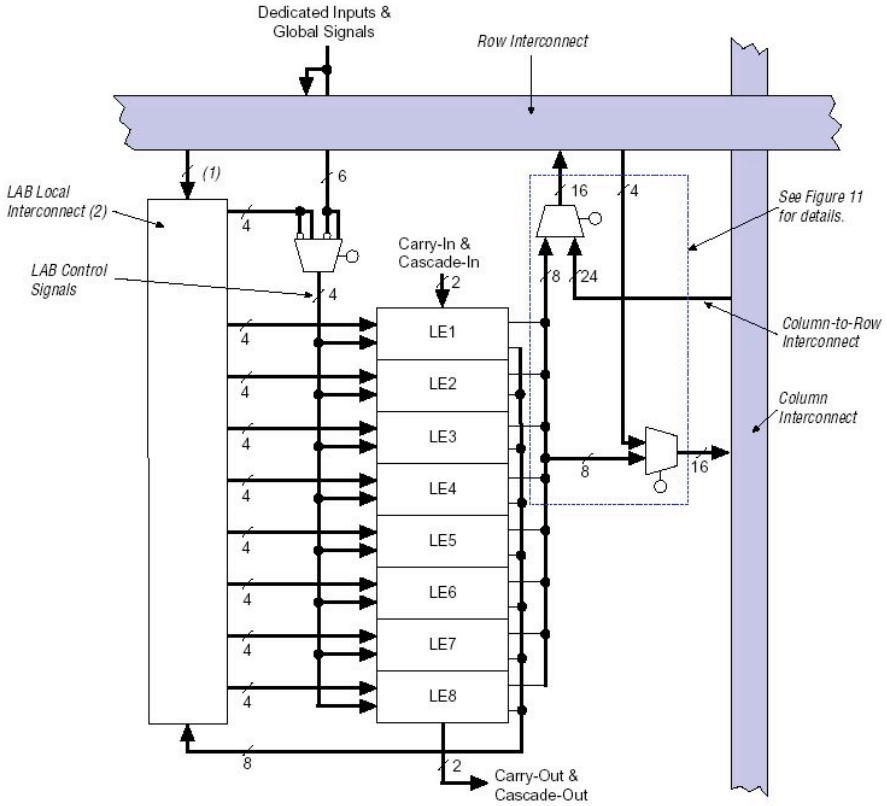
b. What functionality is provided by the Parallel Logic Expanders? (7 points)

They allow product terms from one macrocell to be sent to the Product Term Selection Matrix of other macrocells in the same LAB (subject to certain restrictions), in effect allowing one macrocell to "borrow" product terms from adjacent macrocells.

c. What options are available for setting and clearing (as opposed to simply loading a value into) the D/T register shown on the right? (5 points)

The Product Term Selection Matrix can select a product term to set the register (the "PRN" input) or clear the register (the "CLRN" input). The register can also be cleared by the Global Clear signal.

4. Consider the Altera FLEX 10k Logic Array Block, illustrated in the figure below:



a. What is the point of grouping a number of LEs together into a Logic Array Block like this, instead of treating each one separately? (8 points)

LEs in a LAB can communicate though the LAB Local Interconnect, which is faster than communicating between LABs using the FastTrack row and column interconnect. In addition, LEs in a LAB can be connected into carry and cascade chains to facilitate fast arithmetic. Finally, LEs in a LAB can share product terms through the Parallel Logic Expanders and Shared Logic Expanders.

b. What is the functionality of the multiplexors in the rectangle at the upper right (the one labeled "See Figure 11 for details")? (7 points)

They send the outputs of the LEs to either the FastTrack Interconnect rows or columns. In addition, they allow values to be transferred from a row to a column or vice-versa.

5. What functionality is provided by the Embedded Array Blocks (EABs) in the Altera FLEX 10k FPGAs? (10 points)

The EAB is basically a large RAM with registers on the input and output ports. It can be used as a memory (RAM, ROM, dual-port RAM, or FIFOs of various sizes) or as a very large lookup table (LUT) — ideal for multipliers or other complex combinational circuits.

6. ICs are built on a silicon wafer; how is that wafer produced? (5 points)

Silicon is melted in a quartz crucible in a helium or argon atmosphere, and then a single crystal on the end of a probe is inserted into the molten silicon and slowly drawn out while being rotated. This process results in a single-crystal cylinder, which is then sawed into wafers. The wafers are polished on one side, and are then ready for IC fabrication.

7. Consider the VHDL process below. What is the function of the first line of code ("PROCESS (Reset, Clock)"), and how does that functionality interact with the rest of the code? Be specific. (10 points)

```
PROCESS (Reset, Clock)
BEGIN
    IF Reset = '1' THEN
        Q3 <= '0';
    ELSEIF ( Clock'EVENT AND Clock = '1' ) THEN
        Q3 <= D;
    END IF;
END PROCESS;
```

It says that this code is a process, meaning the function is executed concurrently with other VHDL functions, but its contents should be executed sequentially. In addition, it declares the function to be sensitive to changes in Reset and Clock, meaning that the function is reevaluated whenever the values of Reset or Clock change.

8. Describe some of the differences between AHDL and VHDL. (15 points)

Many answers possible.