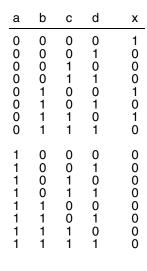
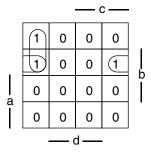
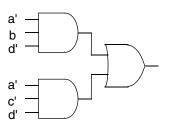
Implementing a Truth Table Using An And-Or Structure (Review)

 Given a truth table, we can use a Karnaugh map to find the minimum 2level SOP implementation







x = a'bd' + a'c'd'

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PLAs

- A 2-level *and-or* structure is replicated many times in a <u>programmable</u> array called a *PLA* (*programmable logic array*)
 - Parts of a CPU's datapath or next-state logic can be built out of PLAs
 - Small circuits can be built out of PLAs
- At the input of each gate, there's a "fuse" which can be left whole, or broken
 - So the designer can control which inputs go to each and gate, and which outputs of the and gates go to each or gate
- A PLA can be either
 - Mask programmable customer orders a programmed PLA from the manufacturer
 - Field programmable customer can program PLA (once)

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PLAs

■ A 2-level *and-or* structure is replicated many times in a <u>programmable</u> array called a *PLA* (*programmable logic array*)

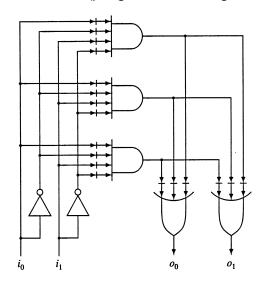


Diagram from Computer Systems, Maccabe, Irwin 1993

 This PLA has 2 inputs, 2 outputs, and can represent up to 3 product terms

PLA Example

■ This is an *abstract* diagram of a PLA with 6 inputs, 4 outputs, which can represent up to 12 product terms

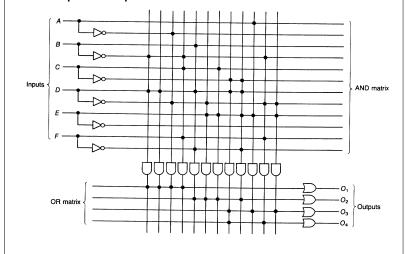


Diagram from Digital Design, Johnson & Karim, PWS-Kent 1987

Try the Java KMap->PLA animation at http://tech-www.informatik.unihamburg.de/applets/kvd

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Field-Programmable Logic Device

- The next evolutionary step beyond the PLA is the *field-programmable logic device* (FPLD), also called the:
 - Field-programmable gate array (FPGA)
 - Complex programmable logic device (CPLD)
- FPLD characteristics
 - Based on either an array of PLA-like andor structures, or on look-up tables
 - Usually includes connections from these structures to 4 nearest neighbors
 - May include long connections across chip
 - May include D (or more complex) flipflops, to more easily build sequential circuits, possibly even RAM
 - Many can be "programmed" repeatedly
 - Available in different sizes up to 500,000 gates (100MHz, 2.5 volt, 0.25μ, 5 metal)

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Programming Using Antifuses

- An antifuse is normally open ("off"); when enough current (5–15mA) passes through it it closes ("on")
 - Current melts a thin insulating dielectric and forms a permanent silicon link
 - Disadvantage can only program once
 - Programmed in a special hardware device
 - An antifuse FPLD may contain 750,000 antifuses, but only about 2% of them typically need to be programmed
 - Takes about 5-10 minutes for each chip
- Advantages:
 - Small about the size of a via
 - Low resistance, low capacitance = fast
- Antifuses can be used in FPLDs to:
 - Connect inputs to cells
 - Connect cells to interconnect

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Programming Using EPROMs & EEPROMs (Floating Gates)

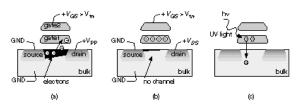


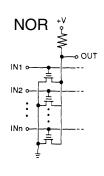
Figure from Application-Specific Integrated Circuits, Smith, Addison-Wesley, 1997

■ EPROM programming & operation:

- To program: a high (>12V) programming voltage V_{PP} is applied to the drain, causing electrons to "jump" onto the floating gate (gate1)
 - The electrons on gate1 raise the threshold voltage V_t enough that the programmed transistor is always off
- To erase: the transistor is exposed to UV light, which provides enough energy for the electrons stuck on gate1 to jump back onto the bulk, returning the transistor to normal operation
- Can be reprogrammed many times

Programming Using EPROMS & EEPROMs (Floating Gates) (cont.)

- EEPROMs are similar, but are erased electrically
 - Faster to erase than EPROM, and can be done "in-circuit"
 - Requires larger cell than EPROM
- Advantages
 - Can be programmed repeatedly, in-circuit
 - Fairly small requires only 1 transistor
- Can be used in FPLDs to:
 - Connect inputs to cells
 - In NOR gate, when transistor is programmed (disabled), an input of 1 can not pull output down to VSS
 - Connect cells to interconnect

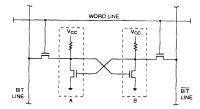


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Programming Using Static RAMs (SRAMs)

Five Transistor RAM Cell WORD LINE WORD LINE A B X3713

Four Transistor RAM Cell



Six Transistor RAM Cell

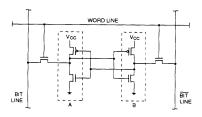


Figure from Field-Programmable Gate Array Technology, Trimberger, Kluwer, 1994

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Programming Using Static RAMs (SRAMs) (cont.)

■ Disadvantages:

- Must load configuration from ROM, disk, etc. on power-up
- Large requires several transistors

Advantages:

- Can be programmed repeatedly, in-circuit
 Can be programmed quickly (< 1ms)
- Part has been 100% tested at factory
- Same basic process as CMOS, so quickly takes advantage of new fab processes
 - CMOS also requires less power than circuits requiring pull-up resistors

■ SRAMs can be used in FPLDs to :

- Connect inputs to cells, or even to replace the cell if it's a LUT
- Connect cells to interconnect

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