Altera FLEX 8000 Block Diagram

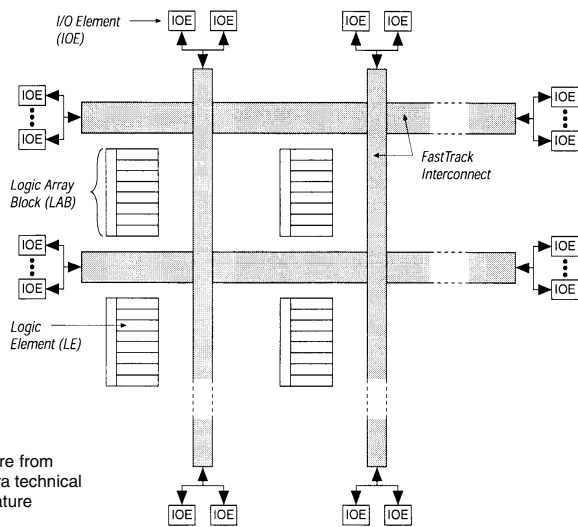

Figure from Altera technical literature

■ FLEX 8000 chip contains 26–162 LABs

  ● Each LAB contains 8 Logic Elements (LEs), so a chip contains 208–1296 LEs, totaling 2,500–16,000 usable gates

  ● LABs arranged in rows and columns, connected by FastTrack Interconnect, with I/O elements (IOEs) at the edges
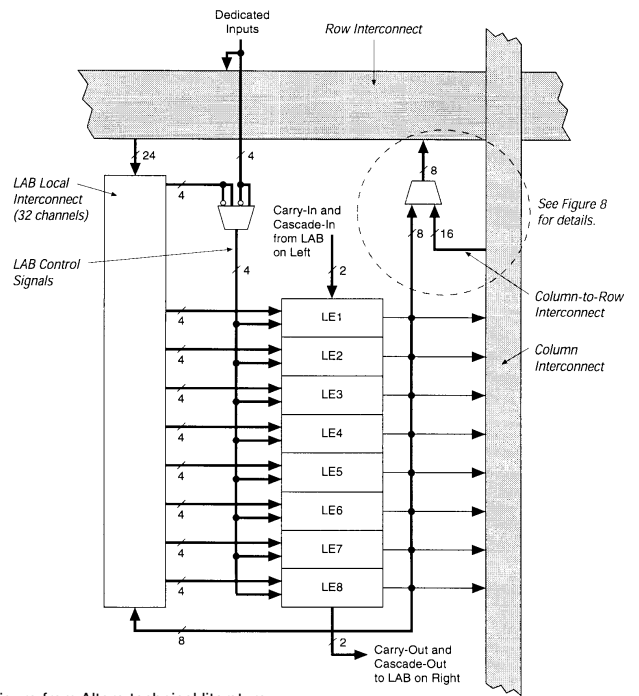
Altera FLEX 8000 Logic Array Block

Figure from Altera technical literature

■ LAB = 8 LEs, plus local interconnect, control signals, carry & cascade chains
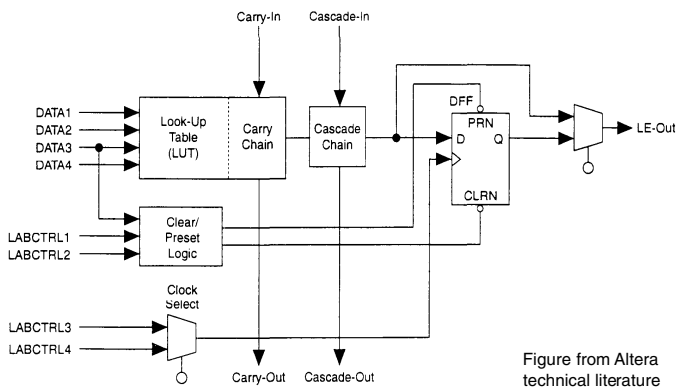
Altera FLEX 8000 Logic Element

Figure from Altera technical literature

■ Each Logic Element (LE) contains:

  ● 4-input Look-Up Table (LUT)
    ■ Can produce any function of 4 variables

  ● Programmable flip-flop
    ■ Can configure as D, T, JR, SR, or bypass
    ■ Has clock, clear, and preset signals that can come from dedicated inputs, I/O pins, or other LEs

  ● Carry chain & cascade chain

Altera FLEX 8000 Carry Chain
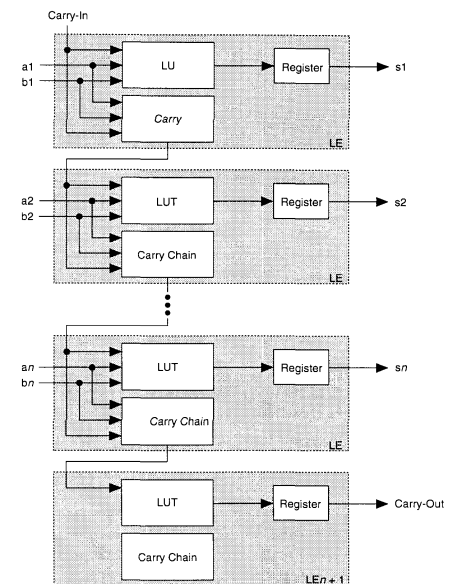# (Example: n-bit adder)

Figure from Altera technical literature

■ *Carry chain* provides very fast (< 1ns) carry-forward between LEs

  ● Feeds both LUT and next part of chain

  ● Good for high-speed adders & counters

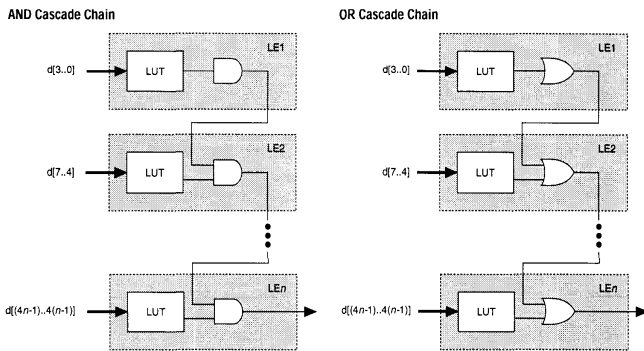# Altera FLEX 8000 Cascade Chain

AND Cascade Chain

OR Cascade Chain

Figure from Altera technical literature

- *Cascade chain* provides wide fan-in

  - Adjacent LE's LUTs can compute parts of the function in parallel; cascade chain then serially connects intermediate values

  - Can use either a logical AND or a logical OR (using DeMorgan's theorem) to connect outputs of adjacent LEs

  - Each additional LE provides 4 more inputs to the width of the function
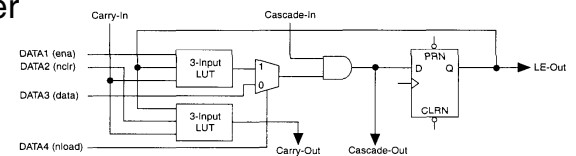
Altera FLEX 8000 LE Operating Modes

Normal
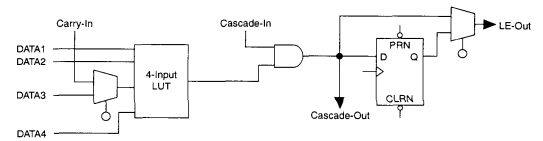
Arithmetic
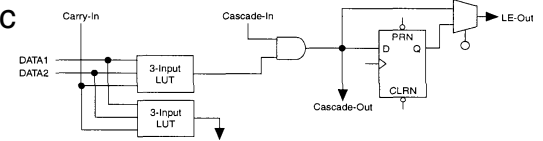
Up/down Counter

Figure from Altera technical literature

- Each mode uses LE resources differently

  - 7 out of 10 inputs (4 data from LAB local interconnect, feedback from register, and carry-in & cascade-in) go to specific destinations to implement the function

  - Remaining 3 provide clock, clear, and preset for register

Altera FLEX 8000 Operating Modes (cont.)

- Normal mode

  - Used for general logic applications, and wide decoding functions that can benefit from the cascade chain

- Arithmetic mode

  - Provides two 3-input LUTs to implement adders, accumulators, and comparators
    - One LUT provides a 3-bit function
    - Other LUT generates a carry bit

- Up/down counter mode

  - Provides counter enable, synchronous up / down control, and data loading options

  - Uses two 3-input LUTs
    - One LUT generates counter data
    - Other LUT generates fast carry bit
    - Use 2-to-1 multiplexer for synchronous data loading, clear and preset for asynchronous data loading
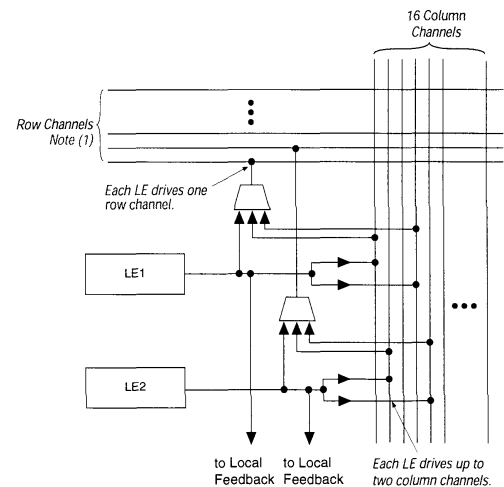
Altera FLEX 8000 FastTrack Interconnect

Figure from Altera technical literature

Note:
(1) See Table 4 for the number of row channels.

- Device-wide rows and columns

  - Each LE in LAB drives 2 column (total 16) channels, which connects… that column

  - Each LE in LAB drives 1 row channel, which connects to other LABs in that row

    - 3-to-1 muxs connect either LE outputs or column channels to row channels
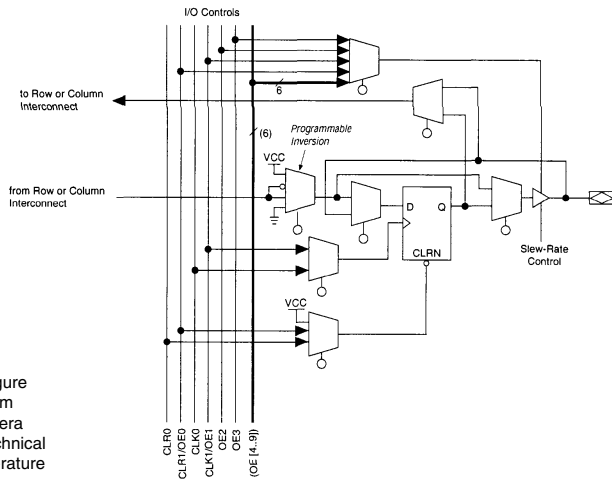
Altera FLEX 8000 I/O Elements

I/O Controls

to Row or Column Interconnect

from Row or Column Interconnect

6

(6) *Programmable Inversion*

VCC

D   Q

CLRN

VCC

Slew-Rate Control

Figure from Altera technical literature

CLR0
CLR1/OE0
CLK0
CLK1/OE1
OE2
OE3
(OE [4..9])

■ Eight I/O Elements (IOEs) are at the end of each row and column

● Some restrictions on how many row / column channels each IOE connects to

● Contains a register that can be used for either input or output

■ Associated I/O pins can be used as either input, output, or bidirectional pins

Altera FLEX 8000 Configuration

■ Loading the FLEX 8000's SRAM with programming information is called *configuration*, and takes about 100ms

● After configuration, the device initializes itself (resets its registers, enables its I/O pins, and begins normal operation)

● Configuration & initialization = command mode, normal operation = user mode

■ Six configuration schemes are available:

● Active serial — FLEX gives configuration EPROM clock signals (not addresses), keeps getting new values in sequence

● Active parallel up, active parallel down — FLEX 8000 gives configuration EPROM sequence of addresses to read data from

● Passive parallel synchronous, passive parallel asynchronous, passive serial — passively receives data from some host