CS 4/55111 **VLSI Design**

Project #4

Due to Prof. Walker by 5pm on Friday 21 November 2003
this project counts as 15% of your course grade

Implement a 4-bit ripple-carry adder in AHDL, implement a 4-bit carry-look-ahead adder in AHDL, simulate each adder so that it runs as fast as possible on an Altera FLEX EPF10K20RC240-4, and compare the performance of the two adders. Then modify the two designs so that you can download them onto the FLEX chip on a UP1 board, take two 4-bit inputs from a DIP switch, and display the output from each adder on a 7-segment display.

Ripple-carry adders and carry-look-ahead adders are described in the handout from *Principles of Digital Design*, by Daniel D. Gajski, Prentice-Hall, 1997.

Note that this project counts more than the previous projects (15% of your course grade versus 10%), and that the documentation makes up a significant portion of your grade on this project.

Turn in:

a) a document that describes your design and any design decisions that you made (10 points)

b) a readable (not microscopic) printout of the AHDL code and any schematics (5 points)

c) a printout of the test inputs and simulation output that shows that that each adder works as expected (just simulate the adders, not the DIP switches or 7-segment displays), annotated to explain the operation of the circuit (25 points)

d) a comparison of the performance of the two adders (20 points)

e) a signature on the statement below by Prof. Walker, by the TA (Ping Xu), by one of Prof. Walker's research students (Kevin Schaffer, Meiduo Wu, or Hong Wang), or by ***two*** other students in the class (40 points):

I certify that _____ has successfully downloaded this design to a UP1 board and the design works correctly.

_____ Name _____ Date

_____ Name _____ Date