



Name: \_\_\_\_\_

2. The Actel ACT, like many FPLDs, has specific constraints on the use of horizontal and vertical channels. In the case of the ACT, cell inputs must come from one of the two adjacent horizontal tracks, while cell outputs connect to dedicated vertical tracks called “output stubs”. Why constrain the cell I/O like this, instead of being more flexible? (10 points)

3. What is the biggest difference, in terms of architecture, between the Altera FLEX 8k, Altera FLEX 10k, and Altera APEX families? (15 points)

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4. What is the Altera FLEX family's "carry chain" used for? (5 points)
5. Explain the process of constructing a wafer for use in chip fabrication. (10 points)
6. Why is the production of cell-based ASIC design so much more expensive than a FPGA-based design, except when a very large volume of the design is produced? Be specific. (10 points)

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7. Consider the two VHDL processes below. How do they differ in terms of functionality? Be specific. (15 points)

```
PROCESS
BEGIN
    WAIT UNTIL ( Clock'EVENT AND Clock = '1' );
    IF Reset = '1' THEN
        Q2 <= '0';
    ELSE
        Q2 <= D;
    END IF;
END PROCESS;
```

```
PROCESS (Reset, Clock)
BEGIN
    IF Reset = '1' THEN
        Q3 <= '0';
    ELSEIF ( Clock'EVENT AND Clock = '1' ) THEN
        Q3 <= D;
    END IF;
END PROCESS;
```

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8. AHDL and VHDL are hardware description languages, with many features in common. However, each language has some features that the other is missing, which may occasionally make it a better choice for implementing a design. Describe some situations when each language is more appropriate than the other. (15 points)