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CS 4/55111 **Final Exam** VLSI Design

Monday 13 December 2004

1. **Compared to ASICs, FPLDs have the distinct advantage of programmability, possibly even reprogramability.**

   a. **Where is this programmability used in the FPGA — i.e., just what can be programmed? (10 points)**

      Programming points are used in the FPGA to control the functionality of the macrocells/LEs, to control the cell's connection to interconnect, to control the interconnection of rows and columns, and to control the functionality and connection of I/O pins. For FPGAs supporting memory, the initial contents of those memories can also be programmed.

   b. **In an FPLD, SRAM programming is more flexible than either EPROM or antifuse programming, but requires more chip area for each programming point. Explain. (10 points)**

      SRAM is very flexible because the chip can be reprogrammed repeatedly and quickly. EPROM-based chips can also be reprogrammed repeatedly, but this process is slower. Antifuse-based chips can not be reprogrammed.

      SRAM programming points are the largest, as each requires 4-6 transistors (one memory cell). EPROM programming points are about the size of a gate, and thus are smaller, and antifuse programming points are about the size of a via, and thus are the smallest.

2. **The Actel ACT, like many FPLDs, has specific constraints on the use of horizontal and vertical channels. In the case of the ACT, cell inputs must come from one of the two adjacent horizontal tracks, while cell outputs connect to dedicated vertical tracks called "output stubs". Why constrain the cell I/O like this, instead of being more flexible? (10 points)**

   Allowing more flexibility would have two negative effects. First, the additional programming points would require more area, decreasing the area available on the chip for logic cells. Second, the additional flexibility means more choices, so compile time would be longer.

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3. What is the biggest difference, in terms of architecture, between the Altera FLEX 8k, Altera FLEX 10k, and Altera APEX families? (15 points)

In addition to the LABs/LEs in the FLEX 8k, the FLEX 10k adds one Embedded Array Block (EAB) per row, which can be used to implement various kinds of memories. The APEX adds yet more memories, configuring the chip into MegaLAB structures, each with LABs and ESBs (Embedded System Blocks); these ESBs can be configured as memories or as very large lookup tables. In addition, each family supports larger chips than the family before it.

4. What is the Altera FLEX family's "carry chain" used for? (5 points)

In multi-bit arithmetic operations, the carry chain allows a carry out from one bit to connect to the carry in for the next bit. It supports fast arithmetic operations, without need for carry lookahead or other more complex techniques.

5. Explain the process of constructing a wafer for use in chip fabrication. (10 points)

Silicon is melted in a quartz crucible in a helium or argon atmosphere, and then a single crystal on the end of a probe is inserted into the molten silicon and slowly drawn out while being rotated. This process results in a single-crystal cylinder, which is then sawed into wafers. The wafers are polished on one side, and are then ready for IC fabrication.

6. Why is the production of cell-based ASIC design so much more expensive than a FPGA-based design, except when a very large volume of the design is produced? Be specific. (10 points)

In ASICs, the fixed costs are very high — design software is expensive, and expensive masks must be created. The variable costs per part are lower than for FPGAs, but the fixed costs are so high that very large volumes are required to overcome those fixed costs.

7. Consider the two VHDL processes below. How do they differ in terms of functionality? Be specific. (15 points)

```
PROCESS
BEGIN
    WAIT UNTIL ( Clock'EVENT AND Clock = '1' );
        IF Reset = '1' THEN
            Q2 <= '0';
        ELSE
            Q2 <= D;
        END IF;
```

```
END PROCESS;
```

This process is constantly active, waiting for a rising edge of the clock. When that rising edge occurs, if the reset line is high, it stores and outputs 0; otherwise it stores and outputs the D input.

```
PROCESS (Reset, Clock)
BEGIN
    IF Reset = '1' THEN
        Q3 <= '0';
    ELSEIF ( Clock'EVENT AND Clock = '1' ) THEN
        Q3 <= D;
    END IF;
END PROCESS;
```

This process becomes active whenever Reset or Clock changes. When that happens, if the reset line is high, it stores and outputs 0. Otherwise, if there has been a rising edge of the clock, it stores and outputs the D input.

8. AHDL and VHDL are hardware description languages, with many features in common. However, each language has some features that the other is missing, which may occasionally make it a better choice for implementing a design. Describe some situations when each language is more appropriate than the other. (15 points)

Many answers possible…