

# Integrated Circuits (ICs)

- Integrated Circuit (IC) = “chip”
  - General-purpose microprocessor, CPU
  - Application-Specific Instruction Set Processor (ASIP), e.g. video processor or digital signal processor
  - Application-Specific IC (ASIC) or Field-Programmable Logic Device (FPLD)
- IC package contains:
  - silicon chip = “die”
  - Pins, wires between die and pins

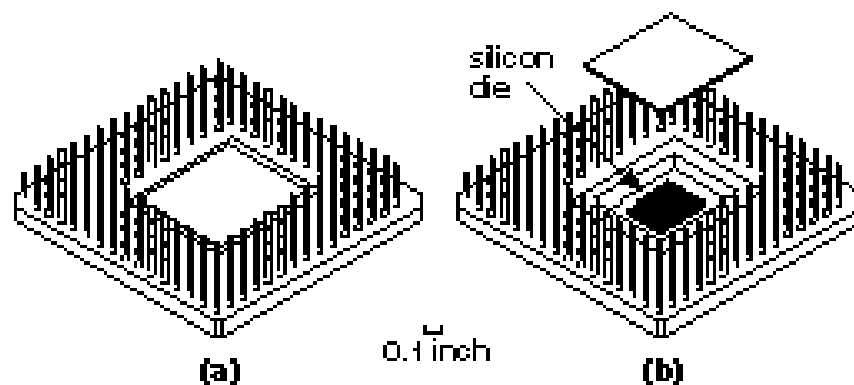


Figure from *Application-Specific Integrated Circuits*, Smith, Addison-Wesley, 1997

- Package may have heat sink attached

# Some Applications of ICs

## ■ Home

- Appliances, intercom, telephones, security system, garage door opener, answering machines, fax machines, home computers, TVs, cable TV tuner, VCR, camcorder, video games, cellular phones, sewing machines, cameras, exercise equipment, microwave oven

## ■ Office

- Telephones, computers, security system, fax machines, copier, printers, pagers

## ■ Automobile

- Trip computer, air bags, ABS, instrumentation, security system, transmission control, entertainment system, climate control, keyless entry, cellular phone, GPS

List from *Hardware/Software Codesign*, Giovanni De Micheli, 1996.

# Integrated Circuits (ICs) (cont.)

- A modern digital system is built out of a collection of integrated circuits (ICs), each of which is made up of gates
  
- ICs are typically classified based on the number of gates they contain
  - SSI (small scale integration) < 10
    - 4 nand gates
    - 4 or gates
    - 4 and gates
  
  - MSI (medium...) 10-100
    - simple adders, counters
    - multiplexers
    - flip-flops
  
  - LSI (large...) 100-10,000
    - Interface devices
    - Calculators
    - Digital clocks
    - Simple microprocessors

# Integrated Circuits (ICs) (cont.)

## ■ Classification, cont.

### ● VLSI (very large...) >10,000

#### ■ Modern microprocessors

- 8086 = 29,000
- i386DX = 275,000
- i486DX = 1,200,000
- Pentium = 3,100,000
- Pentium Pro = 5,500,000
- Pentium II = 7,500,000

- Pentium M = 77,000,000  
(half are for the L2 cache)

#### ■ Application-Specific Instruction Set Processor (ASIP), e.g. video processor or digital signal processor

#### ■ Application-Specific IC (ASIC)

- Generally cost-effective only when produced in high volume (hundreds of thousands of part)
- Also used when very high performance is needed

#### ■ Field-Programmable Logic Device (FPLD)

- Very common, 80,000 new design starts in 2003 (vs. 4,000 for ASICs)

# ASICs vs. FPLDs

- IC contains a *chip* (“die”) cut from a *wafer*
  - Transistors, wires, etc. are built up on the chip in a series of *layers* (10-50 layers)
  - A *mask* is used to define the components of a layer as they are applied to the chip
  
- ASICs vs. FPLDs (+ pizza equivalent)
  - Full-custom ASIC
    - Prepare pizza sauce, toppings, dough from scratch; takes a long time
  - Standard-cell-based ASIC
    - Choose from limited selection of toppings and dough; less work but still slow
  - Gate-array-based ASIC
    - Add canned toppings to pre-cooked crusts; save some time and cost
  - Field-programmable logic device
    - Frozen pizza — limited selection, trivial to cook, very cheap

# Full-Custom ASICs

- Design — engineer does detailed design of logic cells, circuit, and layout
  - Time-consuming and costly!
  - Primarily used if no pre-designed modules are available (e.g., new or highly specialized circuit), or when very high performance is needed
  
- Fabrication — design is sent to a *fabrication facility* (a “fab”), where it is etched onto *wafers*, each wafer containing 100’s of chips
  - Wafers used to be 8”, now 13”, discs
  - Fabrication is expensive (huge fixed startup cost), and takes a couple of months
  - Most chips fabricated using CMOS techniques (details later in the course)

# Standard-Cell-Based ASICs

- Design — chip is built from pre-defined modules called *standard cells*
  - Standard cells are built by someone else using full-custom design techniques
  - Save time, money, and risk by using a well-designed, verified *cell library*
    - But — have to pay for the cell library
  - Also use larger cells (microprocessors, etc.) called *mega cells* (sometimes *cores*)

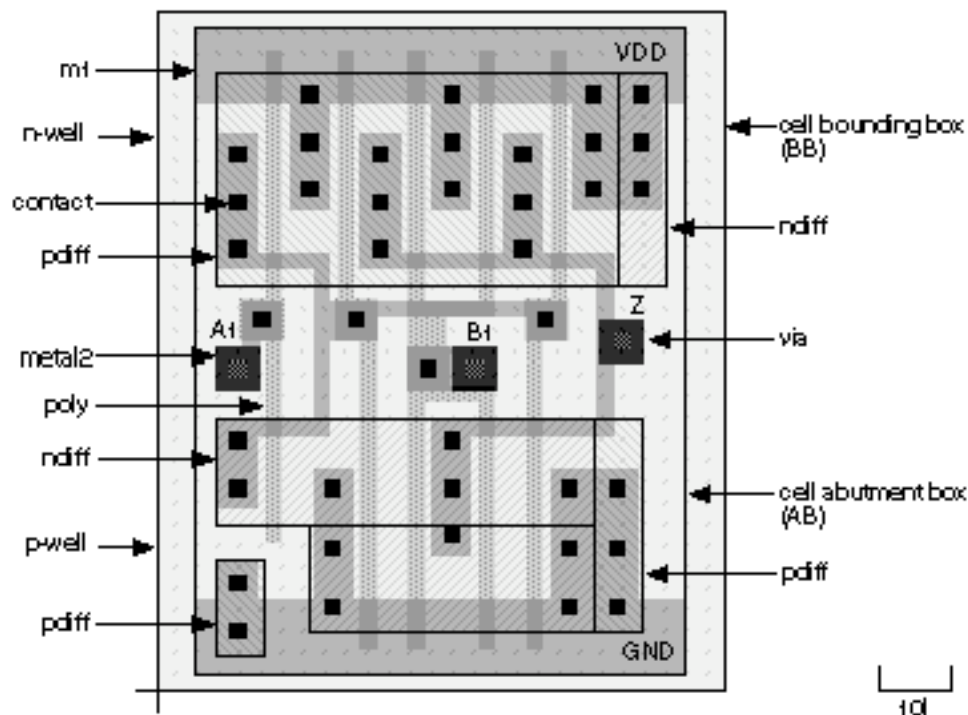
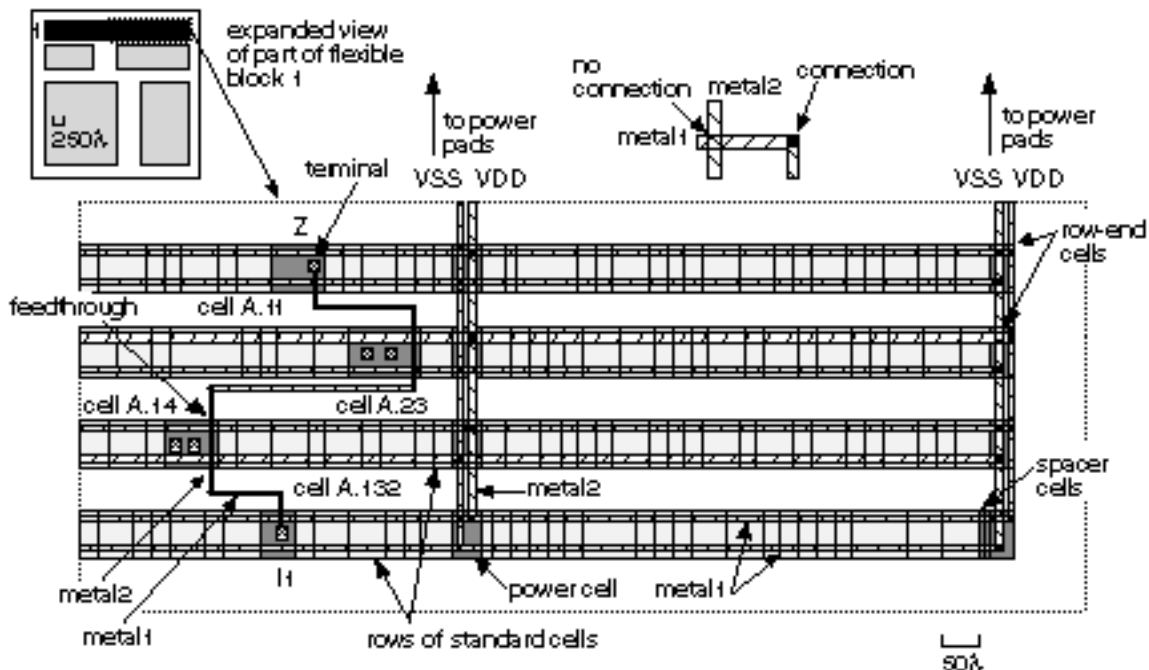


Figure from *Application-Specific Integrated Circuits*, Smith, Addison-Wesley, 1997

# Standard-Cell-Based ASICs (cont.)

- Cells fit together like bricks in a wall — rows of (variable-width) cells
  - Most interconnect goes in *channels* between rows, though some cells may be designated as *feedthroughs (vias)* between rows
  - Most *metal layers* provide interconnect
    - Others provide power and ground
  - Fabrication remains costly and slow





# Gate-Array-Based ASICs

- Designed using pre-defined modules
- Fabrication time reduced — transistors are placed in a fixed pattern on the chip
  - Interconnect is defined by designer and fabricated using a custom mask
- Chip is partially fabricated (cells, power, etc. added) and then stockpiled
  - When design is received for fabrication, the remaining metal layers are added
  - Cheaper — everyone shares cost of producing high volume of initial chip
  - Quick turn-around — days, couple weeks
- Variations:
  - Channeled gate arrays
  - Channelless gate arrays

# Programmable Logic Devices (PLDs)

- Standard ICs, available in standard configurations, sold in high volume
  - No customized cells or masks, just a single large block of programmable interconnect
  - Can be configured / programmed to create a specialized device
  - Fast turn-around time
  
- Examples
  - Mask-programmable ROM — programmed when ordered
  - Programmable ROM — programmed electrically, erased electrically or using ultraviolet light, all by customer
  - PAL, PLA — 2-level sum-of-products and/or array, programmed electrically by customer (blowing fuses in array)

# Field Programmable Logic Devices (FPLDs)

- Known by a variety of names:
  - Field-Programmable Gate Array (FPGA)
  - Field-Programmable Logic Device (FPLD)
  - Complex Programmable Logic Device (CPLD)
  
- Similar to PLDs, but more complex
  - Core is a regular array of programmable logic cells, each of which contains combinational and sequential logic
  - Programmable interconnect surrounds the logic cells
  - Some method provided for programming the base logic cells and the interconnect
  - Designed using pre-defined modules, with “fabrication” turn-around on the order of minutes

## ASICs vs. FPLDs

<b>Characteristic</b>	<b>ASIC</b>	<b>FPLD</b>
Time to market	Long	Short
High volume unit cost	Low	High
NRE	High	None
Flexibility after manufacturing	None	High
Performance	Very High	Medium
Density	Very High	Medium
Power consumption	Low	High
Minimum order quantity	High	None
Design flow complexity	Very High	Medium
Complexity of testing	High	Low
Turnaround time	Months	Hours
<i>Source: Jack Horgan, EDA Weekly, Monday 8/9/04</i>		