

Altera's MAX+PLUS II Development System

- Supports Altera MAX and FLEX devices
- Design entry includes: schematic capture, waveform entry, and the AHDL, VHDL, and Verilog hardware description languages (HDLs) [Verilog \geq 9.xx only]
- Documentation:
 - Tutorials in Hamblen Chapters 1 and 4
 - Brief overview in Salcic Section 3.4
 - Altera's "data sheet" overview (~20 pages) (link on class web page)
 - Altera's "Getting Started" manual (~ 350 pages) (link on class web page)
 - Detailed overview in Chapter 2, "A Perspective" (~80 pages)
 - Printout(s) in VLSI Design Lab
 - Chapter 3, "Tutorial"

Using the MAX+PLUS II Software

- 9.23 Student Edition in Salcic book
- 10.1 Student Edition in Hamblen book
- 10.2 Baseline Edition on Altera web site**
- Differences from commercial version:
 - Can't use non-Altera design entry tools
 - Only supports devices on UP1 Educ. Board
- Install on your home PC if desired
 - Install the software
 - Use form on web page to send your disk drive serial number to Altera, wait for license file from Altera by email
 - *Install into MAX+PLUS II to enable tools (Options / License Setup, select license file)*
- Procedure for projects:
 - Work on projects at home, or in the VLSI Design Lab (MSB 353)
 - Then come to the VLSI lab to download and test on a UP1 Education Board

Schematic Capture using the Graphical Editor in Altera's MAX+PLUS II

- Follow along in Hamblen Chapter 1 Introduction and Section 1.1

- Chapter 1 Introduction
 - The UP1 board
 - The (active-low) pushbuttons
 - The (active-low) “period” on the 7-segment LED displays

- Section 1.1 — Design Entry Using the Graphic Editor
 - New graphic display file, selection of Flex 10K chip
 - Input of OR gate and input/output pins
 - Naming of I/O pins and their assignment to actual pins on UP1 board
 - Saving the schematic

Design Using Altera's MAX+PLUS II

- Follow along in Hamblen Sections 1.2, 1.3, 1.4, 1.9, 1.10
 - Compiling the design
 - Errors, warnings, report file
 - (Timing) simulation
 - Entering simulation test vectors
 - Simulation and results
 - Downloading to the Flex 10k chip on the UP1 Education Board
 - Hookup — parallel cable and power
 - JTAG setup
 - Download and test the design!
 - Timing analysis
 - Floorplan editor
 - Note automatic place and route
- You should try this sometime soon, possibly without actually downloading