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CS 4/55111 **Exam #1** VLSI Design

Monday 13 March 2000

1. **Why are field-programmable logic devices so cost-effective for small-volume designs, but much less cost-effective than standard-cell based chips for high-volume designs? (15 points)**

   With field-programmable logic devices, the fixed costs are lower (the tools are cheap, and testing of the chip is not required by the customer), so they do not have to be distributed over a high volume of devices, thus making small-volume designs cost-effective. However, the variable costs, which account for the cost of each device, are much higher, and those costs would dominate in high-volume designs, thus making high-volume design not very cost-effective.

2. **Briefly describe the difference between a D flip-flop and T flip-flop. (15 points)**

   (Both are generally edge-triggered devices)

   A D flip-flop "stores" the value applied to its D input on a specific edge of the clock, and then makes that value available as its Q output.

   A T flip-flop — as used in Project 2 — "toggles" its output value on a specific edge of the clock as long as the T input is high (if the T input is low, not change occurs to its output value).

3. **How are the various components of a CMOS transistor, such as the diffusion regions that form the source and drain, "drawn" on the transistor? (10 points)**

   A "mask" is formed on the chip by applying photoresist, partiallly exposing that photoresist to ultraviolet light through a mask, and then removing the exposed areas using a solvent. The chip can then be doped with impurities though the resulting holes in the mask on the chip, and afterwards, the photoresist mask can be removed.

4. **Explain how the Waveform Editor and the Simulator in the Altera MAX+PLUS II tools are designed to work together. (15 points)**

   The Waveform Editor is used to specify (1) specific nodes and waveform values that are to be used as inputs to the simulator, and (2) nodes for which outputs are desired. The simulator then simulates the design using those inputs, and displays output waveforms for the desired output nodes.

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5. Suppose you are trying to choose between the Actel ACT 1 family and the Xilinx 4000 family. What types of designs would be best suited for each of these families of devices, and why? (15 points)

The Actel device uses antifuses for programming, as opposed to the Xilinx device, which uses SRAM programming. Since antifuse programming requires smaller, faster, programming elements on the chip, the Actel device would probably be denser and faster, which may be important in some designs. However, the Xilinx device would be more suitable if reprogrammability is necessary.

The Xilinx devices has more powerful logic cells, and potential for on-chip memory of various kinds — flexibility which might be required in more complex designs.

6. The Altera UP1 Education Board contains an Altera MAX 7128 and an Altera FLEX 10K20. Distinguish between these two devices in terms of their capabilities on the UP1 board and their internal architecture (programming method, cell organization, routing, etc.). (30 points)

See Lectures 12, 18, 19, and 20.