Overview of This Course: 4 Main Components

- Introduction to VLSI design
  - Brief introduction to VLSI design and ASICs, review of logic design
  - Using Altera’s Max-PLUS II CAD tool for schematic capture and simulation
- IC technology
  - Brief introduction to CMOS, comparison of various FPLDs
  - Project(s) involving manual design, and schematic capture and simulation using Altera’s Max-PLUS II
- HDL-based design
  - Design using AHDL and VHDL
  - Project(s) involving automated design from AHDL and VHDL descriptions

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Logic Synthesis Design Flow

- Alternative design entry methods
  - HDL-based design — describe design in textual form using familiar programming constructs plus some additional ones
    - Decisions regarding flip-flops etc. are made automatically by the CAD tool
    - Semi-automated design
  - Schematic capture — draw and interconnect structural elements (gates, flip-flops, registers, etc.)
    - Sequential or combinational design
    - Manual design with automated bookkeeping
- Compilation / Synthesis — produce a flat netlist of gates, optimizing the design to minimize area, speed, power, etc.
- Simulation and verification — make sure the design does what you think it does

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Logic Synthesis Design Flow (cont.)

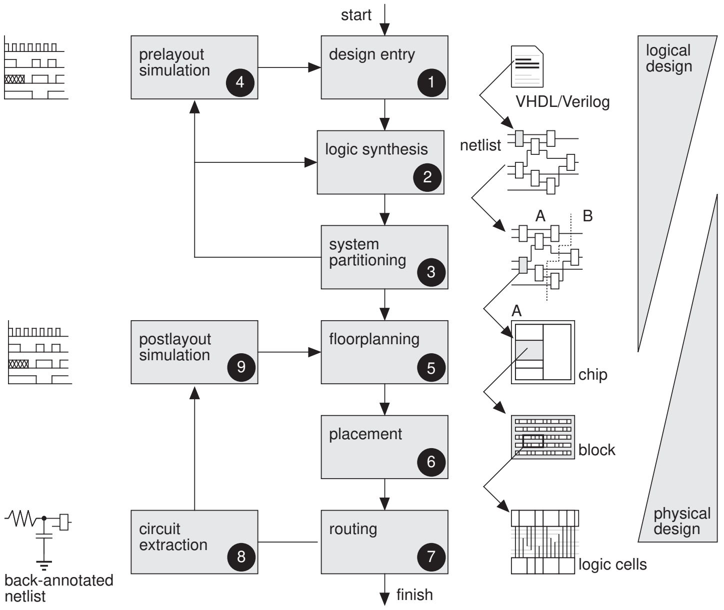

Figure from *Application-Specific Integrated Circuits*, Smith, Addison-Wesley, 1997

Logic Synthesis in a Larger Context

- System synthesis — converts a task specification into processors, memories, ASICs, etc. plus software
  - Hardware / software codesign
  - Tradeoffs between hardware & software
- Behavioral (high-level) synthesis — converts an algorithmic description of behavior into registers, adders, ALUs, busses, multiplexors, etc.
  - Scheduling breaks design into states
  - Data path synthesis produces interconnected set of functional units, registers, etc.
- Logic synthesis — converts a structural description into gates and flip-flops
  - Designer must specify all states