Gate-Array-Based ASICs

- Transistors are predefined in a fixed pattern on the chip
  - Interconnect is defined by designer and fabricated using a custom mask
  - Designer chooses cells from a gate-array library of predefined, pretested cells
- Chip is partially fabricated (cells, power, etc. added) and then stockpiled
  - When design is received for fabrication, the remaining metal layers are added
  - Cheaper — everyone shares cost of producing high volume of initial chip
  - Quick turn-around — days, couple weeks
- Variations:
  - Channeled gate arrays
  - Channelless gate arrays

Programmable Logic Devices (PLDs)

- Standard ICs, available in standard configurations, sold in high volume
  - But can be configured / programmed to create a specialized device
  - No customized cells or masks, just a single large block of programmable interconnect
  - Fast turn-around time
- Examples
  - Mask-programmable ROM — programmed when ordered
  - Programmable ROM — programmed electrically, erased electrically or using ultraviolet light, all by customer
  - PAL, PLA — 2-level sum-of-products and/or array, programmed electrically by customer (blowing fuses in array)

Field Programmable Logic Devices (FPLDs)

- Known by a variety of names:
  - Field-Programmable Gate Array (FPGA)
  - Field-Programmable Logic Device (FPLD)
  - Complex Programmable Logic Device (CPLD)
- Similar to PLDs, but more complex
  - No customized mask layers
  - Some method for programming the base logic cells and the interconnect
  - Core is a regular array of programmable logic cells, each of which contains combinational and sequential logic
  - Programmable interconnect surrounds the logic cells
  - Design turn-around is on the order of hours

Economics of ASICs

- For a given design, which type of ASIC is the most cost-effective?
  - (full-custom) ASIC?
  - MGA (mask-programmable gate array)?
  - CBIC (cell-based integrated circuit = standard-cell-based ASIC)?
- Answer: consider the ASIC as a product, and examine the fixed costs and variable costs
  - total product cost = fixed product cost + variable product cost
  - *Fixed product cost* is independent of sales volume
    - Fixed product costs amortized per product sold decrease as sales volume increases
  - *Variable product cost* includes assembly costs and manufacturing costs

Example of ASIC Economics

- Sample costs:
  - CBIC: fixed cost $146,000; part cost $8
  - MGA: fixed cost $86,000; part cost $10
  - FPGA: fixed cost $21,800; part cost $39

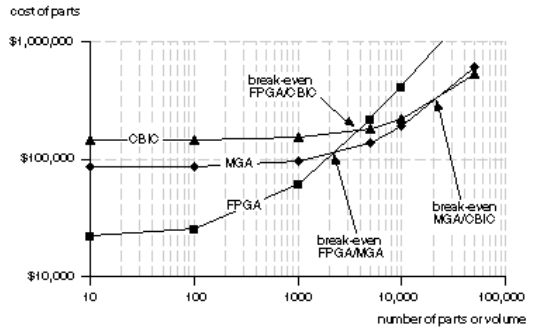

Figure from *Application-Specific Integrated Circuits*, Smith, Addison-Wesley, 1997

- Break-even points:
  - FPGA to MGA is around 2,000 parts
  - FPGA to CBIC is around 4,000 parts
  - MGA to CBIC is around 20,000 parts

ASIC Fixed Costs

- Design: estimate of designer productivity
- Production test: make sure the IC works
- Non-recurring engineering (NRE): work done by ASIC vendor — developing mask, production tests, prototypes, etc.

	FPGA		MGA		CBIC	
Training:	$800		$2,000		$2,000	
Days		2		5		5
Cost/day		$400		$400		$400
Hardware	$10,000		$10,000		$10,000	
Software	$1,000		$20,000		$40,000	
Design:	$5,000		$20,000		$20,000	
Size (gates)		10,000		10,000		10,000
Gates/day		500		200		200
Days		20		50		50
Cost/day		$400		$400		$400
Design for test:			$2,000		$2,000	
Days				5		5
Cost/day				$400		$400
NRE:			$30,000		$70,000	
Masks				$10,000		$50,000
Simulation				$10,000		$10,000
Test program				$10,000		$10,000
Second source:	$2,000		$2,000		$2,000	
Days		5		5		5
Cost/day		$400		$400		$400
Total fixed costs	$21,800		$86,000		$146,000	

Figure from *Application-Specific Integrated Circuits*, Smith, Addison-Wesley, 1997

ASIC Variable Costs

- Wafer size: 6” & 8” common, 12” soon
- 10k gates = small design, 100k = large
- Gate utilization: space used for gates, not used for interconnect
- Defect density is measure of fabrication quality (defect on a die is usually fatal)
- Yield is percentage of usable dies

	FPGA	MGA	CBIC	Units
Wafer size	6	6	6	inches
Wafer cost	1,400	1,300	1,500	$
Design	10,000	10,000	10,000	gates
Density	10,000	20,000	25,000	gates/sq.cm
Utilization	60	85	100	%
Die size	1.67	0.59	0.40	sq.cm
Die/wafer	88	248	365	
Defect density	1.10	0.90	1.00	defects/sq.cm
Yield	65	72	80	%
Die cost	25	7	5	$
Profit margin	60	45	50	%
Price/gate	0.39	0.10	0.06	cents
Part cost	$39	$10	$8	

Figure from *Application-Specific Integrated Circuits*, Smith, Addison-Wesley, 1997