Altera's MAX+PLUS II Development System

- Supports Altera MAX and FLEX devices
- Design entry includes: schematic capture, waveform entry, and the AHDL, VHDL, and Verilog hardware description languages (HDLs) [Verilog in 9.xx only]
- Documentation:
  - Tutorials in Hamblen Chapters 1 and 4
  - Brief overview in Salcic Section 3.4
  - Altera's "data sheet" overview (~20 pages) (link on class web page)
  - Altera's "Getting Started" manual (~ 350 pages) (link on class web page)
    - Detailed overview in Chapter 2, "A Perspective" (~80 pages)
      - Printout(s) in VLSI Design Lab
    - Chapter 3, "Tutorial"

Using the MAX+PLUS II Software

- 7.21 Student Edition in Salcic book
  - Runs on PCs
    - Windows 3.1, 95, NT 3.51 & 4.0
    - Requires 32MB memory, 35MB disk space
  - Differences from commercial version:
    - Can't use non-Altera design entry tools
    - Only supports devices on UP1 Educ. Board
    - Can't generate output files other than for programming chips on UP1 Educ. Board
  - You can install at home, but must register with Altera (see Altera's web page) to get an authorization code to use it
    - Start installing, get Software Guard ID
    - Use form on web page to send it to Altera
    - Within 12 hours, should get Authorization Code from Altera by email
    - Input into MAX+PLUS II to enable it

Using the MAX+PLUS II Software

- 9.23 Student Edition in Hamblen book
  - Runs on PCs
    - Windows 95, 98, NT 3.51 & 4.0
    - Uses about 90MB disk space for software plus Hamblen's examples
  - You can install at home, but must register with Altera (see Altera's web page) to get a license file to use it
    - Install the software
    - Use form on web page to send your disk drive serial number to Altera
    - Within 12 hours, should get a license file from Altera by email
    - Install along with MAX+PLUS II to enable it
- Procedure for projects:
  - Work on projects at home, in MSB 139, or in the VLSI Design Lab (MSB 353)
  - Then come to the VLSI lab to download and test on a UP1 Education Board

Altera MAX+PLUS II Overview

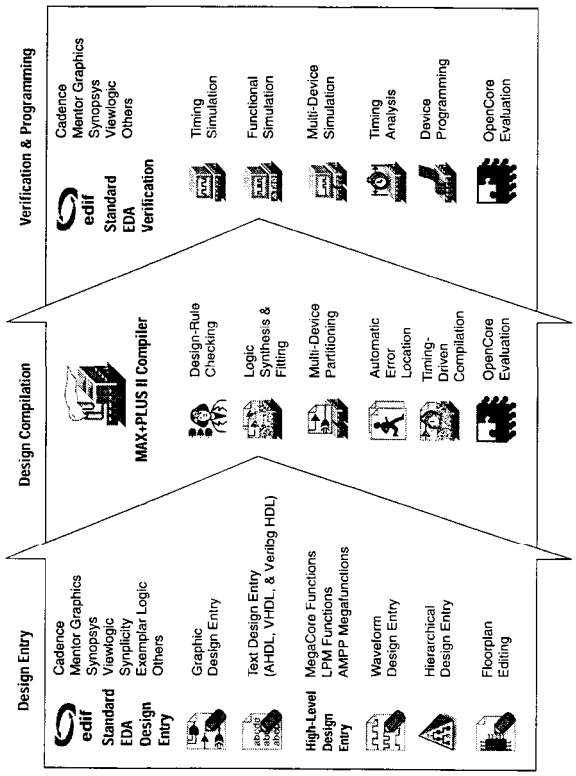


Figure from Altera technical literature

The “Chiptrip” Tutorial Example

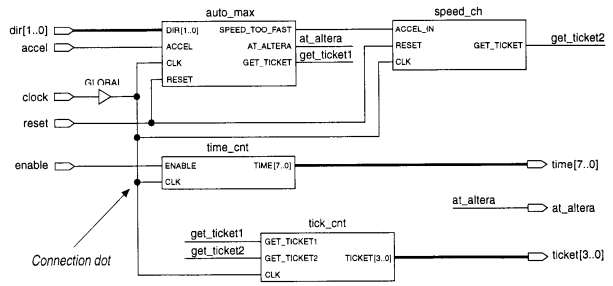


Figure from Altera technical literature

- Simulates an auto driving around town
  - auto_max — AHDL state machine that keeps track of location of auto and acceleration at that point in time, gives ticket if you accelerate on small roads
  - speed_ch — waveform state machine that gives ticket if you accelerate for a second time
  - tick_cnt — counter that counts tickets
  - time_cnt — AHDL counter that keeps track of time taken to reach Altera

Graphic Editor

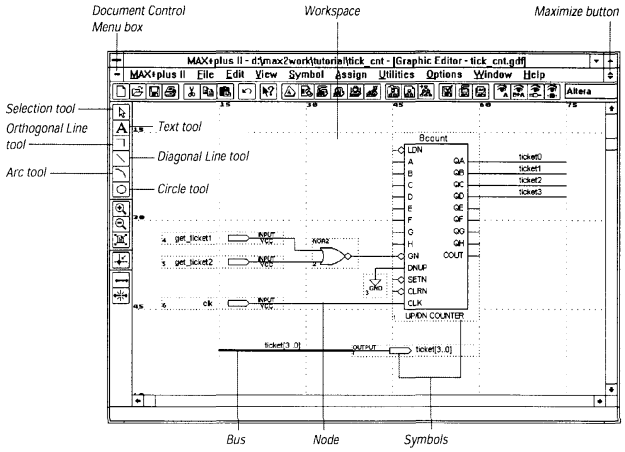


Figure from Altera technical literature

- Enter cells from various predefined component libraries, or user-defined cells
- Connect cells using nets, buses, or name
- “Smart” selection tool — automatically becomes proper tool for task at hand

Waveform Editor

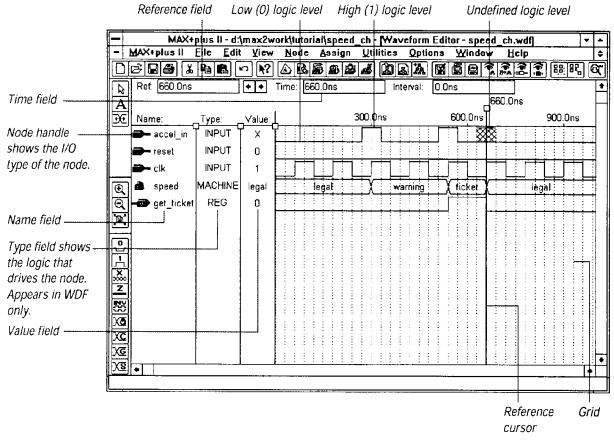
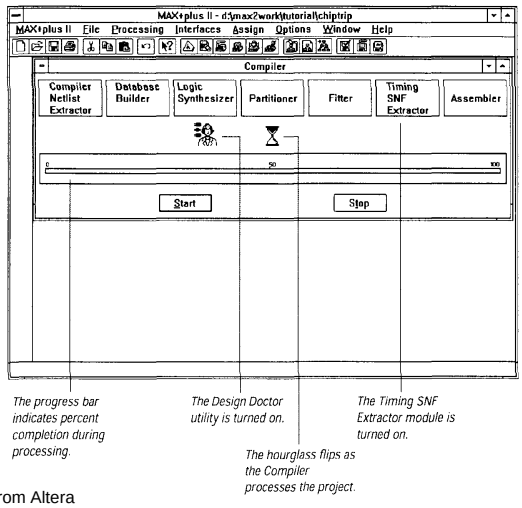


Figure from Altera technical literature

- Can contain logical and state machine inputs; combinational, registered, and state machine outputs; and “buried” nodes to help define desired outputs
  - Can specify state names for state machines
- Can compare desired and actual outputs

Compiler



Figuref from Altera technical literature

- Checks for design entry errors, builds a single large flat database
- Logic synthesis to minimize resource usage (see Assign/Global Project Logic Synthesis), partitioner and fitter to match to available devices

Simulation Results

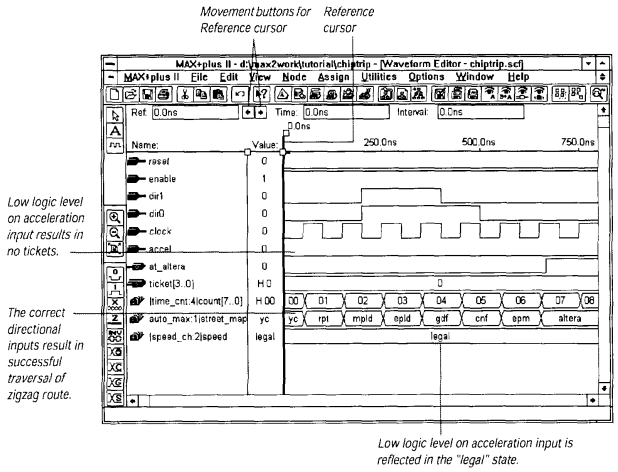


Figure from Altera technical literature

- Use waveform editor to specify simulation inputs
- Simulate, then view results in waveform editor (as shown above)
  - Simulate individual or grouped nodes (particularly good for state machines)

Floorplan Editor

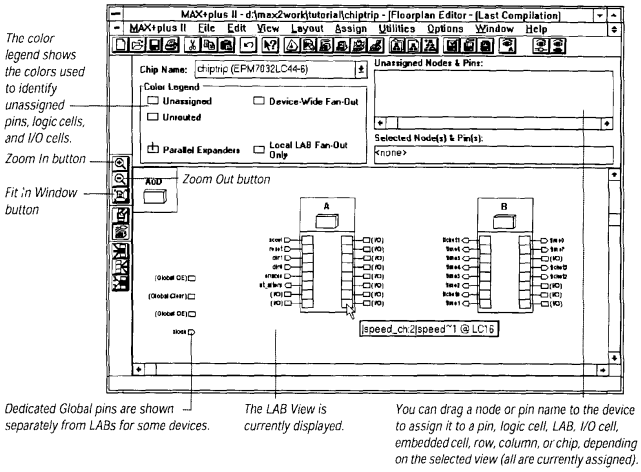


Figure from Altera technical literature

- Device view shows pins, LAB view shows LABs, equations, I/O, and routing
- Can use to edit assignments
- After compilation, get information on most congested area of chip, number of expanders used within each LAB

Design Using Altera's MAX+PLUS II

- Follow along in Hamblen Sections 1.2, 1.3, 1.4, 1.9, 1.10
  - Compiling the design
    - Errors, warnings, report file
  - (Timing) simulation
    - Entering simulation test vectors
    - Simulation and results
  - Downloading to the Flex 10k chip on the UP1 Education Board
    - Hookup — parallel cable and power
    - JTAG setup
    - Download and test the design!
  - Timing analysis
  - Floorplan editor
    - Note automatic place and route
- You should try this sometime soon, possibly without actually downloading