Using Altera's MAX+PLUS II

- Hamblen 1 — covered before
- Hamblen 2 — The UP1 CPLD Board
  - Also see following slides
- Hamblen 4 — Tutorial II: Sequential Design and Hierarchy
  - Using the UP1core hex to 7 segment decoder in a design
  - Using buses
  - Timing analysis for registered performance
  - Testing the design, redesigning to fix the switch contact bounce
- Hamblen 5 — UP1core Library Functions
  - Hex to 7 Segment Decoder, Pushbutton Debouncer, Pushbutton Single Pulse

Altera UP 1 Education Board

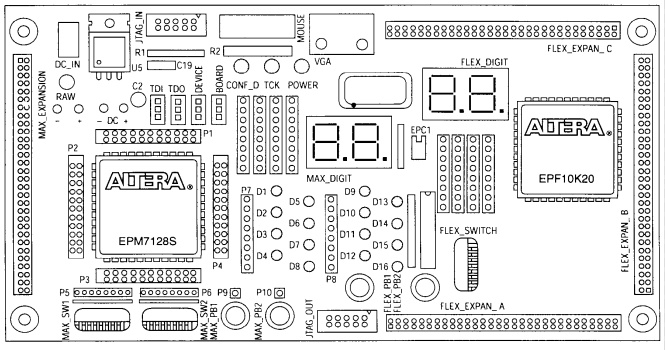

Figure from Altera technical literature

- Contains one EPM7128S device
  - Socket-mounted 84-pin PLCC package
  - 128 macrocells = 2,500 gates (AND-OR, EEPROM)
- Contains one EPF10K20 device
  - 240-pin RQFP package
  - 1,152 LEs and 6 EABs = 20,000 gates (LUT, SRAM)

Altera UP 1 Education Board (cont.)

- Resources available for 7128
  - 2 push-button switches (active low)
  - 2 octal dip-switches (active low)
  - 16 LEDs (active low)
  - Two-digit 7-segment display (active low)
  - Expansion port (left side of board)
  - Connect to female headers around chip
- Resources available for 10K20
  - 2 push-button switches (active low)
  - 1 octal dip-switch (active low)
  - Two-digit 7-segment display (active low)
  - VGA port, mouse port
  - 3 expansion port (right side of board)
  - Connect to female headers around chip