Cross-Section of an N-Channel MOS Transistor (Review)

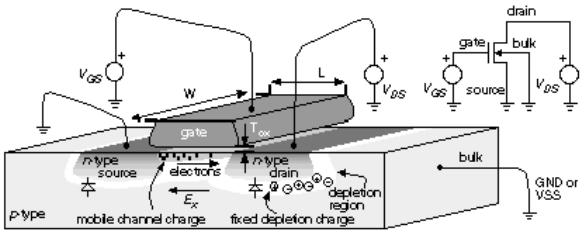

Figure from *Application-Specific Integrated Circuits*, Smith, Addison-Wesley, 1997

- Base is silicon *substrate* (*bulk*, *well*, *tub*) that's been *doped* with p-type impurities (full of positively-charged *holes*)
  - Two *diffusion* areas heavily doped with n-type impurities (full of negatively-charged *electrons*) form the *source* and *drain*
  - Transistor action takes place at the *channel*, connecting the source and drain
- A very thin layer of silicon dioxide (SiO_2), called the *gate oxide*, insulates the *gate*, made of polysilicon, from the channel

IC Fabrication

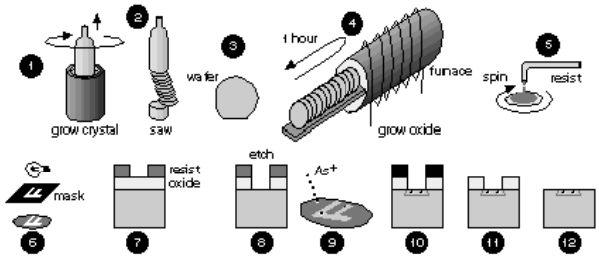

Figure from *Application-Specific Integrated Circuits*, Smith, Addison-Wesley, 1997

1. Start with silicon (Si), refined from quartzite, dope it with p- or n-type impurities, and melt it at 1500°C

2.&3. Draw out a single crystal (6" or 8"), saw it into thin (600µm) *wafers*, polish one side, and grind down an edge or two

4. Batch of wafers (a *wafer lot*) is placed on a *boat* and put in a furnace to grow a layer (1000 Å) of silicon dioxide (SiO_2) (called the *oxide*)

IC Fabrication (cont.)

- IC fabrication process uses a series of masking steps to create the layers that form the transistors etc. on the chip

5. A thin layer (1 µm) of liquid photoresist (*resist*) is spun onto each wafer, and it is baked at 100°C to harden the resist

6. The wafer is partially exposed to ultraviolet light through a *mask*, which polymerizes the exposed areas; the polymerized part is then removed using an organic solvent

7. The exposed oxide is *etched* away, making the oxide match the mask

8. The exposed silicon substrate is doped with appropriate ions by an *ion implanter*

9. & 10. Resist and oxide are removed

Fabricating a CMOS Transistor

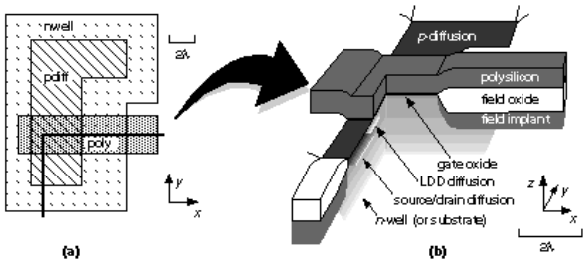

Figure from *Application-Specific Integrated Circuits*, Smith, Addison-Wesley, 1997

- Continuing the fabrication process:
  - Polycrystalline silicon (*poly*) is deposited using using *chemical vapor deposition* (*CVD*) to deposit dopants using a gaseous source in a furnace
    - Poly wires (e.g., transistor gates) are deposited before diffusion to create self-aligned transistors — this avoids small gaps that might otherwise occur if the order is reversed
  - Metal layers are deposited in a similar manner, called *sputtering*

Fabricating a CMOS Transistor (cont.)

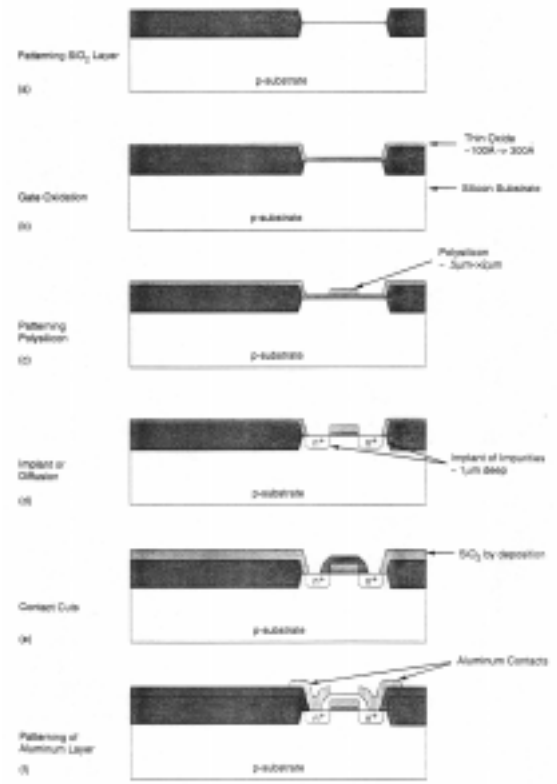

Figure from *Principles of CMOS VLSI Design*, Weste, Addison-Wesley, 1993

Wires and Vias

- "Wires" can be fabricated using diffusion, polysilicon, or metal
  - Must be insulated from each other using silicon dioxide; can be built up as layers
  - Diffusion used only for within a cell
  - Poly used between adjacent cells
  - Metal used for longer connections
    - Chip may have 5-6 layers of metal
  - Cuts in the silicon dioxide between layers are called *vias*
- Metal layer 1 is used for VDD and VSS; other layers are used for interconnection
  - Under high currents, electron collisions with metal grains can cause the metal to move (*metal migration*), so in large designs, sizing the power supply lines is critical to keep chip from failing

CMOS Inverter in a n-well Process

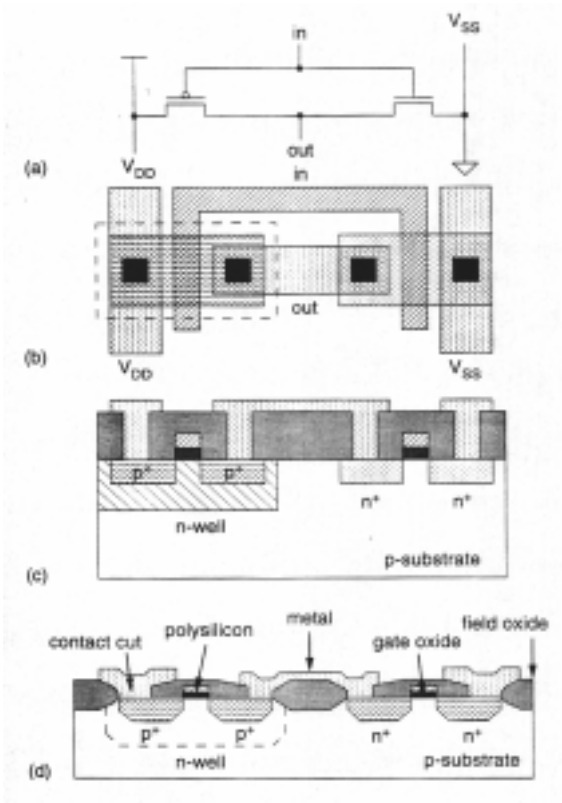

Figure from *Principles of CMOS VLSI Design*, Weste, Addison-Wesley, 1993

CMOS Inverter in a n-well Process, With Tub Ties

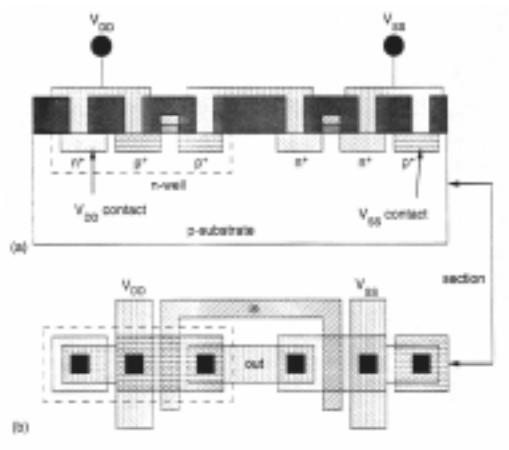

Figure from *Principles of CMOS VLSI Design*, Weste, Addison-Wesley, 1993

- An n-channel (p-channel) transistor's substrate must be tied to VSS (VDD)
  - The special vias that provide these connections are called *tub ties*
    - Need one every 1-2 transistors (SCMOS)
  - Tie area in substrate is heavily doped to provide a low-resistance connection

Design Rules & Fabrication Errors

- Common fabrication errors:
  - Wire too wide — may *short* (contact) an adjacent wire
  - Wire too narrow — may break under load, and become *open*
- Solution — impose *design rules* to specify what's legal and illegal
  - Wires — specify minimum width and minimum spacing between wires
  - Poly — must extend beyond channel to ensure that there is no short between source and drain
  - Diffusion — must extend enough to have room for a contact to that region
  - Via — must be smaller than what it's contacting, what it's contacting must extend back under SiO_2

Scaleable Design Rules

- Fabrication processes are constantly being improved
  - (Gordon) Moore's Law (version 2) says that the number of transistors on a chip is doubling every 18 months
- We take advantage of these improvements by designing according to *scaleable design rules*
  - Specified in terms of λ, the minimum feature size possible in that process
  - In MOSIS SCMOS rules, mimium channel width (poly) is 2λ , and minimum wire width is 2λ
    - MOSIS = MOS Implementation Service, located at the Information Sciences Institute at the University of Southern California (USC), does small-volume fabrication for universities (partially NSF-funded) and commercially (www.isi.edu)

SCMOS Design Rules (cont.)

- MOSIS (rev. 7), dimensions in λ

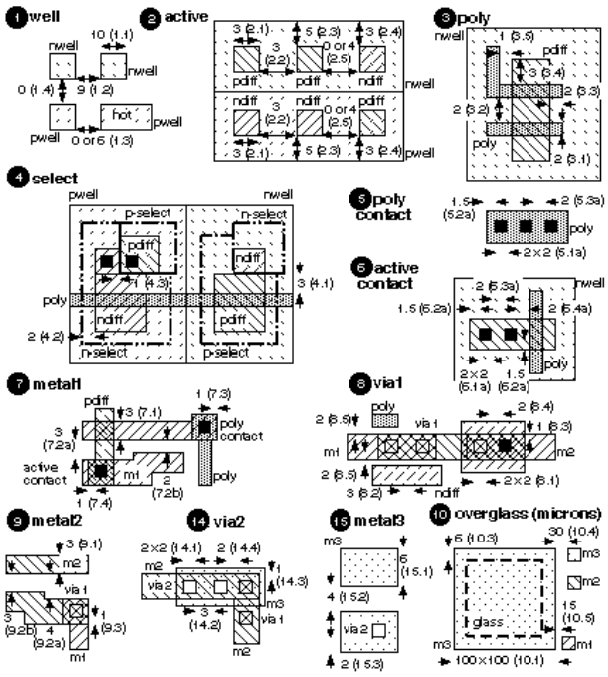

Figure from *Application-Specific Integrated Circuits*, Smith, Addison-Wesley, 1997

SCMOS Design Rules (cont.)

- MOSIS (rev. 7), dimensions in λ

TABLE 2.7 MOSIS scalable CMOS rules version 7the process front end.

Layer	Rule	Explanation	Value / λ
well (CWN, CWP)	1.1	minimum width	10
	1.2	minimum space (different potential, a hot well)	9
	1.3	minimum space (same potential)	0 or 6
	1.4	minimum space (different well type)	0
active (CAA)	2.1/2.2	minimum width/space	3
	2.3	source/drain active to well edge space	5
	2.4	substrate/well contact active to well edge space	3
	2.5	minimum space between active (different implant type)	0 or 4
poly (CPG)	3.1/3.2	minimum width/space	2
	3.3	minimum gate extension of active	2
	3.4	minimum active extension of poly	3
	3.5	minimum field poly to active space	1
select (CSN, CSP)	4.1	minimum select spacing to channel of transistor 1	3
	4.2	minimum select overlap of active	2
	4.3	minimum select overlap of contact	1
	4.4	minimum select width and spacing 2	2
poly contact (CCP)	5.1.a	exact contact size	2 ∞ 2
	5.2.a	minimum poly overlap	1.5
	5.3.a	minimum contact spacing	2
active contact (CCA)	6.1.a	exact contact size	2 ∞ 2
	6.2.a	minimum active overlap	1.5
	6.3.a	minimum contact spacing	2
	6.4.a	minimum space to gate of transistor	2

Table from *Application-Specific Integrated Circuits*, Smith, Addison-Wesley, 1997