Implementing a Truth Table Using An And-Or Structure (Review)

- Given a truth table, we can use a Karnaugh map to find the minimum 2-level SOP implementation

a	b	c	d	x
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

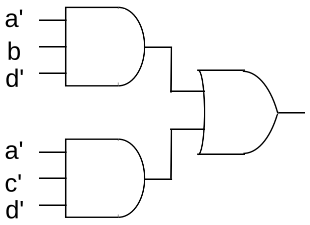
c

1	0	0	0
1	0	0	1
0	0	0	0
0	0	0	0

b

a

d



x = a'bd' + a'c'd'

PLAs

- A 2-level *and-or* structure is replicated many times in a programmable array called a *PLA* (*programmable logic array*)
  - Parts of a CPU’s datapath or next-state logic can be built out of PLAs
  - Small circuits can be built out of PLAs
- At the input of each gate, there's a “fuse” which can be left whole, or broken
  - So the designer can control which inputs go to each and gate, and which outputs of the and gates go to each or gate
- A PLA can be either
  - Mask programmable — customer orders a programmed PLA from the manufacturer
  - Field programmable — customer can program PLA (once)

PLAs

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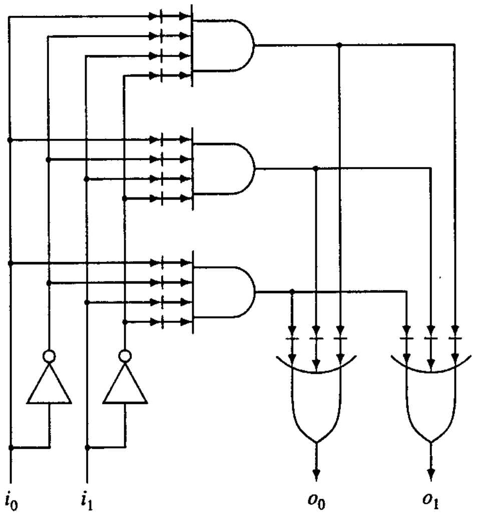


Diagram from *Computer Systems*, Maccabe, Irwin 1993

- This PLA has 2 inputs, 2 outputs, and can represent up to 3 product terms

PLA Example

- This is an *abstract* diagram of a PLA with 6 inputs, 4 outputs, which can represent up to 12 product terms

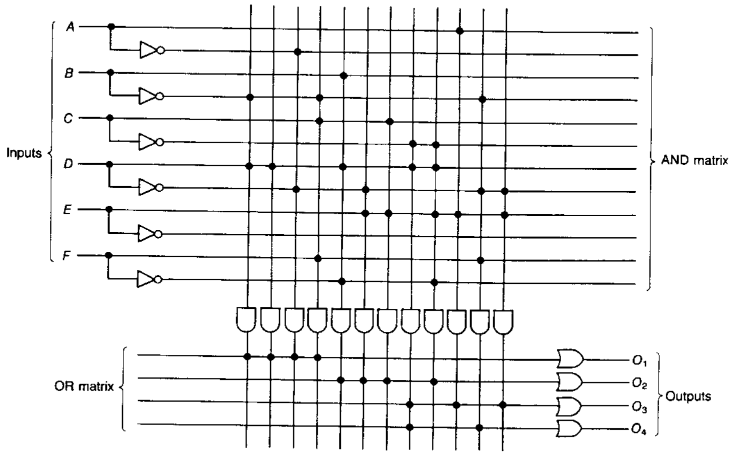


Diagram from *Digital Design*, Johnson & Karim, PWS-Kent 1987

- Try the Java KMap->PLA animation at http://tech-www.informatik.uni-hamburg.de/applets/kvd

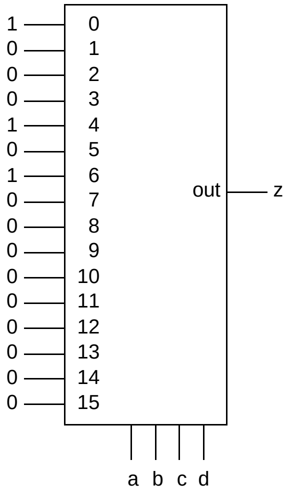
Field-Programmable Logic Device

- The next evolutionary step beyond the PLA is the *field-programmable logic device* (FPLD), also called the:
  - Field-programmable gate array (FPGA)
  - Complex programmable logic device (CPLD)
- FPLD characteristics
  - Based on either an array of PLA-like *and-or* structures,or on look-up tables
    - Usually includes connections from these structures to 4 nearest neighbors
    - May include long connections across chip
  - May include D (or more complex) flip-flops, to more easily build sequential circuits, possibly even RAM
  - Many can be “programmed” repeatedly
  - Available in different sizes up to 500,000 gates (100MHz, 2.5 volt, 0.25µ, 5 metal)

Implementing a Truth Table Using a Multiplexor

- Besides and-or structures, another alternative is to use a 4-input multiplexor

a	b	c	d	x
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

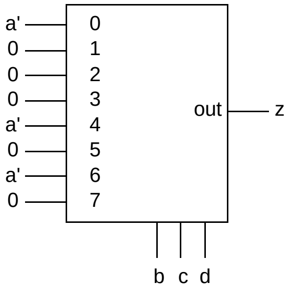


- Any function of N inputs can be implemented using a 2^N to 1 multiplexor

Implementing a Truth Table Using a Multiplexor (cont.)

- An alternative is to “fold” the truth table, and tie each input to either 1, 0, or the MSB, and only use a 3-input multiplexor

a	b	c	d	x
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0



- Any function of N inputs can be implemented using a 2^{N-1} to 1 multiplexor
  - Some FPLDs are based on multiplexors, and attach simple gates to selector lines

Implementing a Truth Table Using a ROM

- Yet another alternative is to use a ROM

a	b	c	d	x
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
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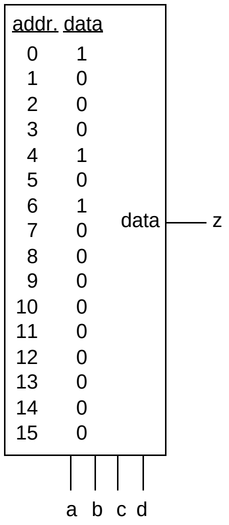
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0



addr.	data
0	1
1	0
2	0
3	0
4	1
5	0
6	1
7	0
8	0
9	0
10	0
11	0
12	0
13	0
14	0
15	0

- Any function of N inputs can be implemented using a 2^Nx 1 bit ROM
  - Some FPLDs are based on static RAMs (SRAMS) loaded at power-up; these are said to use *look-up tables* (LUTs)

Different Implementation Styles

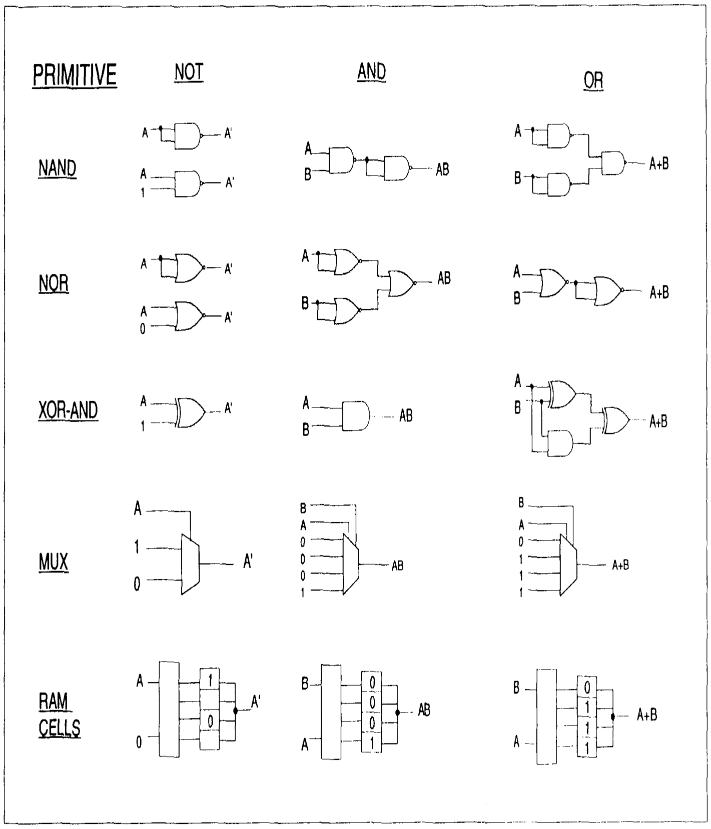


Diagram from *Digital Design Using Field Programmable Gate Arrays*, Chan & Mourad, Prentice Hall 1994