Types of FPLDs

Programming Method	Multiplexor	Look-Up Table (LUT)	AND-OR
Antifuse	**Actel** ACT 1, ACT 2, ACT 3 **Quicklogic** **Crosspoint**		
EPROM			**Altera** MAX 5000, 7000 *(Salcic 2.1)* **Xilinx** EPLD
SRAM	**Plessy**	**Altera** Flex 8000, Flex 10K *(Salcic 2.2)* **Xilinx** LCA 2000, 3000, 4000 *(Salcic 2.3)*	

Type of Base Cell

FPGAs **CPLDs**

- Layout / routing
  - Row-based: Actel
  - Matrix-based: Altera, Quicklogic, Xilinx

Programming Using Antifuses

- An *antifuse* is normally open ("off"); when enough current (5–15mA) passes through it it closes ("on")
  - Current melts a thin insulating dielectric and forms a permanent silicon link
  - Disadvantage — can only program once
    - Programmed in a special hardware device
    - An antifuse FPLD may contain 750,000 antifuses, but only about 2% of them typically need to be programmed
    - Takes about 5-10 minutes for each chip
- Advantages:
  - Small — about the size of a via
  - Low resistance, low capacitance = fast
- Antifuses can be used in FPLDs to :
  - Connect inputs to cells
  - Connect cells to interconnect

Programming Using EPROMs & EEPROMs (Floating Gates)

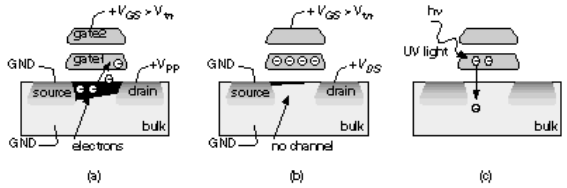
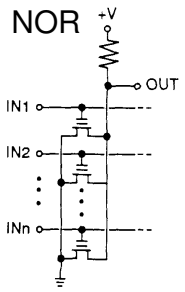


Figure from *Application-Specific Integrated Circuits*, Smith, Addison-Wesley, 1997

- EPROM programming & operation:
  - To program: a high (>12V) programming voltage V_{PP} is applied to the drain, causing electrons to "jump" onto the floating gate (gate1)
    - The electrons on gate1 raise the threshold voltage V_t enough that the programmed transistor is always off
  - To erase: the transistor is exposed to UV light, which provides enough energy for the electrons stuck on gate1 to jump back onto the bulk, returning the transistor to normal operation
  - Can be reprogrammed many times

Programming Using EPROMS & EEPROMs (Floating Gates) (cont.)

- EEPROMs are similar, but are erased electrically
  - Faster to erase than EPROM, and can be done "in-circuit"
  - Requires larger cell than EEPROM
- Advantages
  - Can be programmed repeatedly, in-circuit
  - Very small — requires only vertical space
- Can be used in FPLDs to :
  - Connect inputs to cells
    - In NOR gate, when transistor is programmed (disabled), an input of 1 can not pull output down to VSS
  - Connect cells to interconnect



Programming Using Static RAMs (SRAMs)

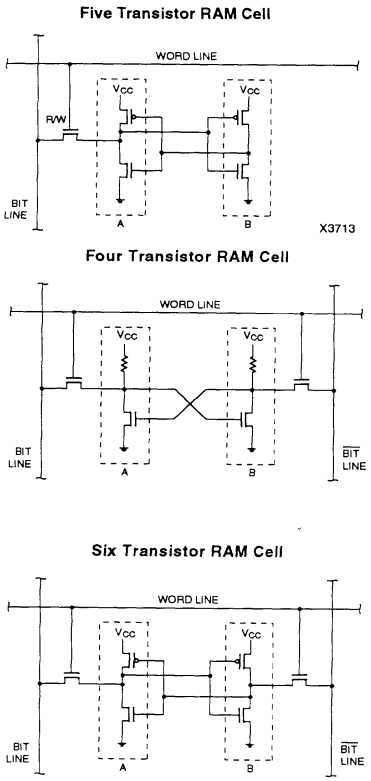


Figure from *Field-Programmable Gate Array Technology*, Trimberger, Kluwer, 1994

Programming Using Static RAMs (SRAMs) (cont.)

- Disadvantages:
  - Must load configuration from ROM, disk, etc. on power-up
  - Large — requires several transistors
- Advantages:
  - Can be programmed repeatedly, in-circuit
    - Can be programmed quickly (< 1ms)
  - Part has been 100% tested at factory
  - Same basic process as CMOS, so quickly takes advantage of new fab processes
    - CMOS also requires less power than circuits requiring pull-up resistors
- SRAMs can be used in FPLDs to :
  - Connect inputs to cells, or even to replace the cell if it's a LUT
  - Connect cells to interconnect

Row-Based Layout

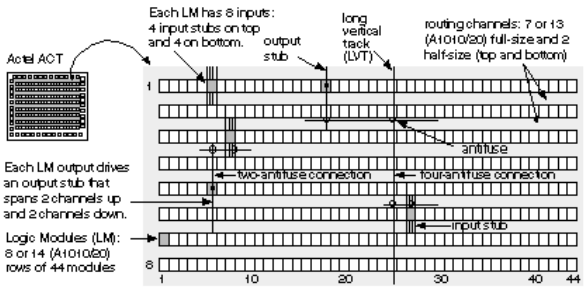


Figure from *Application-Specific Integrated Circuits*, Smith, Addison-Wesley, 1997

- Cells are arranged in rows
  - Horizontal channels between rows
  - Vertical channels above cells: some short, some long
  - Each *channel* contains a fixed number of *tracks*, each track holds one wire
    - Wires may be divided into fixed-length *segments* within each track
  - In figure above, cell inputs connect to horizontal wires, outputs to vertical wires

Matrix-Based Layout

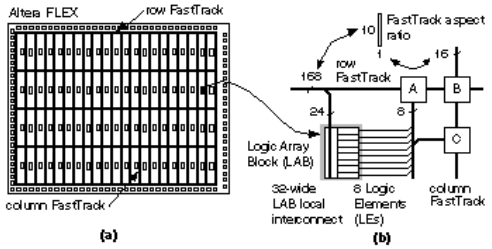


Figure from *Application-Specific Integrated Circuits*, Smith, Addison-Wesley, 1997

- Cells are arranged in an array (*matrix*)
  - Horizontal and vertical channels between cells
  - Each *channel* contains a fixed number of *tracks*, each track holds one wire
  - In figure above:
    - Cell inputs connect to horizontal tracks
    - Box A connects cell output(s) to horizontal tracks, and box C connects cell output(s) to vertical tracks
    - Box B acts as a switchbox between horizontal and vertical tracks

FPGA Pricing

- Pricing = base price plus adjustments
  - Discount for buying in quantity
  - Discount for buying after process matures
  - Premium for faster speed grade
  - Premium for better package types
  - Premium for industrial or military quality
- Some prices from distributors (2/26/98)
  - Xilinx prices at http://www.marshall.com
    - Biggest = 388 macrocells,
      fastest = 15ns (75 MHz),
      $127 for 1–24, $82 for >100
    - Smallest = 36 macrocells,
      slowest = 15ns (75 MHz)
      $5 for 1–24, $3 for >100
    - Fastest = 5ns (200 MHz),
      36 macrocells
      $19 for 1–24, $12 for >100