CS 4/55111

Project #1

VLSI Design

Due in class on Friday 25 February 2000

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1. Do **Lab Exercise 5 on page 25** of *Rapid Prototyping of Digital Systems*.

   Turn in:

   a) a printout of the schematic

   b) a printout of the test vectors and simulation output that shows that that the circuit works as expected

   c) a printout of the timing analysis showing the input to output delay matrix

   d) a statement signed by Prof. Walker or one of his graduate students who use the VLSI Design Lab (Liying Chen, Junli Li, Wenjun Miao, or Kun Qiu) saying that you successfully downloaded the design to a UP1 board and it worked correctly
   (Note — these students are there doing their own research, so although they may not mind signing off that your design works, they are not TAs for the course, and should not be expected to provide technical assistance with Altera's MAX+PLUS II tools.)

2. Do **Lab Exercise 13 on page 26** of *Rapid Prototyping of Digital Systems*, retargeting the XOR example of Lab Exercise 5 to the MAX chip.

   Turn in:

   a) a printout of the schematic

   b) a printout of the test vectors and simulation output that shows that that the circuit works as expected

   c) a printout of the timing analysis showing the input to output delay matrix

   d) a statement signed by Prof. Walker or one of his graduate students who use the VLSI Design Lab (Liying Chen, Junli Li, Wenjun Miao, or Kun Qiu) saying that you successfully downloaded the design to a UP1 board and it worked correctly
   (Note — these students are there doing their own research, so although they may not mind signing off that your design works, they are not TAs for the course, and should not be expected to provide technical assistance with Altera's MAX+PLUS II tools.)