

Name: _____

3. Consider the two VHDL processes below, each of which will be implemented by a D flip-flop during logic synthesis. How will the two resulting flip-flops differ, and why? Be specific. (15 points)

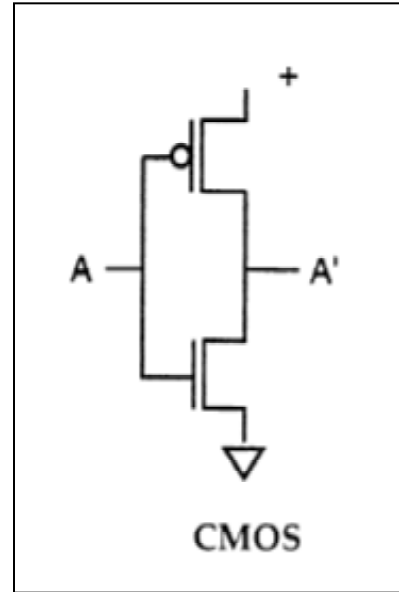
```
PROCESS
BEGIN
    WAIT UNTIL ( Clock'EVENT AND Clock = '1' );
    IF reset = '1' THEN
        Q2 <= '0';
    ELSE
        Q2 <= D;
    END IF;
END PROCESS;
```

```
PROCESS (Reset, Clock)
BEGIN
    IF Reset = '1' THEN
        Q3 <= '0';
    ELSEIF ( Clock'EVENT AND Clock = '1' ) THEN
        Q3 <= D;
    END IF;
END PROCESS;
```

4. CMOS transistors are made primarily of silicon, which isn't a very good conductor. Why make transistors out of silicon, instead of a good conductor like copper? (10 points)

Name: _____

5. Consider the device built from two CMOS transistors as shown at the right. Briefly describe what function it performs, and how it works. (15 points)



6. The Altera MAX 7000 family provides sharable expanders and parallel expanders within each macrocell. What are these expanders, and how are they used? (10 points)

Name: _____

7. The primary difference between the Altera FLEX 8000 family and FLEX 10K family is the presence of Embedded Array Blocks (EABs) in the FLEX 10K. What are these EABs, and how are they used? (10 points)

8. Consider the Xilinx Virtex family of FPGAs, introduced on the attached three pages. How does this family compare to the FPLDs we discussed in class? These few pages obviously do not provide much detail, but provide the best comparison you can, given this brief overview. Note that this question counts more than any other question on the exam. (20 points)