Altera FLEX 8000 Block Diagram

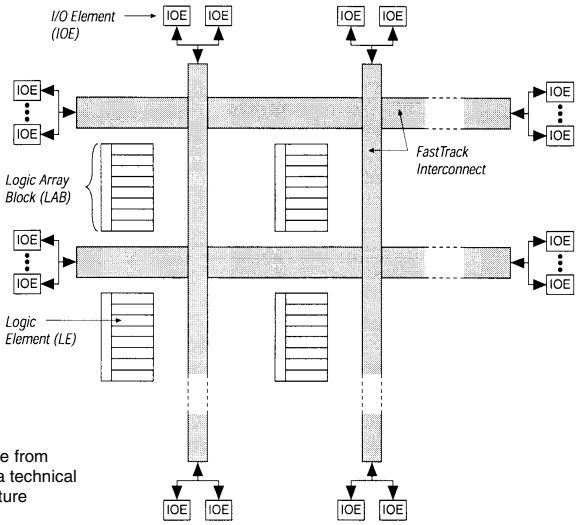


Figure from Altera technical literature

- FLEX 8000 chip contains 26–162 LABs
  - Each LAB contains 8 Logic Elements (LEs), so a chip contains 208–1296 LEs, totaling 2,500–16,000 usable gates
  - LABs arranged in rows and columns, connected by FastTrack Interconnect, with I/O elements (IOEs) at the edges

Altera FLEX 8000 Logic Array Block

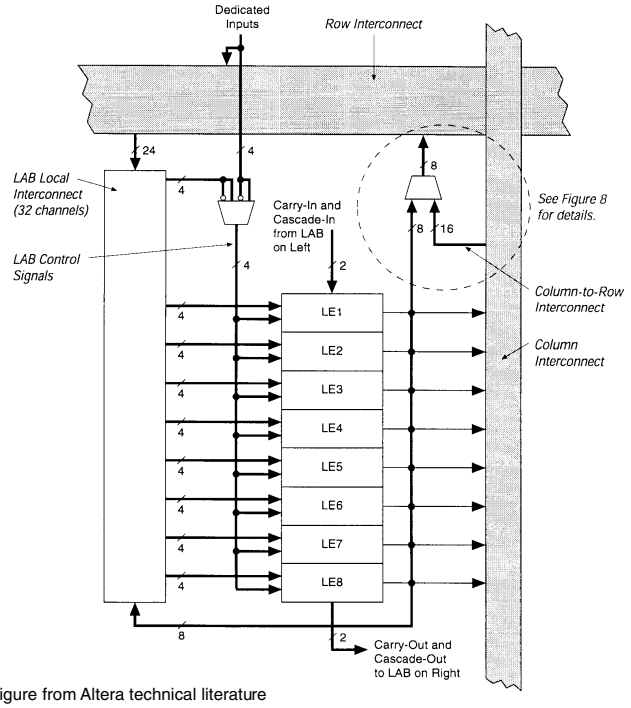


Figure from Altera technical literature

- LAB = 8 LEs, plus local interconnect, control signals, carry & cascade chains

Altera FLEX 8000 Logic Element

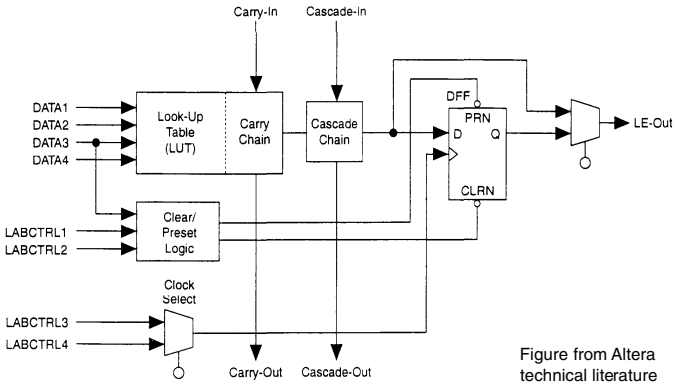


Figure from Altera technical literature

- Each Logic Element (LE) contains:
  - 4-input Look-Up Table (LUT)
    - Can produce any function of 4 variables
  - Programmable flip-flop
    - Can configure as D, T, JR, SR, or bypass
    - Has clock, clear, and preset signals that can come from dedicated inputs, I/O pins, or other LEs
  - Carry chain & cascade chain

Altera FLEX 8000 Carry Chain (Example: n-bit adder)

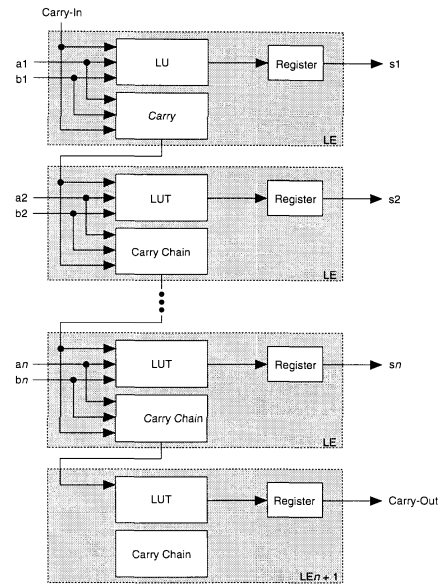


Figure from Altera technical literature

- *Carry chain* provides very fast (< 1ns) carry-forward between LEs
  - Feeds both LUT and next part of chain
  - Good for high-speed adders & counters

Altera FLEX 8000 Cascade Chain

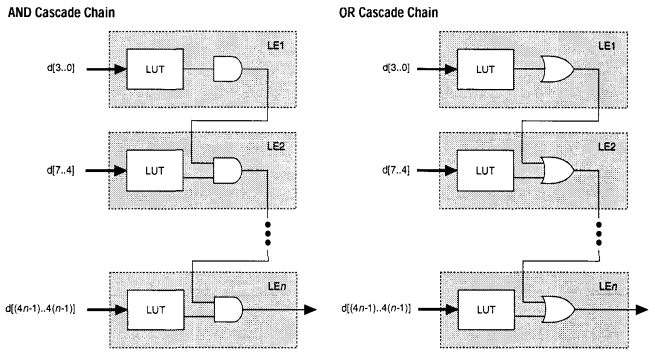
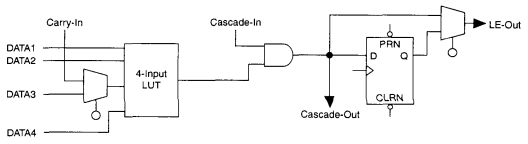


Figure from Altera technical literature

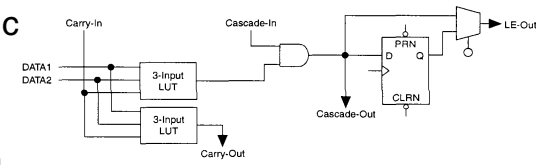
- *Cascade chain* provides wide fan-in
  - Adjacent LE's LUTs can compute parts of the function in parallel; cascade chain then serially connects intermediate values
  - Can use either a logical AND or a logical OR (using DeMorgan's theorem) to connect outputs of adjacent LEs
  - Each additional LE provides 4 more inputs to the width of the function

Altera FLEX 8000 LE Operating Modes

Normal



Arithmetic



Up/down Counter

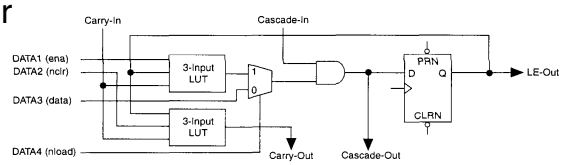


Figure from Altera technical literature

- Each mode uses LE resources differently
  - 7 out of 10 inputs (4 data from LAB local interconnect, feedback from register, and carry-in & cascade-in) go to specific destinations to implement the function
  - Remaining 3 provide clock, clear, and preset for register

Altera FLEX 8000 Operating Modes (cont.)

- Normal mode
  - Used for general logic applications, and wide decoding functions that can benefit from the cascade chain
- Arithmetic mode
  - Provides two 3-input LUTs to implement adders, accumulators, and comparators
    - One LUT provides a 3-bit function
    - Other LUT generates a carry bit
- Up/down counter mode
  - Provides counter enable, synchronous up / down control, and data loading options
  - Uses two 3-input LUTs
    - One LUT generates counter data
    - Other LUT generates fast carry bit
    - Use 2-to-1 multiplexer for synchronous data loading, clear and preset for asynchronous data loading

Altera FLEX 8000 FastTrack Interconnect

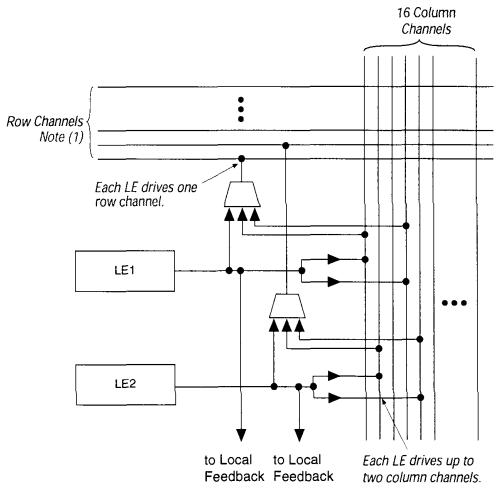


Figure from Altera technical literature

Note:
(1) See Table 4 for the number of row channels.

- Device-wide rows and columns
  - Each LE in LAB drives 2 column (total 16) channels, which connects… that column
  - Each LE in LAB drives 1 row channel, which connects to other LABs in that row
    - 3-to-1 muxs connect either LE outputs or column channels to row channels

Altera FLEX 8000 I/O Elements

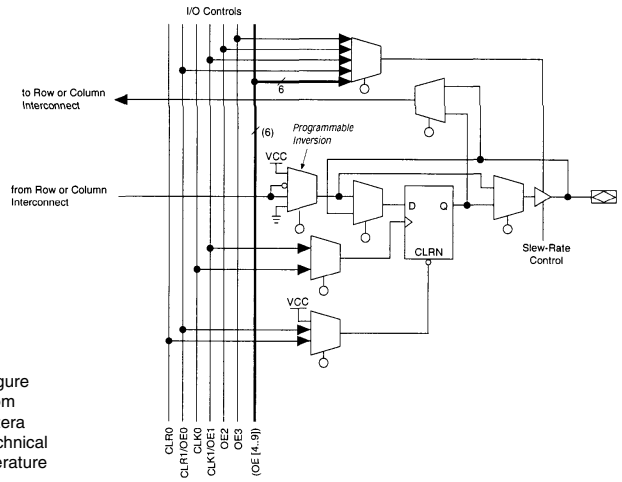


Figure from Altera technical literature

- Eight I/O Elements (IOEs) are at the end of each row and column
  - Some restrictions on how many row / column channels each IOE connects to
  - Contains a register that can be used for either input or output
    - Associated I/O pins can be used as either input, output, or bidirectional pins

Altera FLEX 8000 Configuration

- Loading the FLEX 8000's SRAM with programming information is called *configuration*, and takes about 100ms
  - After configuration, the device initializes itself (resets its registers, enables its I/O pins, and begins normal operation)
  - Configuration & initialization = command mode, normal operation = user mode
- Six configuration schemes are available:
  - Active serial — FLEX gives configuration EPROM clock signals (not addresses), keeps getting new values in sequence
  - Active parallel up, active parallel down — FLEX 8000 gives configuration EPROM sequence of addresses to read data from
  - Passive parallel synchronous, passive parallel asynchronous, passive serial — passively receives data from some host

Altera FLEX 10K Block Diagram

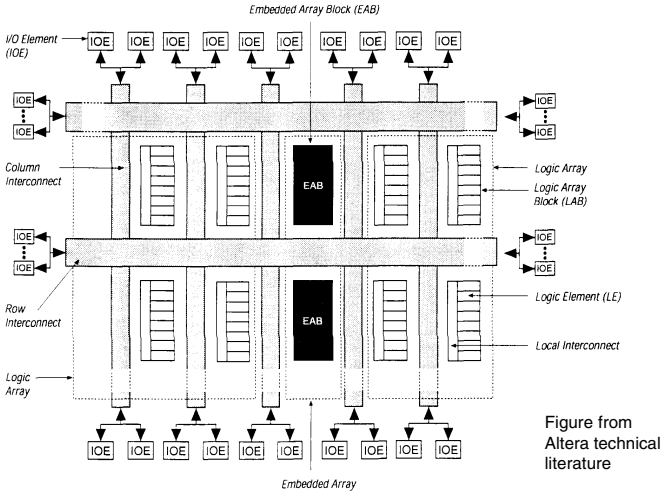


Figure from Altera technical literature

- FLEX 10K chip contains 72–1520 LABs
  - Each LAB contains 8 Logic Elements (LEs), so a chip contains 576–12,160 LEs, totaling 10,000–250,000 usable gates
- Each chip also contains 3–20 Embedded Array Blocks (EABs), which can provide 6,164–40,960 bits of RAM

Altera FLEX 10K Embedded Array Blocks (EABs)

- Each chip contains 3–20 EABs, each of which can be used to implement either logic or memory
- When used to implement logic, an EAB can provide 100 to 600 gate equivalents (in contrast, a LAB provides 96 g.e.'s)
  - Provides a very large LUT
    - Very fast — faster than general logic, since it's only a single level of logic
    - Delay is predictable — each RAM block is not scattered throughout the chip as in some FPGAs
  - Can be used to create complex logic functions such as multipliers (e.g., a 4x4 multiplier with 8 inputs and 8 outputs), microcontrollers, large state machines, and DSPs
  - Each EAB can be used independently, or combined to implement larger functions

Altera FLEX 10K
Embedded Array Blocks (cont.)

- Using EABs to implement memory, a chip can have 6K–40K bits of RAM
  - Each EAB provides 2,048 bits of RAM, plus input and output registers
  - Can be used to implement synchronous RAM, ROM, dual-port RAM, or FIFO
  - Each EAB can be configured in the following sizes:
    - 256x8, 512x4, 1024x2, or 2048x1
  - To get larger blocks, combine multiple EABs:
    - Example: combine two 256x8 RAM blocks to form a 256x16 RAM block
    - Example: combine two 512x4 RAM blocks to form a 512x8 RAM block
    - Can even combine all EABs on the chip into one big RAM block
    - Can combine so as to form blocks up to 2048 words without impacting timing

Altera FLEX 10K
Embedded Array Blocks (cont.)

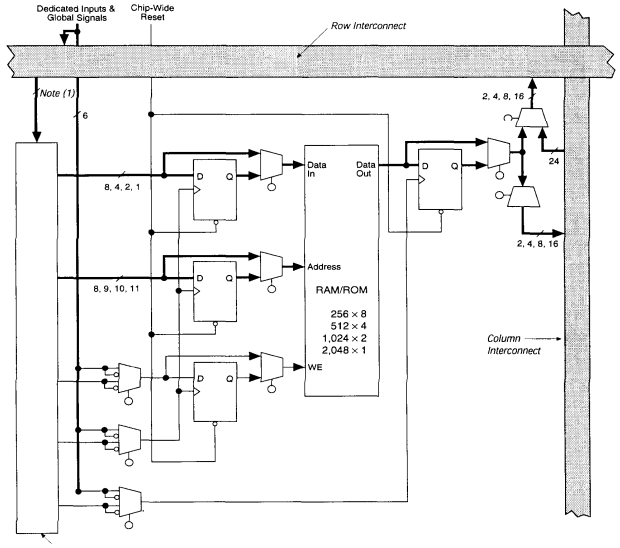


Figure from Altera technical literature

- EAB gets input from a row channel, and can output to up to 2 row channels and 2 column channels
- Input and output buffers are available