Altera FLEX 8000 Block Diagram (Review)

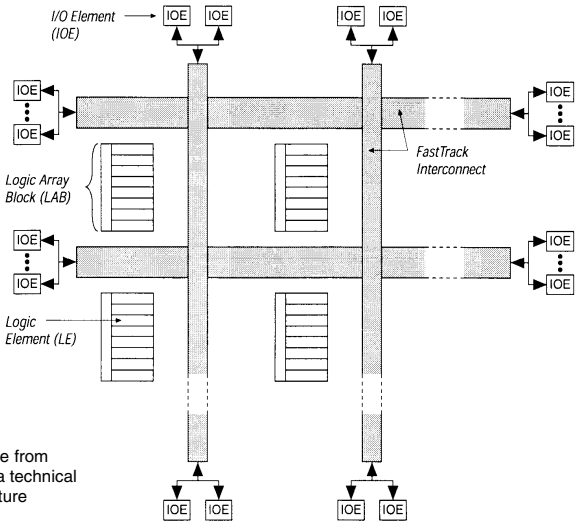


Figure from Altera technical literature

- FLEX 8000 chip contains 26–162 LABs
  - Each LAB contains 8 Logic Elements (LEs), so a chip contains 208–1296 LEs, totaling 2,500–16,000 usable gates
  - LABs arranged in rows and columns, connected by FastTrack Interconnect, with I/O elements (IOEs) at the edges

Altera FLEX 10K Block Diagram (Review)

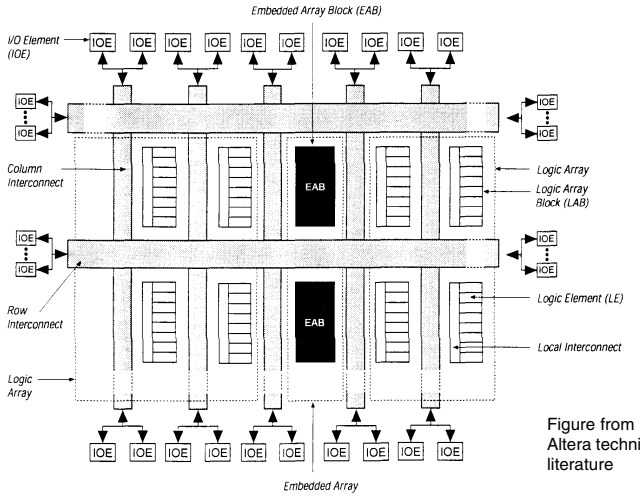


Figure from Altera technical literature

- FLEX 10K chip contains 72–1520 LABs
  - Each LAB contains 8 Logic Elements (LEs), so a chip contains 576–12,160 LEs, totaling 10,000–250,000 usable gates
- Each chip also contains 3–20 Embedded Array Blocks (EABs), which can provide 6,164–40,960 bits of RAM

Altera APEX 20K Overview

- APEX 20K chip contains:
  - 256–3,456 LABs, each of which contains 10 Logic Elements (LEs), so a chip contains 2,560–51,840 Les, 162,000–2,391,552 usable gates
  - 16–216 Embedded System Blocks (EABs), each of which can provide 32,768–442,368 bits of memory
    - Can implement CAM, RAM, dual-port RAM, ROM, and FIFO
- Organization:
  - MultiCore architecture, combining LUT, product-terms, & memory in one structure
    - Designed for “system on a chip”
  - MegaLAB structures,each of which contains 16 LABs, one ESB, and a MegaLAB interconnect (for routing within the MegaLAB)
    - ESB provides product terms ***or*** memory

APEX LABs and Interconnect

- Logic Array Block (LAB)
  - 10 LEs
  - Interleaved local interconnect (each LE connects to 2 local interconnect, each local interconnect connects to 10 LEs)
    - Each LE can connect to 29 other Les through local interconnect
- Logic Element (LE)
  - 4-input LUT, carry chain, cascade chain, same as FLEX devices
  - Synchronous and asynchronous load and clear logic
- Interconnect
  - MegaLAB interconnect between 16 LABs, etc. inside each MegaLAB
  - FastTrack row and column interconnect between MegaLABs

APEX Embedded System Blocks (ESBs)

- Each ESB can act as a macrocell and provide product terms
  - Each ESB gets 32 inputs from local interconnect, from adjacent LAB or MegaLAB interconnect
  - In this mode, each ESB contains 16 macrocells, and each macrocell contains 2 product terms and a programmable register (parallel expanders also provided)
- Each ESB can also act as a memory block (dual-port RAM, ROM, FIFO, or CAM memory) configured in various sizes
  - Inputs from adjacent local interconnect, which can be driven from MegaLAB or FastTrack interconnect
  - Outputs to MegaLAB and FastTrack, some outputs to local interconnect

Xilinx XC4000

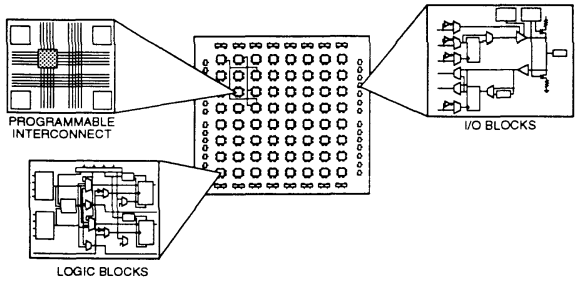


Figure from *Field-Programmable Gate Array Technology*, Trimberger, Kluwer, 1994

- Based on LUTs and SRAM programming
- Xilinx XC4000 chip contains a matrix of Combinational Logic Blocks (CLBs)
  - Chips range from 10x10 to 56x56 CLBs
  - Each CLB can be used for logic or RAM
    - Used entirely as logic, a chip provides 3,000–85,000 gates
    - Used entirely as RAM,a chip provides 3,200–100,352 bits of RAM
    - With "typical" usage of 20–30% RAM, a chip provides 2,000–55,000 gates

Xilinx XC4000 Combinational Logic Block

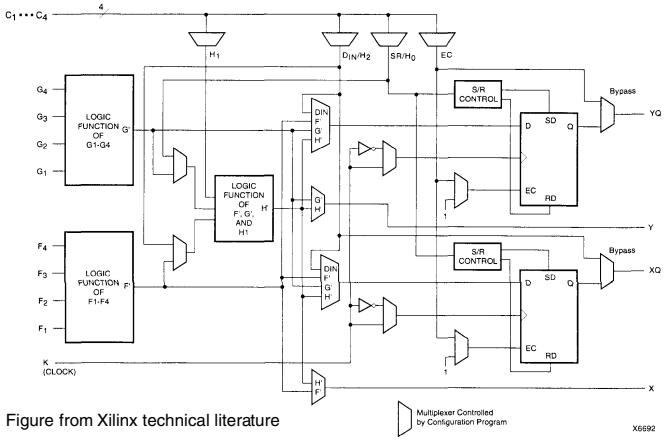


Figure from Xilinx technical literature

- Each Combinational Logic Block (CLB):
  - Two 4-input LUTs (called "function generators" F and G)
    - A 3-input LUT, which has 1–3 of its inputs coming from outside the CLB
    - CLB can implement two 4-variable functions, one 5-variable function, or some functions of up to 9 variables
  - Two edge-triggered D flip-flops

Xilinx XC4000 CLB Carry Logic

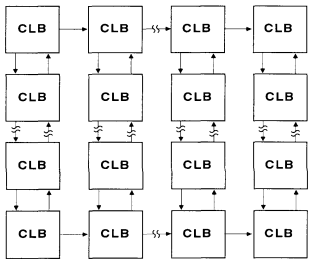


Figure 12: Available XC4000E Carry Propagation Paths

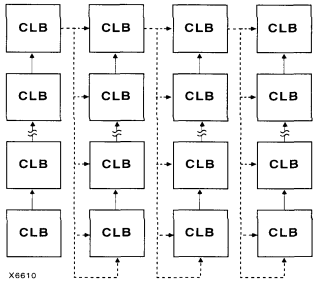


Figure 13: Available XC4000X Carry Propagation Paths (dotted lines use general interconnect)

Figure from Xilinx technical literature

- *Fast carry logic* provides carry and borrow signals
  - Not shown on previous slide, this computation occurs between CLB inputs and F & G LUTs
  - Results are propagated between CLBs
  - Flexibility is limited in high-capacity XC4000X series to improve speed
  - Allows high-speed address calculation, high-speed addition for DSP, etc.

RAM

- LUTs can be treated as RAM cells
- Single-port operation
  - Configure as either one 16x2 or 32x1 bit array (both LUTs), two 16x1 bit arrays (both LUTs), or one 16x1 bit array (one LUT; use the other as logic)
  - Each has a common read / write port
  - Synchronous (edge-triggered) operation
  - Asynchronous (level-triggered) operation
- Dual-port operation
  - Configure as one 16x1 bit array, using both LUTs
  - One write port, two read ports
    - Supports simultaneous read and write operations to same or different addresses
  - Synchronous (edge-triggered) operation

Xilinx XC4000 I/O Block

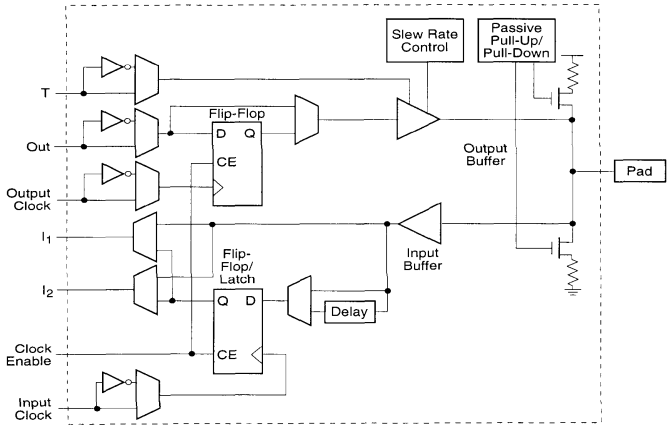


Figure from Xilinx technical literature

- Two I/O Blocks (IOBs) are at the end of each row and column
  - Each IOB contains an input register / latch and an output register / latch
  - Two inputs (to chip): direct & register
  - The associated I/O pin can be used as either an input, output, or bidirectional pin

Xilinx XC4000 Routing

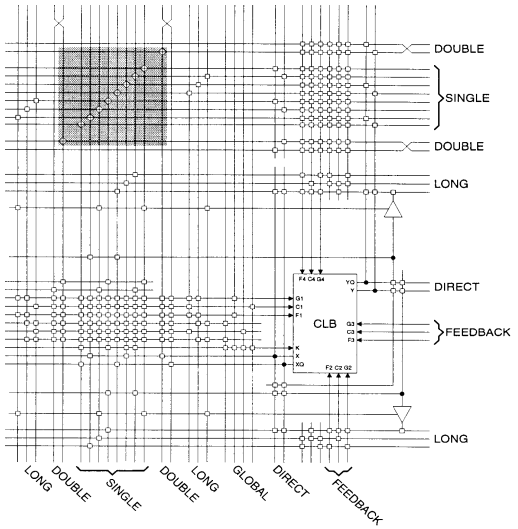
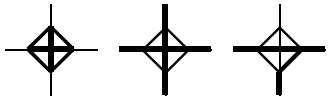


Figure from Xilinx technical literature

- Three kinds of interconnect:
  - Row and column routing
  - IOB routing, which forms a ring around the outside of the CLB array
  - Dedicated networks, primarily intended for clocks, but usable for other signals

Xilinx XC4000 Routing (cont.)

- CLB inputs and outputs connect to channels on all four sides, to provide maximum routing flexibility
- Switch matrix connects rows and columns
  - Six transistors per switch point



- CLBs connect to lines of various lengths:
  - Single-length lines — enter a switch matrix every row / column
  - Double-length lines — enter a switch matrix every two rows / columns
  - Longlines — for high fanout, time-critical nets, or nets that need to be distributed over much of the chip
  - XC4000X only:
    - Quad- and octal-length lines
    - Direct connections between adjacent CLBs

Xilinx FPGAs

- XCS00/XL (Spartan)
  - High volume ASIC replacement
  - 5v, 3v, 2,000–40,000 typical gates
- XC2S00 (Spartan-II)
  - High volume ASIC/ASSP replacement
  - 2.5v, 6,000–150,000 typical gates
- XC4000XLA, XC4000XL, XC4000XV
  - High density
  - 3v, 1,500–500,000 typical gates
- XCV00 (Virtex)
  - High density / performance
  - 2.5v, 34,000–1,124,000 typical gates