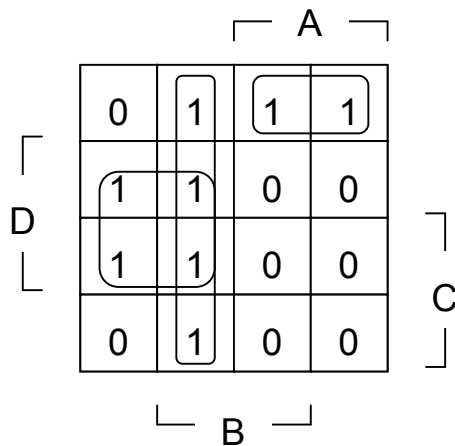
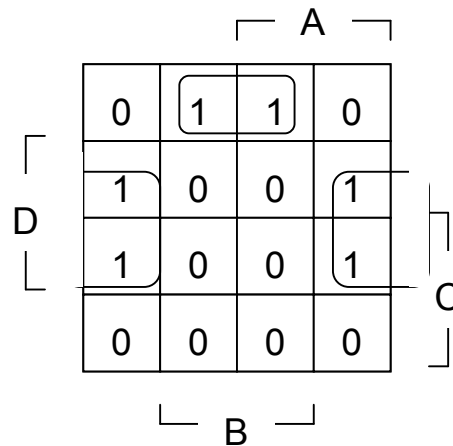


Wednesday 22 March 2006

1. Given the two 4-variable Karnaugh maps below, circle the 1's and write the minimized sum of products expression below each map. (16 points)



Output = $A'D + A'B + AC'D'$
(left to right)



Output = $B'D + BC'D'$
(wrap-around, middle top)

2. What functionality is provided by an S-R latch? Define its inputs and outputs and what happens for the various input combinations. (10 points)

An S-R latch can store a value and then hold that value until a new value is stored. Its inputs are S (“set”) and R (“reset”), and its outputs are Q and Q’ (complement of Q).

The latch is “set”, meaning a “1” is stored in the latch and made available at output Q, when input S=1 and R=0. The latch is “reset”, meaning a “0” is stored in the latch and made available at output Q, when input S=0 and R=1.

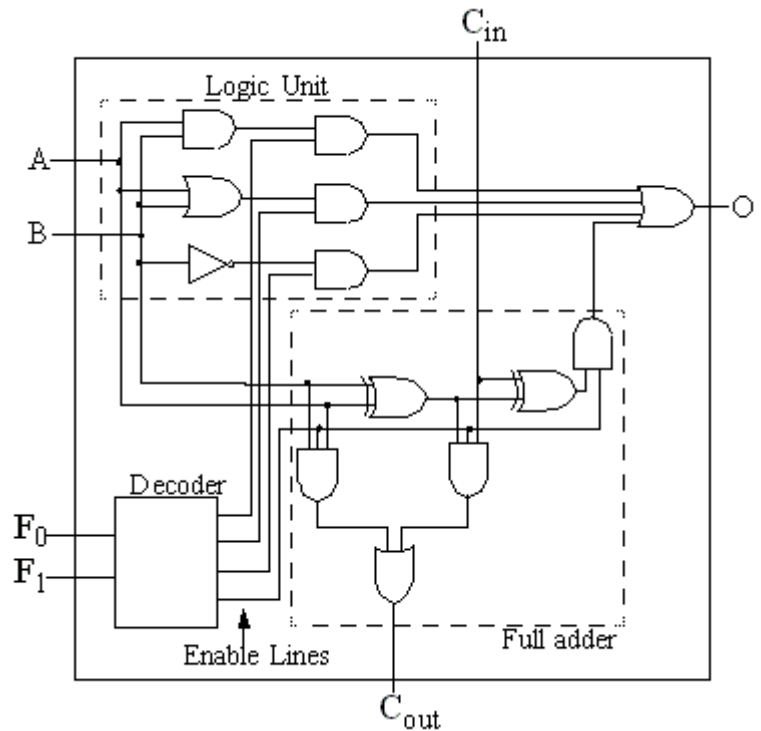
The latch holds the previous value and continues to make it available at output Q, when input S=0 and R=0. The input combination S=R=0 is considered forbidden, as it can lead to incorrect operation.

3. Consider the ALU shown to the right.

a. What functionality is provided by the Decoder? Be specific. (10 points)

The Decoder has two inputs, F_0 and F_1 , giving four input combinations. For each input combination, it puts a “1” on one of its outputs and a “0” on all its other outputs — essentially “enabling” that one output and “disabling” all the other outputs. (It can also be thought of as a 1-n demultiplexer, where the 1 input is hardwired to a value of “1”.)

In this ALU, four separate parts of the circuit compute $A \text{ AND } B$, $A \text{ OR } B$, $A \oplus B$, and $A+B$. The enable outputs of the Decoder are used to specify which part of the circuit gets to send its output to the output of the ALU.



b. The Decoder’s Enable Lines connect to AND gates. What functionality is provided by those AND gates? Be specific. (10 points)

The AND gates act as a switch, or water faucet. If the enable line input to an AND gate is 0, the output of the AND gate is always 0, regardless of the value of the other input to the AND gate. However, if the enable line input to an AND gate is 1, the output of the AND gate is the same as the other input. In this latter case you can think of the switch as being “enabled” or the water faucet turned on.

4. Consider a digital circuit for a consumer electronic product, which could be implemented using either a full-custom ASIC, standard-cell-based ASIC, or FPLD.

a. Which implementation style has the potential to yield the highest-performance circuit, and why? (7 points)

The full-custom ASIC. Standard-cell-based ASICs and FPLDs are implemented using generic pre-defined modules supplied by the manufacturer, whereas modules in full-custom ASICs can be optimized more carefully for higher performance in the specific application at hand.

b. Which has the potential to get the product to market the fastest, and why? (7 points)

FPLDs, since the design need only be loaded into pre-manufactured chips, as opposed to having to send an ASIC design’s netlist to a fabrication facility and wait weeks for the chips to be produced.

5. On the Altera UP1 Education Board, the push buttons are “active low”. What does that mean? (5 points)

When the button is pressed (i.e., becomes “active”) it produces a logic “0” — a “low” signal. Otherwise, the output is a logic “1”.

6. Consider the following AHDL code fragment:

```

SUBDESIGN mealy
{
  clock, reset, y: INPUT;
  z: OUTPUT ;
}
VARIABLE
  ss: MACHINE WITH STATES (s0, s1, s2, s3);
TABLE
  ss, y => z, ss;
  s0, 0 => 0, s0;
  s0, 1 => 1, s1;
  ...
END TABLE;

```

- a. Explain what the two lines enclosed in the box do. Be specific. (10 points)

The left-hand-side specifies the current state and value of input “y”, while the right-hand-side specifies the output “z” and the next state.

Thus those lines say that if the current state is s0 and input y is “0”, the output z should be “0” and the machine should stay in state s0, but if the current state is s0 and input y is “1”, the output z should be “1” and the machine should go to state s1.

- b. Would the operation of the circuit change if the lines enclosed in the box were interchanged? Explain. (10 points)

The operation would not change; concurrent statements like these can be specified in any order. The order is usually chosen so as to make the description as readable as possible.

7. Consider the following AHDL code fragment from the keypad encoder in Salcic Chapter 5:

```
mux.d[3..0] = col[3..0];  
mux.(b,a) = counter.(qb, qa);  
key_pressed = !mux.y;
```

Explain what this code fragment does. Be specific. (15 points)

Line 1: The keys on the keypad are organized into columns numbered 3 to 0, and the output of each column is connected to the 4 inputs of a multiplexor. If a key is pressed in a particular column, that value goes from the output of that column to the corresponding input of the multiplexor.

Line 2: Two bits of a four-bit counter are used to drive the multiplexor control inputs, so that as the counter operates, the control inputs change from 00 to 01 to 10 to 11, selecting each column of the keypad in turn.

Line 3: The (active-low) value in the selected column goes through the multiplexor where is inverted and assigned to key_pressed. Thus if a key is pressed in the selected column, a 0 goes through the multiplexor, and a 1 is assigned to key_pressed, indicating that a key was pressed in that column.