

Name: _____

CS 4/55111

Final Exam

VLSI Design

Monday 8 May 2006

1. VHDL divides the description of a module into an Entity and an Architecture section.
 - a. What is the purpose of each of these two sections? (10 points)

- a. Would it ever make sense to have multiple alternative Architecture sections for a single Entity section? Explain. (5 points)

Name: _____

2. What is a STD_LOGIC type? (10 points)

3. Are statements in VHDL concurrent (like in AHDL) or sequential (like in C or Java)?
Explain. (10 points)

Name: _____

4. Consider the following two VHDL code fragments:

```
PROCESS
BEGIN
  WAIT UNTIL (Clock'EVENT AND Clock='1');
  IF reset='1' THEN
    Q2 <= '0';
  ELSE
    Q2 <= D;
  END IF;
END PROCESS;
```

```
PROCESS (Reset, Clock)
BEGIN
  IF reset='1' THEN
    Q3 <= '0';
  ELSEIF (Clock'EVENT AND Clock='1') THEN
    Q3 <= D;
  END IF;
END PROCESS;
```

How do these two code fragments differ? Be specific. (15 points)

Name: _____

5. It is easy to write code in VHDL that is syntactically correct, but that will not generate the expected hardware once it is compiled onto an FPGA. Explain, preferably with an example or two. (10 points)

6. Compare the relative sizes of the programming points in field-programmable logic device that use antifuse, EEPROM, and SRAM programming technologies. (10 points)

Name: _____

7. How does the local interconnect and sharing of functionality between the macrocells inside an Altera MAX LAB compare to that between the LEs within an Altera FLEX LAB? (20 points)

Name: _____

8. Consider the FLEX 8000 I/O element shown to the right. What functionality is provided by the multiplexor on the right side of the figure (shown shaded with a thick border)? Be specific. (10 points).

