Topic 8: Sequential Circuits

Readings :

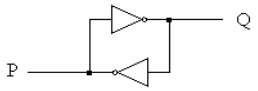
Patterson & Hennesy, Appendix B.4 - B.6

Goals

- Basic Principles behind ***Memory Elements***
- ***Clocks***
- ***Applications*** *of sequential circuits*
- Introduction to the concept of the ***State Machine***

Bistable Devices

Consider the following element



This device exhibits two stable states (bistable)

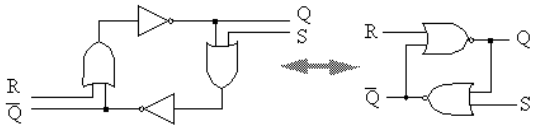
If P=0(Reset), then Q=1(Set).

If P=1(Set), then Q=0(Reset).
So , $P = \overline{Q}$

It is able to retain the two states, Set & Reset indefinitely.

This is a memory cell, but there is no way to set it!

Solution : Add OR gates to make it set-able.



- The circuit on the right is called an S-R Latch (Set-Reset Latch)
- The value of the output Q and its complement represent the stored state.
- R, S are the inputs of the Latch

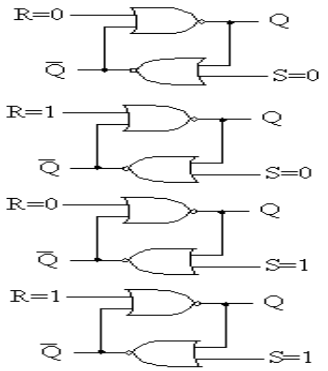
S-R Latches

Four possible cases (inputs) :
RS = 00, 01, 10, 11

Reminder : For a NOR gate, if any input is 1 then the output is 0.

Truth table

R	S	Q	Q'
0	0	1/0	0/1
0	1	1	0
1	0	0	1
1	1	0	0



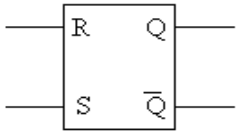
S-R Latches

RS Latch summary

- Q is value stored in memory latch
- RS = 00 is "Hold" condition
- RS = 01 is " Set" condition (force Q=1)
- RS = 10 is " Reset" condition (force Q=0)
- RS = 11 is " Forbidden"

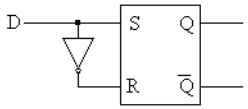
  It can lead to incorrect operation : oscillation or "metastability".
  Q is not the complement of Q' .

Symbol



Problems and Solutions

Problem : What to do about R=S=1
Solution : Don't let it happen. Tie together inputs with an inverter.

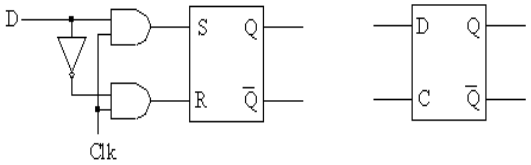


Now we cannot get R=S=1, but :

Problem : We cannot get R=S=0 ("Hold" condition)
Solution : Use "Clock" input.

Result : Clocked D-latch (No clock = hold)

D-Latch



Q(t)	Q(t+1)	D
0	0	0
0	1	1
1	0	0
1	1	1

Necessary topic before we proceed :
"Clocks"

Definition :

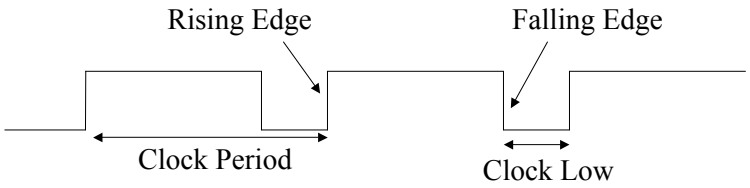
Clock is a free-running signal with a fixed ***Cycle Time*** or ***Clock Period.***

Clock Frequency = 1/Cycle Time

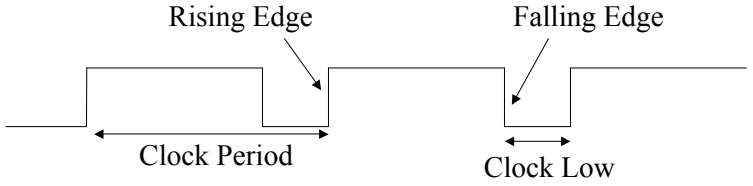
The clock period is divided into two portions:

- Clock is "High"
- Clock is "Low"

- Rising Edge : Transition from Low to High
- Falling Edge: Transition from High to Low



•The duration of "High" and "Low" parts of the clock cycle need not be the same.
•Duty cycle : Fraction of the Period, when the signal is considered active.
•Edge Triggered clocking : All state changes occur at a clock edge.



Edge-Triggered Methodology :

Either the Rising or the Falling Edge of the Clock is considered ***Active = Causes state changes to occur.***

Constraint of Clocked or ***Synchronous Systems*** **:**

Signals must be ***Valid*** when the active clock edge occurs.

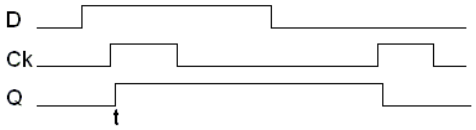
Valid = Stable (not changing) for a short period before and after the edge rise or fall.

Return to the *D-latch*

Clk=0 ; Nothing happens ("Hold" condition)
•Ck = 0 equivalent to (S=0 and R=0)

Clk=1 ; read D into Latch. Update value until C changes to 0.
•Ck = 1 equivalent to S=D and R=D'

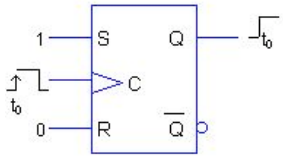
Operation (assuming output is initially deasserted, ie Low)



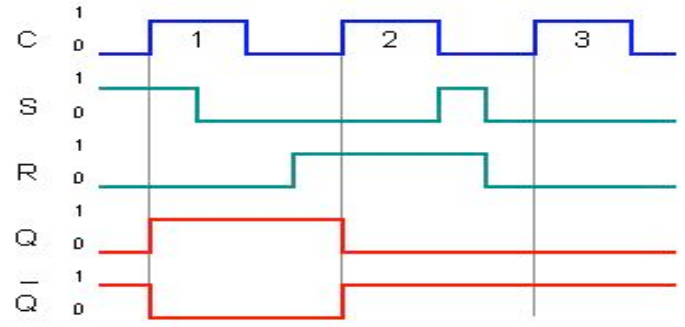
Note : NOT an Edge-Triggered D-Flip-Flop

Edge Triggered S-R Latch

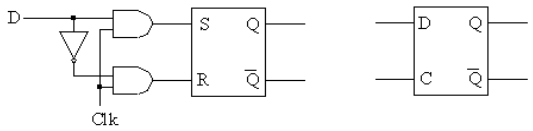
Different Approach

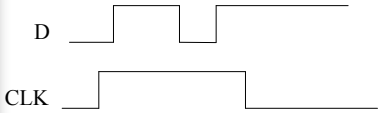


Inputs			Outputs		
S	R	C	Q	Q'	Comments
0	0	↑	Q	Q'	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	?	?	Invalid



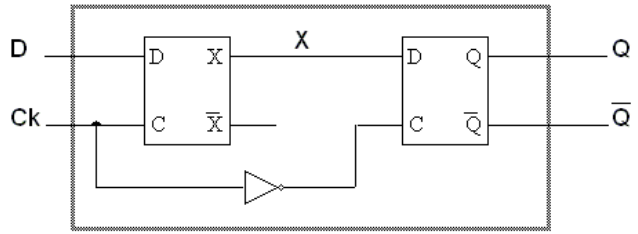
Race Condition : For a D-Latch, if the input changes state, while the clock is still high, then there will be an additional change to the output, although the data to be written was the former value.





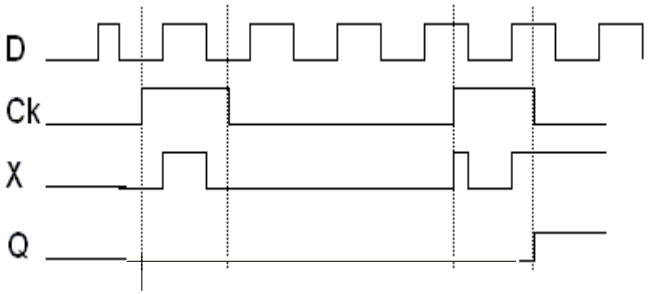
Solution to race condition: ***Master/Slave Flip-Flop***

Also : *Remember the previous reference to the edge triggered S-R*

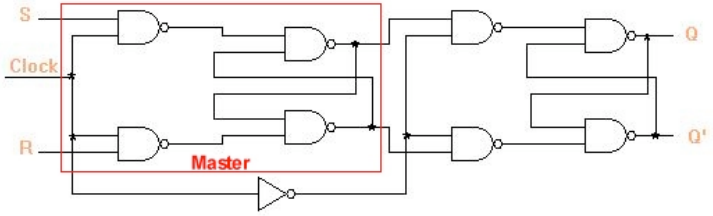


This is a ***Falling-Edge Triggered Master/Slave D Flip-Flop.***

The first Latch, called the Master, follows the input D when the Clock input is asserted. When Ck falls , X is closed and the second latch, called the slave, is open and gets the input from the output of the master latch.



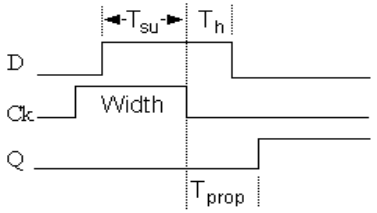
S-R Latch Master/Slave



Edge Triggered devices = Flip Flops

•The Actual circuit is more complex than shown above!

•Characteristics:
- •Setup time (Tsu)
- •Hold time (Th)
- •Propagation Delay (Tprop)
- •Minimum clock width
- •... all are relative to clock edge

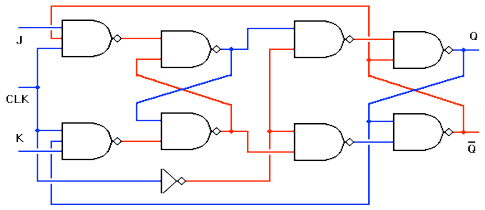


For a 74LS74:
T_{su} = 20 ns
T_h = 5ns
Min Clock Width = 25 ns
T_{prop} (max/typical)
low to high: 25/13
high to low: 40/25

Applications :

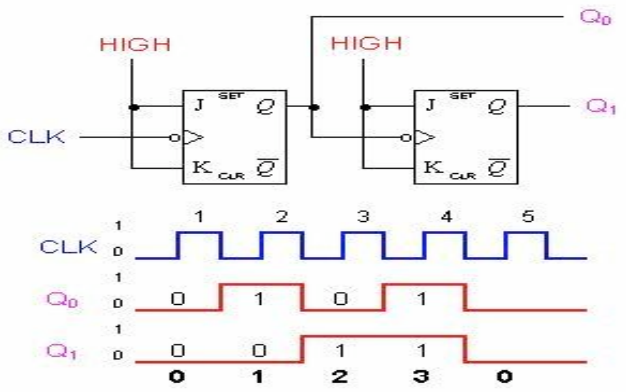
First, introduce another Flip-Flop Type :

J-K Flip-Flop

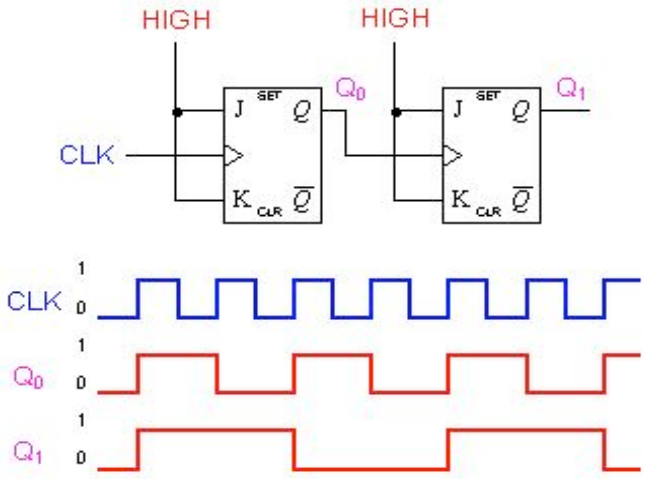


Inputs			Outputs		
J	K	C	Q	Q'	Comments
0	0	↑	Q	Q'	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	Q'	Q	Toggle

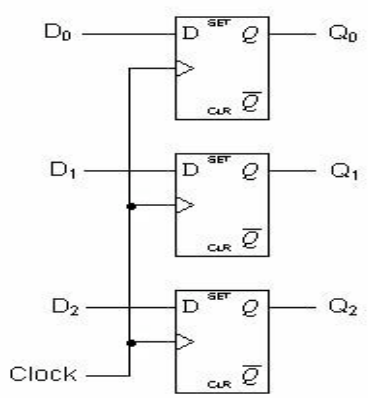
•*Counter*



•*Frequency Divider*



•*Parallel Data Storage*



The Basic Idea Behind Registers