Subtraction

Add: input A and B, Cin=0
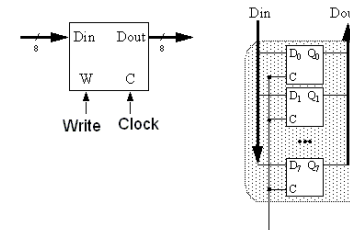
Subtract: input A and B, Cin=1

How come? remember two's complement...

Building Registers

Abstraction:
- Inputs: data[N], clock, write-enable
- Output: data[N]

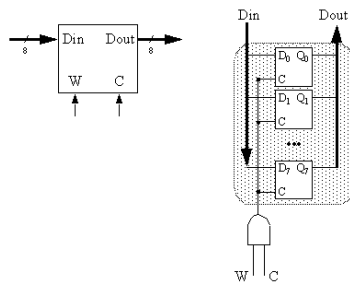Using D Flip-flops, we almost get it (e.g., 8 bit register):

Problem: How do we do write-enable?

N-bit Registers

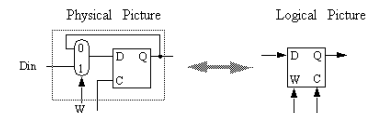**Implementing write-enable**

Solution 1: Gate clock.

What are the problems with this solution?

N-bit Registers

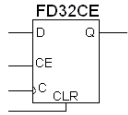Solution 2: Use multiplexor (MUX):

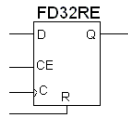By connecting together N of the writable D Flip-flops, N bit register can be implemented.

N-bit Register

Solution 3: Use special FF that have enable "built-in"
   •Xilinx FD32CE (Flip-flop, Data input, Clear input, clock Enable):

```
     FD32CE
   ┌─────────┐
  ─┤D      Q ├─
   │         │
  ─┤CE       │
   │         │
  ─┤C        │
   │  CLR    │
   └─────────┘
```

   Xilinx FD32RE (Flip-flop, Data input, Reset input, clock Enable)

```
     FD32RE
   ┌─────────┐
  ─┤D      Q ├─
   │         │
  ─┤CE       │
   │         │
  ─┤C        │
   │  R      │
   └─────────┘
```
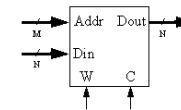
   Remember: never gate clocks!

Register Files

Abstraction
   •holds 2M (e.g., M=4, 24=16) registers.
   •Inputs: Register Number [M], Din [N], Clock, Write-enable
   •Outputs: Dout[N]

```
        ┌──────────┐
   ─────┤Addr  Dout├─────
    M   │          │  N
   ─────┤Din       │
    N   │          │
        │  W    C  │
        └──────────┘
           ▲    ▲
```
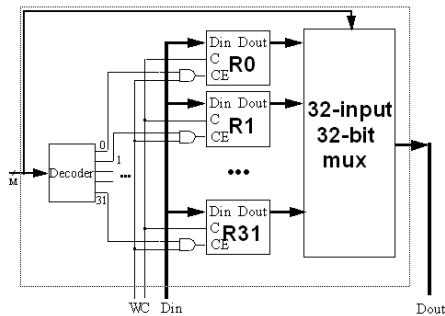
Example:
   •Addr=0011, W=0
   Dout = Reg[3]
   •Addr=0101, W=1, Din=0xFF
   Reg[5] = 0xFF at clock

Register File with mux

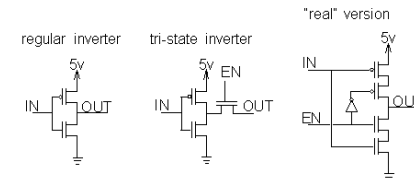How to select a register

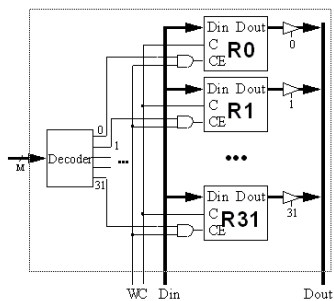## Tri-state outputs

Normal outputs can be 0 or 1

Tri-state outputs can also be *off* ("disabled", on: "enabled")

This allows many outputs to be wired together
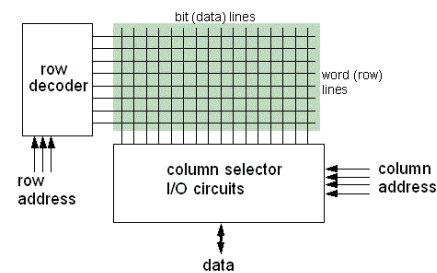   •as long as only *one* is enabled at a time!

Register File with tri-state

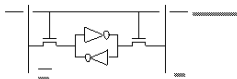Hint: For HOT314 we will implement the register file using a RAM.

What goes in a RAM?

Example: 128 x 1-bit memory *(128=8*16)*

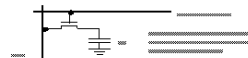## SRAM Cells

6-T static RAM cell

Read:
  •pull bit + bit to Vcc
  •pull 1 row select high
  •cell pulls bit or bit low
  •sense amp detects differential signal between bit and bit

Write:
  •pull 1 row select high
  •drive bit and bit to flip cell

DRAM Cells

1-T dynamic RAM cell

Read:
  •pull bit Vcc/2
  •pull 1 row select high
  •cell "nudges" bit low or high
  •sense amp detects difference to a reference bit line

Write:
  •pull 1 row select high
  •drive bit line to charge/discharge capacitor