CS 4/55111 **Project #2** **VLSI Design**

Due to Prof. Walker by 5:30pm on Wednesday 1 March 2006
this project counts as 10% of your course grade

1. Do **Lab Exercise 4 on page 61** of *Rapid Prototyping of Digital Systems, Second Edition* ("Build a stopwatch with the following modifications…") using the FLEX chip on the UP1 board. Turn in:
   a) a description of your design and any design decisions that you made in your implementation (15 points)
   b) a readable (not microscopic) printout of the schematic (5 points)
   c) a printout of the test inputs and simulation output that shows that that the circuit works as expected, annotated to explain the operation of the circuit (15 points)
   d) a signature on the statement below by Prof. Walker, by the TA (Kevin Schaffer), by one of Prof. Walker's research students listed on the door of the lab, or by ***two*** other students in the class (15 points):

      I certify that _____ has successfully downloaded this design to a UP1 board and the design works correctly.

      _____ Name _____ Date

      _____ Name _____ Date

2. Do **Lab Exercise 4 on page 61** of *Rapid Prototyping of Digital Systems, Second Edition* ("Build a stopwatch with the following modifications…") using the MAX chip on the UP1 board. Turn in:
   a) items (a) through (c) similar to those in problem 1 above (35 points)
   b) a signature on the statement below by Prof. Walker, by the TA (Kevin Schaffer), by one of Prof. Walker's research students listed on the door of the lab, or by ***two*** other students in the class (15 points):

      I certify that _____ has successfully downloaded this design to a UP1 board and the design works correctly.

      _____ Name _____ Date

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4.8 Testing the Modified Design on the UP 1 Board.

Verify that your schematic has the same connections as seen in Figure 4.8. Compile the design and download the design to the UP 1 board. Hit the left FLEX pushbutton several times to clock the counter and watch the seven-segment displays as it counts up. It should now count only once when the pushbutton is hit. The UP1core functions dec_7seg, clk_div, and debounce will be useful in future design projects using the UP 1 board. They can be used in any VHDL, Verilog, schematic, or AHDL designs by using the graphical editor and UP1core symbols.

4.9 Laboratory Exercises

1. Simulate the initial design without the switch debounce circuit by setting up an initial reset pulse and a periodic 200 ns clock input in the simulator. In sequential simulations, turn on the **check setup and hold** option before running the simulator. This will check for flip-flop timing problems that would otherwise go undetected in the simulation.

2. Modify the counter circuit so that it counts down or up depending on the state of FLEX DIP switch 1. FLEX DIP switch 1 is connected to pin 41.

3. Modify the counter circuit so that it parallel loads a count value from the eight FLEX DIP switches on the UP 1 board when PB2 is pushed. Since the FLEX DIP switch inputs are only used when PB2 is hit, they do not need to be debounced. Here are the pin connections for the FLEX DIP switches.

Input Pin	Pin
FLEX_switch_1	41
FLEX_switch_2	40
FLEX_switch_3	39
FLEX_switch_4	38
FLEX_switch_5	36
FLEX_switch_6	35
FLEX_switch_7	34
FLEX_switch_8	33
(1 = Open, 0 = Closed)	

4. Build a stopwatch with the following modifications to the design. Disconnect the counter clk line and connect it to the clock_10hz pin on the clock_div symbol. Clock a toggle flip-flop with the pb_debounced output. A toggle flip-flop, tff, can be found in the prim symbol library. A toggle flip-flop's output changes state every time it is clocked. Connect the output of the toggle flip-flop to the GN line on the counter. The count should start and stop when PB1 is hit. Elapsed time in tenths of seconds should be displayed in hexadecimal. Pushing PB2 should reset the stopwatch.