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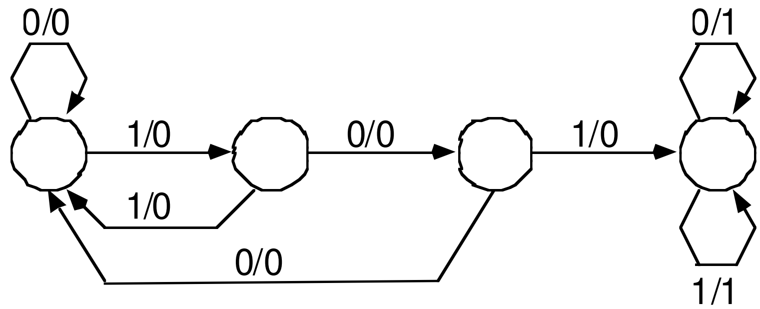
CS 4/55111 # Final Exam **VLSI Design**

Monday 11 May 1998

1. (10 points) Which is cheaper, a standard-cell-based or an FPLD-based implementation of a design? Explain your answer.

2. (15 points) Briefly explain the difference between a VHDL entity and a VHDL architecture, and also explain why there might be a need for multiple architectures that correspond to a single entity.

3. (25 points) The state diagram below defines a state machine to recognize the bit pattern “101”. If the input is named “bit” and the output is named “correct”, a label of the form x/y indicates that the state transition is made when “bit” has the value “x”, and that “y” is output on “correct”.



In the space below, write AHDL code for this state machine. Every detail of the syntax need not be correct, but the code should be as complete as possible.

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4. (50 points) A product brief accompanying this exam describes the ORCA OR3 family of field-programmable gate arrays, available from Lucent Technologies (formerly Bell Labs).

   a. (15 points) How is this family of devices *similar* to the Altera FLEX 10K family, in terms of programming, base cell architecture, special features, etc.?

b. (15 points) How is this family of devices *different* from the Altera FLEX 10K family, in terms of programming, base cell architecture, special features, etc.?

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c. (20 points) Suppose you work for a company, and you have been using the Altera MAX+PLUS II tools and the Altera FLEX 10K family for the past two years in your designs. What factors might influence you to change to Lucent's ORCA OR3 family for your next design?