Types of ASICs

- IC contains a *chip* ("die") cut from a *wafer*
  - Transistors, wires, etc. are built up on the chip in a series of layers (10-15 layers)
  - A *mask* is used to define the components of a layer as they are applied to the chip
- Types of ASICs (and pizza equivalent)
  - Full-custom ASIC
    - Pizza built from scratch, takes a long time to prepare and cook
  - Standard-cell-based ASIC
    - Custom-built from predefined selection, takes a long time to cook
  - Gate-array-based ASIC
    - Pre-cooked crusts, predefined selections, cooks quickly, somewhat cheaper
  - Field-programmable logic device
    - Frozen pizza — limited selection, cook it yourself at home, very cheap

Full-Custom ASICs

- Engineer designs some or all of the logic cells, circuit, and layout
- Mostly used:
  - If no pre-designed cells are available (e.g., new or highly specialized circuit)
  - If high-performance, less area, lower power, etc. is needed
- Fabricated in batches of 5 to 30 *wafer lots*, each wafer containing 10–100 chips
- Various technologies used (details later):
  - Bipolar — legacy from analog circuits, more consistent characteristics of components across chip / wafer
  - CMOS — more widely available, lots of cells and tools, wave of the future (at least for now)

Standard-Cell-Based ASICs

- Chip is built from pre-defined logic cells (gates, adders, etc.) called *standard cells*
  - Standard cells are built by someone else using full-custom design techniques
  - Save time, money, and risk by using a predesigned, pretested *cell library*
    - But — have to pay for the cell library
  - Also use larger cells (microprocessors, etc.) called *mega cells* (sometimes *cores*)

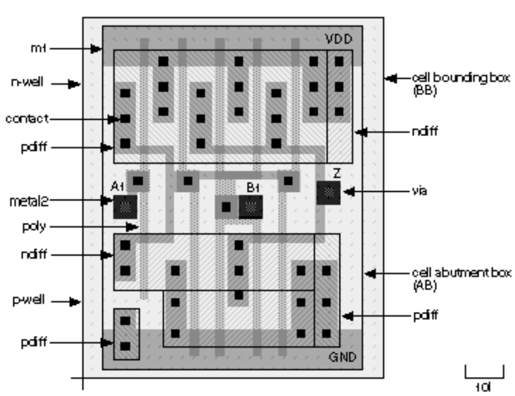

Figure from *Application-Specific Integrated Circuits*, Smith, Addison-Wesley, 1997

Standard-Cell-Based ASICs (cont.)

- Cells fit together like bricks in a wall — rows of (variable-width) cells
  - Most interconnect goes in *channels* between rows
  - Some cells may be designated as *feedthroughs* between rows
  - Other *metal layers* also provide interconnect
    - Connection between layers is called a *via*

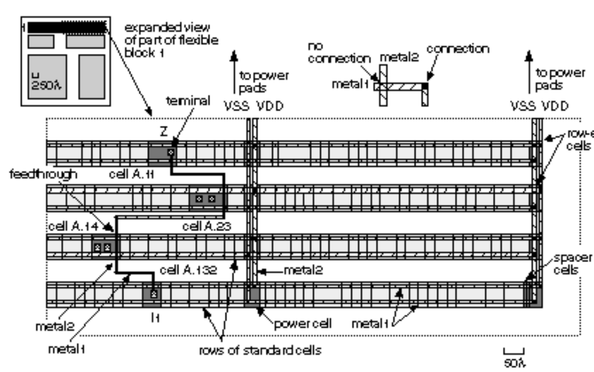

Figure from *Application-Specific Integrated Circuits*, Smith, Addison-Wesley, 1997

Gate-Array-Based ASICs

- Transistors are predefined in a fixed pattern on the chip
  - Interconnect is defined by designer and fabricated using a custom mask
  - Designer chooses cells from a gate-array library of predefined, pretested cells
- Chip is partially fabricated (cells, power, etc. added) and then stockpiled
  - When design is received for fabrication, the remaining metal layers are added
  - Cheaper — everyone shares cost of producing high volume of initial chip
  - Quick turn-around — days, couple weeks
- Variations:
  - Channeled gate arrays
  - Channelless gate arrays

Programmable Logic Devices (PLDs)

- Standard ICs, available in standard configurations, sold in high volume
  - But can be configured / programmed to create a specialized device
  - No customized cells or masks, just a single large block of programmable interconnect
  - Fast turn-around time
- Examples
  - Mask-programmable ROM — programmed when ordered
  - Programmable ROM — programmed electrically, erased electrically or using ultraviolet light, all by customer
  - PAL, PLA — 2-level sum-of-products and/or array, programmed electrically by customer (blowing fuses in array)

Field Programmable Logic Devices (FPLDs)

- Known by a variety of names:
  - Field-Programmable Gate Array (FPGA)
  - Field-Programmable Logic Device (FPLD)
  - Complex Programmable Logic Device (CPLD)
- Similar to PLDs, but more complex
  - No customized mask layers
  - Some method for programming the base logic cells and the interconnect
  - Core is a regular array of programmable logic cells, each of which contains combinational and sequential logic
  - Programmable interconnect surrounds the logic cells
  - Design turn-around is on the order of hours