Schematic Entry

- Circuit schematics are drawn on *schematic sheets*, which come in standard sizes (8.5x11, 11x17, etc.)
  - Each sheet includes a labeled border, and a block listing the circuit name, designer's name, date, etc.
  - There are standards for most of the commonly-used symbols
- Terms used in circuit schematics:

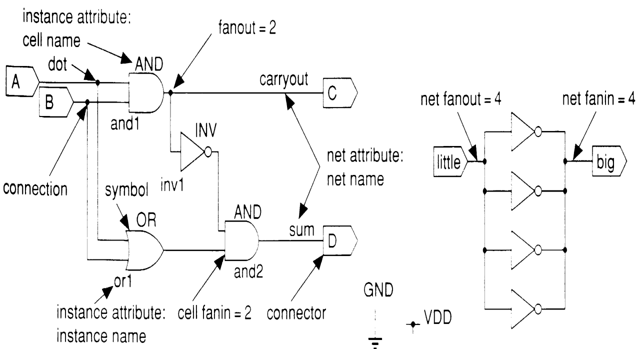


Figure from *Application-Specific Integrated Circuits*, Smith, Addison-Wesley, 1997

Hierarchical Design

- *Hierarchy* is used to reduce the size and complexity of the schematic
  - The alternative — drawing all symbols on one giant schematic with no hierarchy — is called a *flat schematic*
    - Flat schematics are impractical to work with for even thousands of components
    - Flat netlists, however, are occasionally used when the hierarchy isn't relevant

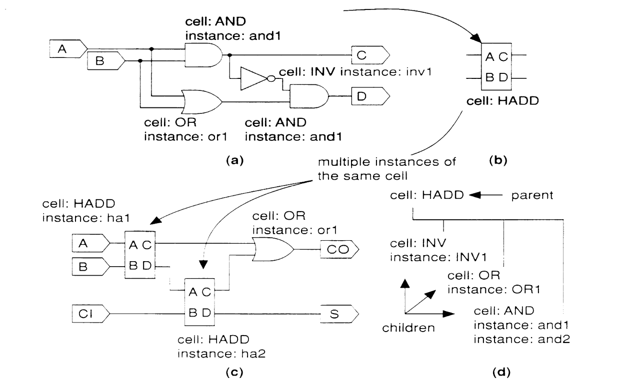


FIGURE 9.3 Schematic example showing hierarchical design. (a) The schematic of a half-adder. the subschematic of cell HADD. (b) A schematic symbol for the half adder. (c) A schematic that uses the half-adder cell. (d) The hierarchy of cell HADD.

Figure from *Application-Specific Integrated Circuits*, Smith, Addison-Wesley, 1997

Cell Library

- *Components* (sometimes called *modules*) in an ASIC schematic are chosen from a library of cells
  - ASIC vendors provide a schematic library of primitive gates for schematic entry
- Problem — no standard exists
  - Individual vendors might use different names to refer to a 2-input xor gate
    - May be some variation on TTL 7400-series names:
      - 2-input NAND = 7400
      - 2-input AND = 7408
      - 2-input OR = 7432
      - 2-input XOR = 7486
    - May be more descriptive:
      - nand2, xor3, …
  - Behavior may vary
    - Which input does 2-input multiplexor select when select input S = 0?

Names

- Each cell, whether a primitive cell or a subschematic, has a name
  - Each use of a cell in a schematic is a different *instance* of that cell, and is given a unique *instance name*
- Each cell is represented by a picture, or icon, called a *symbol*
  - Primitive cells (e.g., AND gates) have standardized non-rectangular symbols
  - Subschematics are represented by special custom icons

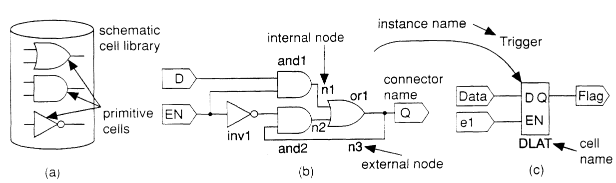


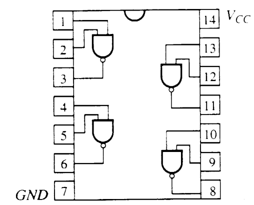
Figure from *Application-Specific Integrated Circuits*, Smith, Addison-Wesley, 1997

Nets

- Cell instances have *terminals*, also known as pins, connectors, or signals, that are the inputs and outputs of the cell
- Cell instances are connected by *wire segments*, commonly called *nets*
  - A *local* (internal) net is internal to a cell
  - An *external* net connects to the inputs and / or outputs of the cell
- Nets may sometimes be collected together into *buses* for convenience
  - May be represented by a thicker line on the schematic, with some indication of number of nets involved
  - Individual nets can still be accessed when necessary

Components

- Each symbol on the schematic may correspond to a *component*, which may contain component parts
  - An example of a component is a SN74LS00N device, which contains four 2-input NAND gates (component parts)
- A printed circuit board (PCB) may contain some number of ICs
  - If the IC is in a dual-in-line (DIP) package, the pins are numbered counter-clockwise from the upper-left corner when looking down on the package



(a) 7400

  - The schematic may indicate which cell instances belong to the same component, and which component pins are assigned to each component terminal

Some "Features" of a Schematic Entry Tool

- Windows, mouse, online help, ability to undo commands, etc.
- Design manager / library manager to allow users to create their own libraries; some make-equivalent to keep track of dependencies between files
- Keep track of different versions of a file; append version number to the file name
  - Perhaps more complex version control, where users "check out" design files
- Rubber-banding — drag the cursor, and the wire follows, automatically bending at right angles where appropriate
  - Move components, wires are repositioned appropriately
- Visual feedback (dot) for connections