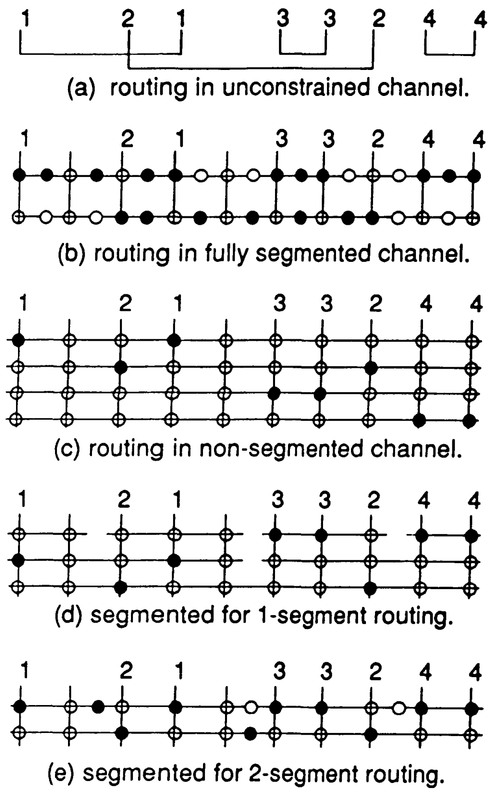
Antifuse Routing



(a) routing in unconstrained channel.

(b) routing in fully segmented channel.

(c) routing in non-segmented channel.

(d) segmented for 1-segment routing.

(e) segmented for 2-segment routing.

Figure from *Field-Programmable Gate Array Technology*, Trimberger, Kluwer, 1994

Antifuse Routing (cont.)

- Fully segmented
  - Switch at every cross point normally passes signals through vertically and horizontally, but can connect the vertical and horizontal tracks
  - Antifuse connects or disconnects the segments of the horizontal channel
- Non-segmented
  - Excessive area requirements
- 1-segment routing
  - Divides the tracks into segments of varying lengths, which allows each net to be routed in a track of more or less the appropriate size
- 2-segment routing
  - Allows track segments to be joined

Actel ACT Routing Architecture

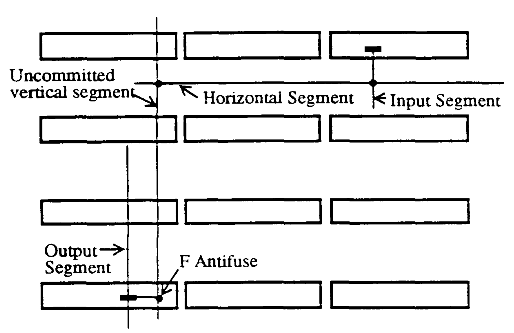


Figure 3.3.4. Routing Using Long Vertical Track (LVT)

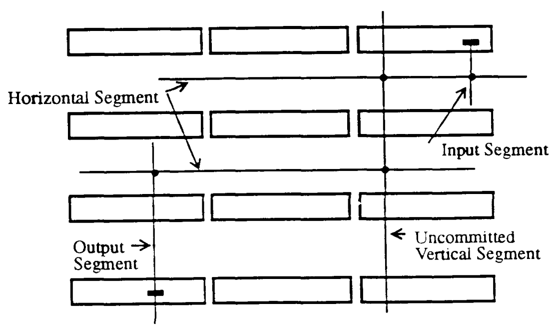


Figure 3.3.5. Routing Using LVTs in another Column

Figure from *Field-Programmable Gate Array Technology*, Trimberger, Kluwer, 1994

Actel ACT Routing Architecture (cont.)

- An Actel FPGA has rows of cells, with horizontal channels between them
  - It also has vertical "channels", but those aren't called channels
- Cell inputs must come from an adjacent horizontal track (see either figure)
- Cell outputs must attach to a vertical track (see bottom figure)
  - Vertical tracks span only two channels above and below the cell
  - Additional vertical segments of varying lengths are also provided, and they can be joined together to form vertical segmented tracks
    - Long vertical tracks— see top figure, where output goes to LVT instead of its dedicated output segment

Actel ACT Routing Architecture (cont.)

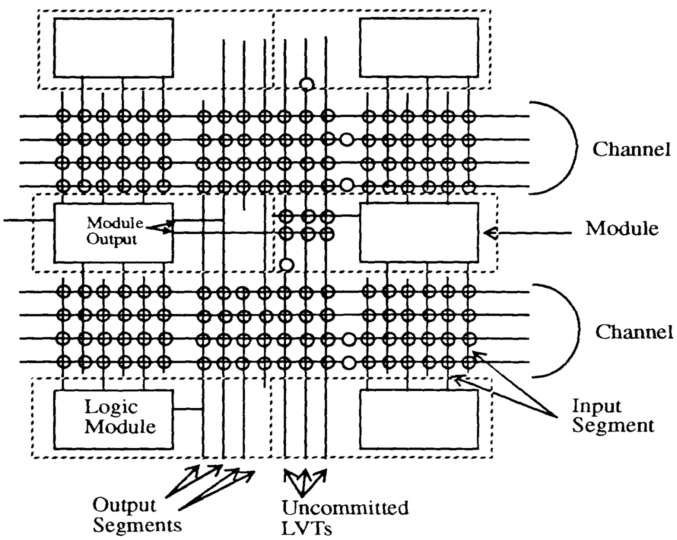


Figure from *Field-Programmable Gate Array Technology*, Trimberger, Kluwer, 1994

- Input segments connect to uncommitted horizontal segment by antifuses
  - Horizontal segments connect by antifuses
- Vertical segments pass over the cells

Actel Act1

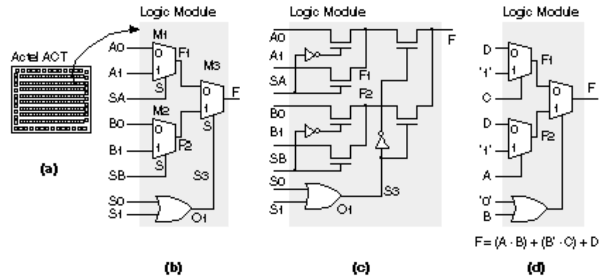


Figure from *Application-Specific Integrated Circuits*, Smith, Addison-Wesley, 1997

- Fairly simple, fine-grained logic module
  - Low delay, small area, very flexible
- Can implement many functions using Shannon's Expansion Theorem
  - Any combinatorial function of 2 inputs
  - Almost any function of 3 inputs, many functions of 4 inputs, some functions of up to 8 inputs
- I/O modules at end of rows & columns

Actel Act2

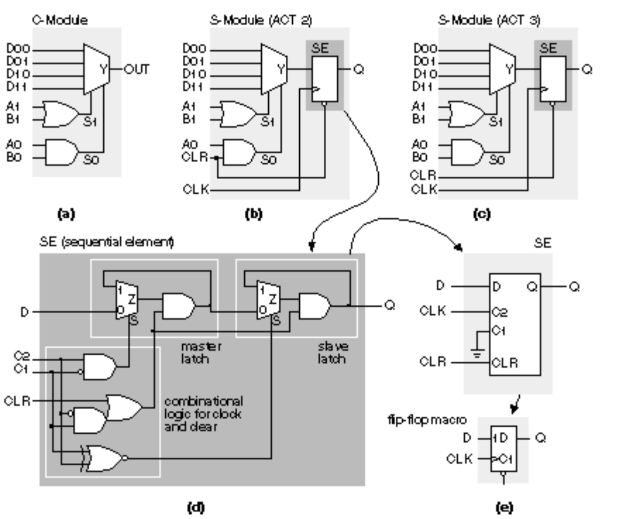


Figure from *Application-Specific Integrated Circuits*, Smith, Addison-Wesley, 1997

- C-module = combinatorial [sic] module
- S-module = sequential module
- Note that the timing of a particular logic macro may vary with its implementation

Actel Act2 (cont.)

- C-module = combinatorial module
  - Act2 c-module provides high fan-in
    - Can implement 16 of the 20 four-input gates in the library (Act1 implements 8)
    - Implements 766 distinct combinational functions, including 13% more four-input macros and 12% more five-input macros than Act1
  - Some loss in ability to implement sequential functions
- S-module = sequential module
  - C-module plus two latches
    - Can provide rising- or falling-edge-triggered D flip-flop, or high- or low-level transparent D latch, with clear
    - Can make it look like a c-module by tying C1 to 1 and C2 to 0
    - Need two or more s-modules to build J-K or more complex flip-flops