Altera FPLD Overview

- Altera MAX 5000 (old), 7000, 7000A (new), 9000 (new)
  - Called “Erasable Programmable Logic Devices”, or EPLDs
  - AND-OR cells, EEPROM programming
  - Good for combinatorially-intensive designs
  - 32 to 1024 macrocells, approximately equal to 600 to 20,000 usable gates
- Altera FLEX 6000 (new), 8000, 10K
  - FLEX = “Flexible Logic Element Matrix”
  - Look-up-table cells, SRAM programming
  - Good for designs with high register count, need for in-circuit reconfigurability, or very large designs
  - 2,500 to 250,000 gates

Altera MAX 7000 Macrocell

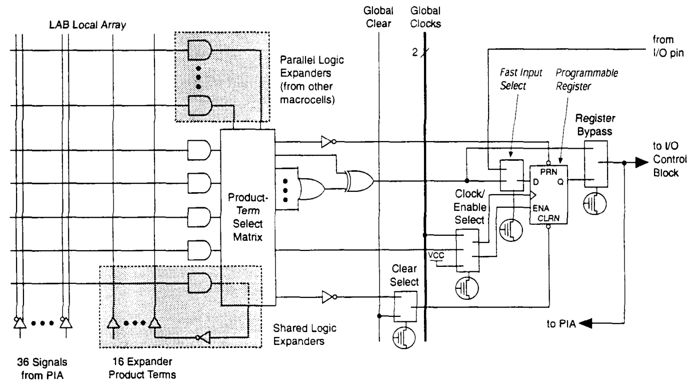

Figure from Altera technical literature

- A MAX 7000 chip contains 2 to 16 Logic Array Blocks (LABs)
  - Each LAB contains 16 macrocells, so a MAX 7000 contains 32 to 256 macrocells
- Macrocell has two parts
  - Logic array and product term selection matrix (combinational)
  - Programmable register (D, T, JK, SR ff)

Altera MAX 7000 Macrocell (cont.)

- Logic array (inside macrocell):
  - 36 inputs from programmable interconnect array (PIA)
    - Each in true and complemented form
  - 5 product terms (*pterms*) (AND gates)
    - *Product term matrix* selects pterms to send to rest of macrocell
  - The *sharable expander* pterm can also be inverted and fed back around to act as an input to any macrocell in that LAB
    - Up to 15 extra pterms for its AND gates
  - All of the pterms in a macrocell can be “borrowed” by an adjacent macrocell in that LAB
    - These are called *parallel expanders*
    - The output of that macrocell’s OR gate is connected to the input of borrower’s OR
    - One macrocell can have as many as 3 sets (<= 5 pterms) of parallel expanders, for a total of up to 20 pterms into its OR

Altera MAX 7000 Macrocell (cont.)

- Product term matrix selects pterms to send to either:
  - OR gate — gives SOP form
  - XOR gate — if “1”, inverts the output of the OR gate
  - Register control inputs (clear, preset, clock, clock enable)
- Register:
  - Can emulate a D, T, JK, or SR flip-flop
  - Can be bypassed to use the macrocell as purely combinational logic
  - Three clocking modes:
    - Global clock signal
    - Global clock with pterm matrix providing clock enable signal
    - Pterm matrix providing clock signal
  - Preset and clear from pterm matrix

Logic Expanders, etc.

- Consider the function

  F = A'CD + B'CD + AB + BC'

  - Can't be implemented using a 3-input OR gate — but what if that's all we have?
  - Rewrite as follows:

    F = (A'+B')CD + (A+C')B

    F = (AB)'(CD) + (A'C)'B

    - Get some of the pterms (e.g., (AB)' and (A'C)') from a sharable expander

- Consider the function

  F = AB' + AC' + AD' + A'CD

  - Again, can't use a 3-input OR gate…
  - Generate complement instead:

    F' = ABCD + A'D' + A'C'

    - Switch 1's and 0's on Karnaugh map
    - Use XOR to invert F' to get F

Altera MAX 7000 Routing

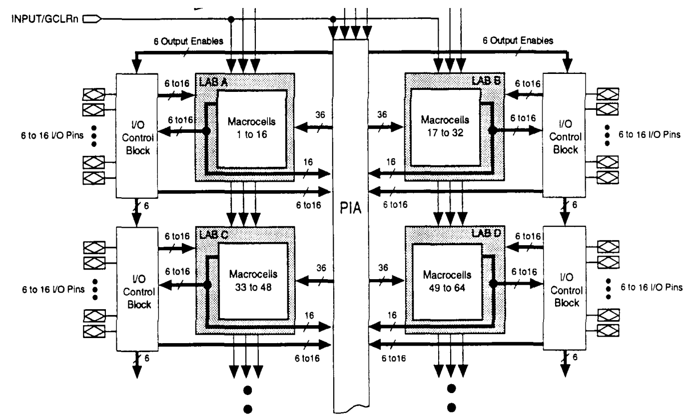

Figure from Altera technical literature

- Logic Array Block (LAB):
  - Contains 16 macrocells (macrocell array), including parallel expanders
  - Connects to
    - Programmable Interconnect Array (PIA) (the 36 inputs described earlier)
    - I/O control block (off-chip connections)

Altera MAX 7000 Routing (cont.)

- I/O Control Block
  - I/O pins connect to
    - I/O control blocks
    - Programmable Interconnect Array (PIA)
  - I/O control block contains the circuitry necessary to program an I/O pin as either:
    - Dedicated output
    - Dedicated input (some devices)
    - Bidirectional pin (some devices)
- Programmable Interconnect Array (PIA)
  - Connects any source signal to any destination the PIA connects to
  - Sources: dedicated inputs, bidirectional I/O pins, and macrocell outputs
  - Layout is fixed, so delay is predictable