Altera FLEX 10K Block Diagram

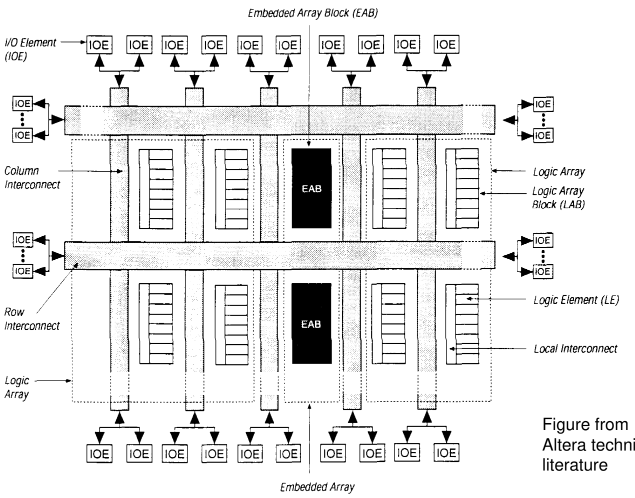

Figure from Altera technical literature

- FLEX 10K chip contains 72–1520 LABs
  - Each LAB contains 8 Logic Elements (LEs), so a chip contains 576–12,160 LEs, totaling 10,000–250,000 usable gates
  - Each LAB also contains 3–20 Embedded Array Blocks (EABs), which can provide 6,164–40,960 bits of RAM

Altera FLEX 10K Embedded Array Blocks (EABs)

- Each LAB contains 3–20 EABs, each of which can be used to implement either logic or memory
- When used to implement logic, an EAB can provide 100 to 600 gate equivalents (in contrast, a LAB provides 96 g.e.'s)
  - Provides a very large LUT
    - Very fast — faster than general logic, since it's only a single level of logic
    - Delay is predictable — each RAM block is not scattered throughout the chip as in some FPGAs
  - Can be used to create complex logic functions such as multipliers (e.g., a 4x4 multiplier with 8 inputs and 8 outputs), microcontrollers, large state machines, and DSPs
  - Each EAB can be used independently, or combined to implement larger functions

Altera FLEX 10K Embedded Array Blocks (cont.)

- When used to implement memory, an EAB can provide 6K–40K bits of RAM
  - Each EAB provides 2,048 bits of RAM, plus input and output registers
  - Can be used to implement synchronous RAM, ROM, dual-port RAM, or FIFO
  - Each EAB can be configured in the following sizes:
    - 256x8, 512x4, 1024x2, or 2048x1
  - To get larger blocks, combine multiple EABs:
    - Example: combine two 256x8 RAM blocks to form a 256x16 RAM block
    - Example: combine two 512x4 RAM blocks to form a 512x8 RAM block
    - Can even combine all EABs on the chip into one big RAM block
    - Can combine so as to form blocks up to 2048 words without impacting timing

Altera FLEX 10K Embedded Array Blocks (cont.)

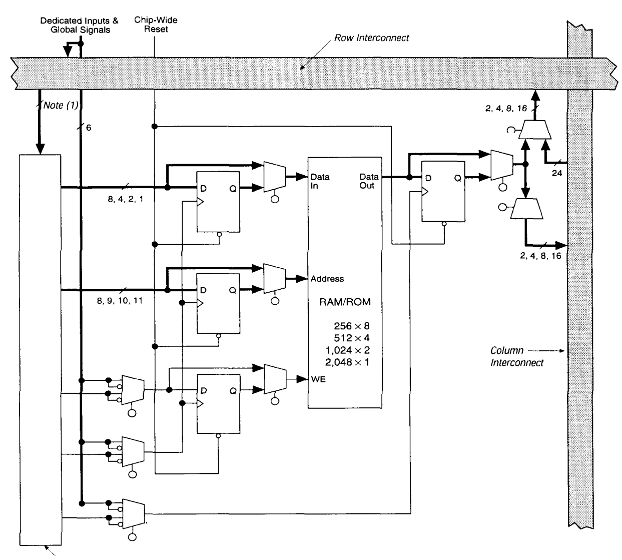

Figure from Altera technical literature

- EAB gets input from a row channel, and can output to up to 2 row channels and 2 column channels
- Input and output buffers are available

Altera UP 1 Education Board

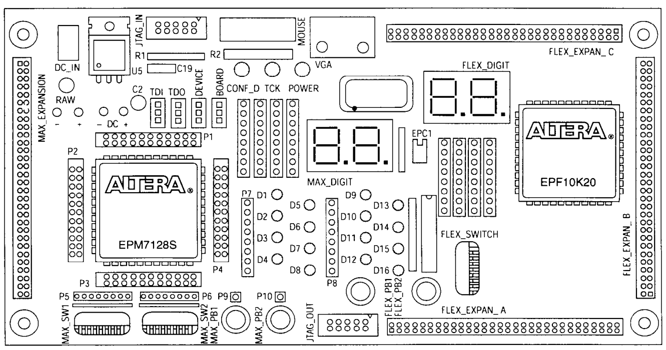

Figure from Altera technical literature

- Contains one EPM7128S device
  - Socket-mounted 84-pin PLCC package
  - 128 macrocells = 2,500 gates (AND-OR, EEPROM)
- Contains one EPF10K20 device
  - 240-pin RQFP package
  - 1,152 LEs and 6 EABs = 20,000 gates (LUT, SRAM)

Altera UP 1 Education Board (cont.)

- Resources available for 7128
  - 2 push-button switches (active low)
  - 2 octal dip-switches (active low)
  - 16 LEDs (active low)
  - Two-digit 7-segment display (active low)
  - Expansion port (left side of board)
  - Connect to female headers around chip
- Resources available for 10K20
  - 2 push-button switches (active low)
  - 1 octal dip-switch (active low)
  - Two-digit 7-segment display (active low)
  - VGA port, mouse port
  - 3 expansion port (right side of board)
  - Connect to female headers around chip

Altera UP 1 Education Board (cont.)

- Miscellaneous
  - Requires 7 to 12 V, 250 mA or greater, power supply (connector at upper left)
  - Programmed using ByteBlaster parallel download cable (attached to a PC)
  - Jumpers above 7128 control programming — 7128 only, 10K only, or both — and connecting multiple boards
- MAX-PLUS II software
  - 7.21 Student Edition in Salcic book
    - Runs on PCs, you can install at home, will be installed in VLSI Design lab
    - Must register with Altera to use
  - 8.0 = “real” version
    - Installed on HP workstation “vlsi”
  - Work at home, in VLSI lab, or on any dept workstation or xterminal, then come to the VLSI lab to download & test your design