Xilinx XC4000

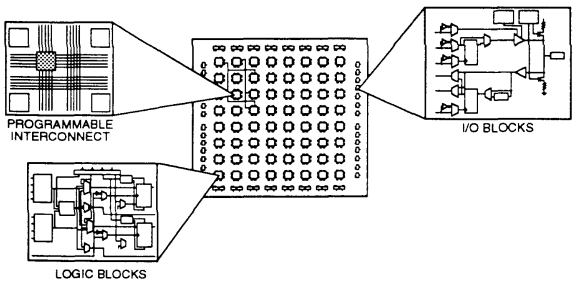


Figure from *Field-Programmable Gate Array Technology*, Trimberger, Kluwer, 1994

- Based on LUTs and SRAM programming
- Xilinx XC4000 chip contains a matrix of Combinational Logic Blocks (CLBs)
  - Chips range from 10x10 to 56x56 CLBs
  - Each CLB can be used for logic or RAM
    - Used entirely as logic, a chip provides 3,000–85,000 gates
    - Used entirely as RAM,a chip provides 3,200–100,352 bits of RAM
    - With “typical” usage of 20–30% RAM, a chip provides 2,000–55,000 gates

Xilinx XC4000 Combinational Logic Block

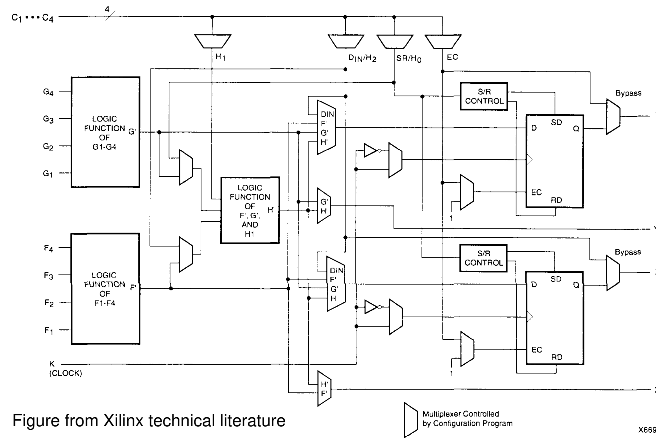


Figure from Xilinx technical literature

- Each Combinational Logic Block (CLB):
  - Two 4-input LUTs (called “function generators” F and G)
    - A 3-input LUT, which has 1–3 of its inputs coming from outside the CLB
    - CLB can implement two 4-variable functions, one 5-variable function, or some functions of up to 9 variables
  - Two edge-triggered D flip-flops

Xilinx XC4000 CLB Carry Logic

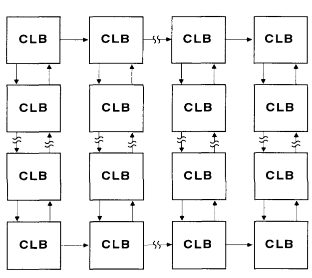


Figure 12: Available XC4000E Carry Propagation Paths

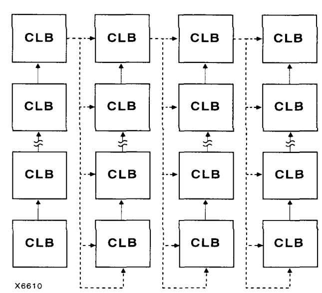


Figure 13: Available XC4000X Carry Propagation Paths (dotted lines use general interconnect)

Figure from Xilinx technical literature

- *Fast carry logic* provides carry and borrow signals
  - Not shown on previous slide, this computation occurs between CLB inputs and F & G LUTs
  - Results are propagated between CLBs
  - Flexibility is limited in high-capacity XC4000X series to improve speed
  - Allows high-speed address calculation, high-speed addition for DSP, etc.

RAM

- LUTs can be treated as RAM cells
- Single-port operation
  - Configure as either one 16x2 or 32x1 bit array (both LUTs), two 16x1 bit arrays (both LUTs), or one 16x1 bit array (one LUT; use the other as logic)
  - Each has a common read / write port
  - Synchronous (edge-triggered) operation
  - Asynchronous (level-triggered) operation
- Dual-operation
  - Configure as one 16x1 bit array, using both LUTs
  - One write port, two read ports
    - Supports simultaneous read and write operations to same or different addresses
  - Synchronous (edge-triggered) operation

Xilinx XC4000 I/O Block

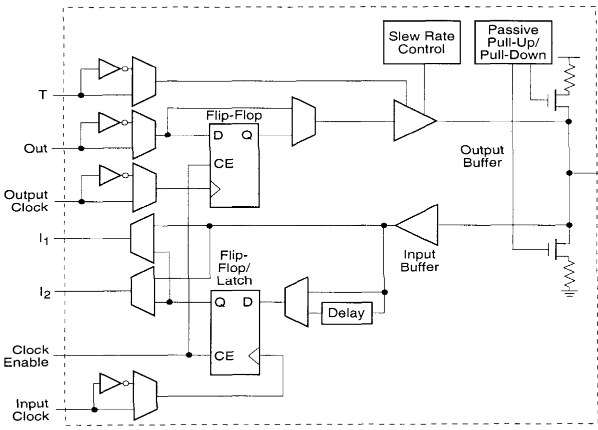


Figure from Xilinx technical literature

- Two I/O Blocks (IOBs) are at the end of each row and column
  - Each IOB contains an input register / latch and an output register / latch
  - Two inputs (to chip): direct & register
  - The associated I/O pin can be used as either an input, output, or bidirectional pin

Xilinx XC4000 Routing

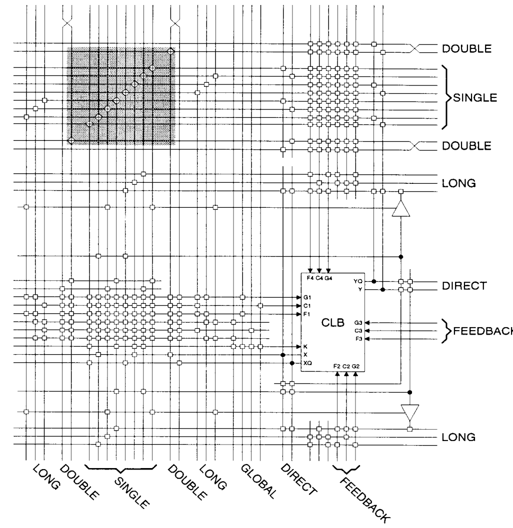
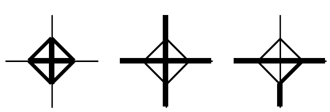


Figure from Xilinx technical literature

- Three kinds of interconnect:
  - Row and column routing
  - IOB routing, which forms a ring around the outside of the CLB array
  - Dedicated networks, primarily intended for clocks, but usable for other signals

Xilinx XC4000 Routing (cont.)

- CLB inputs and outputs connect to channels on all four sides, to provide maximum routing flexibility
- Switch matrix connects rows and columns
  - Six transistors per switch point



- CLBs connect to lines of various lengths:
  - Single-length lines — enter a switch matrix every row / column
  - Double-length lines — enter a switch matrix every two rows / columns
  - Longlines — for high fanout, time-critical nets, or nets that need to be distributed over much of the chip
  - XC4000X only:
    - Quad- and octal-length lines
    - Direct connections between adjacent CLBs