CS 4/55111 **VLSI Design**

Project #2

Due in class on dates shown below

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1. Go through the tutorial in Section 3 of the Altera MAX+PLUS II *Getting Started* manual, entering and compiling the *chiptrip* project. You don't have to do everything in the tutorial, but going through most of it would be highly recommended. For example, you might use the text editor enough to become familiar with it, but then copy the appropriate .tdf files (from the directory **/local/opt/maxplus2/max2work/chiptrip** on vlsi, or from the directory **max2work\chiptrip** on your PC) rather than type in all the tedious details of the state machine.

   When you finish, turn in:
   - printouts of the major components of the design
   - the compilation report file, along with some comments about if and how it changes when you change some of the logic synthesis options
   - waveforms showing the simulation in Session 11, along with a couple of other simulations that demonstrate the two possible ways to get a ticket

   This part is due in class on Wednesday 15 April, and counts 10% of your course grade.

2. Turn in a preliminary proposal for your final project (described in Part 3, below). Give an overview of what you propose to implement for your project, and explain why you chose that project and what you hope to get out of it. Briefly describe the major components of your proposed project, and how it will meet the requirements below.

   This part is due in class on Monday 20 April, and counts 5% of your course grade.

3. For the final class project, use the Altera MAX+PLUS II tools to implement a design of your choice on the Altera UP1 Education Board, subject to the requirements below:
   - you must use either the MAX 7000 or FLEX 10K device on the UP1 Education Board
   - you must use the UP1 Education board, at least one push-button or DIP switch, and at least one LED or 7-segment display as part of your design
   - your design must have at least 3 major components, one of which must be specified using the graphic editor, and one of which must be specified using AHDL and the text editor
   - your design must contain at least one state machine, specified using either AHDL and the text editor or using the waveform editor

   When you finish, turn in an overview describing your design and any major design decisions your had to make. Turn in printouts of the major components, the compilation report file, and simulations showing the operation of the design. Describe any changes that you had to make in the design from what you proposed earlier. All of this is due in class on Wednesday 6 May.

   You will also be required to demonstrate your design on an Altera UP1 Education Board in class during the week of 5/4–5/8.

   This part counts 15% of your course grade.