Class Schedule

Principles of Customized VLSI Design

(29 April 1998)

Date	Lec	Due (Lecs)	Lecture Topic (Section in Text)	Date	Lec	Due (Lecs)	Lecture Topic (Section in Text)	Date	Lec	Due (Lecs)	Lecture Topic (Section in Text)
				1/21	01		Course Introduction	1/23	02		Types of ASICs (Smith 1.1)
1/26	03		Economics of ASICs (Smith 1.4)	1/28	04		ASIC Design Flow (Smith 1.2)	1/30	05		Combinational Logic
2/2	06		Sequential Logic	2/4	07		State Machines	2/6	08		Design Entry (Smith 9.1)
2/9	09		Schematic Capture (Smith 9)	2/11	10		Viewlogic Office (Duckworth 4)	2/13	11		Viewlogic Office (Duckworth 4)
2/16	12		Viewlogic Office (Duckworth 5)	2/18	13		CMOS Transistors & Gates (Smith 2.1)	2/20	14	P1.1 (01–12)	CMOS Fabrication (Smith 2.2)
2/23	15		CMOS Design Rules (Smith 2.3)	2/25	16	P1.2 (01–12)	Toward FPLDs	2/27	17		Types of FPLDs (Salcic 1)
3/2	18		Actel ACT	3/4	19		*finish previous lectures*	3/6	20	P1.3 (01–12)	Altera MAX (Salcic 2.1)
3/9	21		Altera FLEX 8000 (Salcic 2.2)	3/11	22		Altera FLEX 10K (Salcic 2.2)	3/20	23		Xilinx XC4000 (Salcic 2.3)
3/16			**Project Presentations**	3/18			**Project Presentations**	3/20			**Exam 1 (Lecture 01–23)**
Kent Spring Break											
3/30	24		Altera Max-PLUS II Introduction (Salcic 3)	4/1	25		Altera Max-PLUS II Tools (Salcic 3.4)	4/3	26		AHDL Basics (Salcic 4)
4/6	27		Advanced AHDL (Salcic 4)	4/8	28		Design Examples (Salcic 5)	4/10			**No Lecture (Good Friday / Passover)**
4/13	29		SimP Microprocessor (Salcic 6)	4/15	30	P2.1 (24–27)	VHDL Basics (Salcic 7)	4/17			**No Lecture (Walker out of town)**
4/20	31	P2.2 (24–27)	Advanced VHDL (Salcic 7)	4/22	32		Advanced VHDL (Salcic 7)	4/24	33		High-Level Synthesis
4/27	34		Scheduling I	4/29	35		Scheduling II	5/1	36		Data Path Synthesis
5/4			**No Lecture (Longer lectures on WF)**	5/6		P2.3 (24–27)	**Project Presentations (in VLSI Design Lab)**	5/8			**Project Presentations (in VLSI Design Lab)**
5/11	**10:15am–12:30pm**		**Final Exam (Lectures 01–37, emphasis on 24–37)**								