CMOS Transistor Notation

- A CMOS transistor has 3 terminals, called the *gate*, *source*, and *drain*.
- $V_{AB}$ is the voltage between nodes A and B in a circuit.
- Positive power supply (power source)
  - In TTL, written $V_{CC}$ (usually written VCC)
  - In NMOS and CMOS, written $V_{DD}$ (also VDD)
- Negative power supply (power sink)
  - In TTL, written GND (“ground”)
  - In NMOS and CMOS, sometimes written $V_{SS}$ (also VSS)
- CMOS uses positive logic: $V_{DD}$ is logic “1”, $V_{SS}$ is logic “0”

CMOS Transistors as Switches

![CMOS Transistors as Switches](image)

Figure from Application-Specific Integrated Circuits, Smith, Addison-Wesley, 1997

CMOS NAND and NOR Gates

![CMOS NAND and NOR Gates](image)

Figure from Application-Specific Integrated Circuits, Smith, Addison-Wesley, 1997

- Use two transistors to make a CMOS inverter (as shown on previous slide)
- Use four transistors to make a CMOS 2-input NAND gate
  - Rule of thumb: 1 gate = 4 transistors

IC Fabrication Technologies

(Implementing an Inverter)

![IC Fabrication Technologies](image)

Figure from Modern VLSI Design, Wolf, Prentice Hall, 1994

- Bipolar — transistor & resistor (*fastest*)
- NMOS — n-channel depletion mode transistor (top) & n-channel enhancement mode transistor (bottom)
- CMOS — p-channel (*lowest power*) enhancement mode transistor (top) & n-channel enhancement mode transistor (bottom)
Cross-Section of an N-Channel Enhancement Mode MOS Transistor

- Base is silicon substrate (bulk, well, tub) that's been doped with p-type impurities (full of positively-charged holes)
  - Two diffusion areas heavily doped with n-type impurities (full of negatively-charged electrons) form the source and drain
  - Transistor action takes place at the channel, connecting the source and drain
- A very thin layer of silicon dioxide (SiO₂), called the gate oxide, insulates the gate, made of polysilicon, from the channel

Operation of an N-Channel Enhancement Mode MOS Transistor

- Works as a switch — gate-to-source voltage regulates the amount of current that can flow between drain and source
  - When V_{GS} = 0, the p-type channel is full of holes, and the n-type source and drain contain electrons
    - The p-n junctions at source and drain form diodes in opposite directions, so no current flows between source and drain
  - As V_{GS} rises above 0, the few n-type impurities that are present in the p-type channel start to attract electrons
    - The electrons migrate toward the (positively charged) gate, but are stopped by the gate oxide, so collect at the top of the channel
    - When V_{GS} rises to the threshold voltage (V_t), enough electrons have collected to form an n-channel inversion layer, which allows electrons to flow from source to drain (current flows from drain to source)

Operation of an N-Channel Enhancement Mode MOS Transistor (cont.)

- N-channel vs. p-channel
  - N-channel: V_{GS} and V_{DS} both positive, gate and source are n-type (electrons), substrate & channel is p-type (holes), when V_{GS} >> V_t electrons accumulate in channel and flow from source to drain, current flows from drain to source
  - P-channel: V_{GS} and V_{DS} both negative, gate and source are p-type (holes), substrate & channel is n-type (electrons), when V_{GS} >> (more negative) than V_t holes accumulate in channel and flow from source to drain, current flows from source to drain
- Current proportional to W/L of transistor
  - Length (L) = parallel to current flow
  - As W increases, more current can flow
  - As L increases, less current flows

Figure from Application-Specific Integrated Circuits, Smith, Addison-Wesley, 1997