## Types of FPLDs

### Type of Base Cell

<table>
<thead>
<tr>
<th>Programming Method</th>
<th>Multiplexor</th>
<th>Look-Up Table (LUT)</th>
<th>AND-OR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Antifuse</td>
<td>Actel ACT 1, ACT 2, ACT 3</td>
<td>Altera MAX 5000, 7000 (Salcic 2.1)</td>
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<td>Quicklogic</td>
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<td>Crosspoint</td>
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<td>EPROM</td>
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<td></td>
<td>Altera MAX 5000, 7000 (Salcic 2.1)</td>
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<td>SRAM</td>
<td>Plessy</td>
<td>Xilinx EPLD</td>
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<td>Altera Flex 8000, Flex 10K (Salcic 2.2)</td>
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<td>Xilinx LCA 2000, 3000, 4000 (Salcic 2.3)</td>
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</tbody>
</table>

### Layout / routing

- **Row-based:** Actel
- **Matrix-based:** Altera, Quicklogic, Xilinx
Actel ACT Routing Architecture

Figure 3.3.4. Routing Using Long Vertical Track (LVT)

Figure 3.3.5. Routing Using LVTs in another Column

Figure from *Field-Programmable Gate Array Technology*, Trimberger, Kluwer, 1994
An Actel FPGA has rows of cells, with horizontal channels between them, and vertical “channels” called columns.

Cell inputs must come from one of the 2 adjacent horizontal tracks (either figure).

Cell outputs can attach to:

- A dedicated vertical track called the “output stub” (see bottom figure)
  - Output stub spans only two channels above and below the cell

- Long vertical tracks— see top figure, where output goes to LVT instead of its dedicated output segment
  - These are vertical segments of varying lengths that can be joined together to form vertical segmented tracks
Actel ACT Routing Architecture (cont.)

- Input segments connect to uncommitted horizontal segment by antifuses
  - Horizontal segments connect by antifuses
- Vertical segments pass over the cells

Figure from *Field-Programmable Gate Array Technology*, Trimberger, Kluwer, 1994
Actel Act1

- Fairly simple, fine-grained logic module
  - Low delay, small area, very flexible
  - Implements basic gates, D latches, etc.
    - Can implement many functions using Shannon’s Expansion Theorem
      - Any combinatorial function of 2 inputs
      - Almost any function of 3 inputs, many functions of 4 inputs, some functions of up to 8 inputs

- I/O modules at end of rows & columns
C-module = combinatorial [sic] module

S-module = sequential module

Note that the timing of a particular logic macro may vary with its implementation

Figure from *Application-Specific Integrated Circuits*, Smith, Addison-Wesley, 1997
Actel Act2
(cont.)

- **C-module = combinatorial module**
  - Act2 c-module provides high fan-in
    - Can implement 16 of the 20 four-input gates in the library (Act1 implements 8)
    - Implements 766 distinct combinational functions, including 13% more four-input macros and 12% more five-input macros than Act1
  - Some loss in ability to implement sequential functions

- **S-module = sequential module**
  - C-module plus two latches
    - Can provide rising- or falling-edge-triggered D flip-flop, or high- or low-level transparent D latch, with clear
    - Can make it look like a c-module by tying C1 to 1 and C2 to 0
    - Need two or more s-modules to build J-K or more complex flip-flops
Altera FPLD Overview

- MAX 5000 (obsolete), **7000 (in Salcic book)**, 9000 (newer), 3000 (newest)
  - AND-OR cells, EEPROM programming
  - 32 to 560 macrocells, approximately equal to 600 to 12,000 usable gates

- FLEX **8000 (obsolete, in Salcic book)**, 10K, 6000 (new)
  - FLEX = “Flexible Logic Element Matrix”
  - Look-up-table cells plus embedded array blocks (memory), SRAM programming
  - 10,000 to 250,000 gates

- APEX 20K (new)
  - MultiCore cells (LUT, product term, embedded memory), SRAM programming
  - 100,000 to 1,000,000 gates
A MAX 7000 chip contains 2 to 16 Logic Array Blocks (LABs)

- Each LAB contains 16 macrocells, so a MAX 7000 contains 32 to 256 macrocells

- Macrocell has two parts
  - Logic array and product term selection matrix (combinational)
  - Programmable register (D, T, JK, SR ff)
Altera MAX 7000 Macrocell  
(cont.)

- Logic array (inside macrocell):
  - 36 inputs from programmable interconnect array (PIA)
    - Each in true and complemented form
  - 5 product terms (ptersms) (AND gates)
    - Product term matrix selects pterms to send to rest of macrocell
  - The sharable expander pterm can also be inverted and fed back around to act as an input to any macrocell in that LAB
    - “Broadcast” a value within the LAB
  - Some or all of the pterms in a macrocell can also be “borrowed” by an adjacent macrocell in that LAB
    - These are called parallel expanders
    - The output of that macrocell’s OR gate is connected to the input of borrower’s OR
    - One macrocell can have as many as 3 sets (<= 5 pterms) of parallel expanders, for a total of up to 20 pterms into its OR
Altera MAX 7000 Macrocell (cont.)

- Product term matrix selects pterms to send to either:
  - OR gate — gives SOP form
  - XOR gate — if “1”, inverts the output of the OR gate
- Register control inputs (clear, preset, clock, clock enable)

- Register:
  - Can emulate a D, T, JK, or SR flip-flop
  - Can be bypassed to use the macrocell as purely combinational logic
- Three clocking modes:
  - Global clock signal
  - Global clock with pterm matrix providing clock enable signal
  - Pterm matrix providing clock signal
- Preset and clear from pterm matrix
Altera MAX 7000 Routing

Figure from Altera technical literature

- Logic Array Block (LAB):
  - Contains 16 macrocells (macrocell array), including parallel expanders
  - Connects to
    - Programmable Interconnect Array (PIA) (the 36 inputs described earlier)
    - I/O control block (off-chip connections)
Altera MAX 7000 Routing (cont.)

- I/O Control Block
  - I/O pins connect to
    - I/O control blocks
    - Programmable Interconnect Array (PIA)
  - I/O control block contains the circuitry necessary to program an I/O pin as either:
    - Dedicated output
    - Dedicated input (some devices)
    - Bidirectional pin (some devices)

- Programmable Interconnect Array (PIA)
  - Connects any source signal to any destination the PIA connects to
  - Sources: dedicated inputs, bidirectional I/O pins, and macrocell outputs
  - Layout is fixed, so delay is predictable
MAX Devices

■ MAX 7000
  □ 5.0 volt MAX 7000
    ■ 600–10,000 gates, 200 MHz, 44-256 pins
  □ 3.3 volt MAX 7000A, 2.5 volt MAX 7000B
  □ Many packaging options & speed grades

■ MAX 9000 (newer)
  □ 6,000–12,000 gates, 145 MHz, 84-356 pins
  □ Only “bigger” devices, 5v only, fewer speed grades

■ MAX 3000A (newest)
  □ 600–10,000 gates, 192 MHz, 34-208 pins
  □ Only “smaller devices”, 3.3 v, several speed grades
  □ Lowest price per macrocell